



Behavioral Model Application in HSS Simulation

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Talking to the future

Asian IBIS Summit
Shanghai, China
November 4 , 2009

Agenda

- Overview
- Application with IBIS AMI Model
- Application with IBIS AMS Model
- Summary and expectation

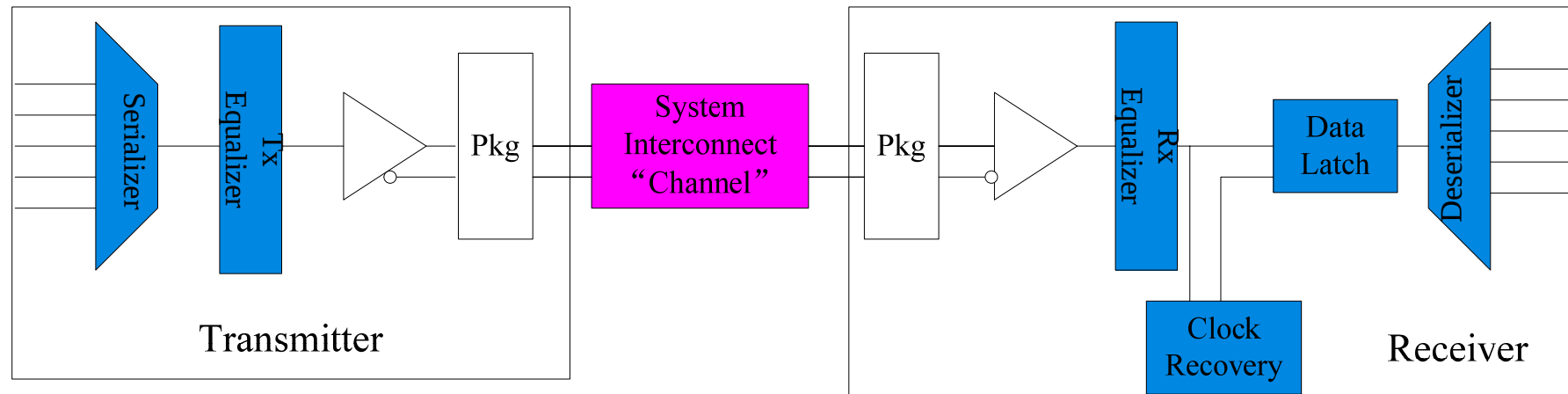
Overview

- The High-Speed Serial (HSS) link Signal Integrity simulation is more important with more uses of Serdes devices.
- Sometimes, the SerDes vendor can't provide the TX&RX spice model for Signal Integrity Simulation for 6Gps+ data rate. Even the models may be provided, the simulation time may be not acceptable.
- SerDes vendor tools always haven't compatibility, so the transceivers must be the same vendor, i.e., the simulation method isn't enough to used for engineering design with different SerDes vendors. Besides, the results is overoptimistic.
- Now, the most effective method to analyze the serial link is through SI and BER test, but it may be too late for finding the questions and the SI test is infeasible.
- For multi-gigabit interconnect system design, the simulation method based on behavioral-level model settles for the simulation time and the precision in engineering compared to other analysis method.

Behavioral-level model

- Use SPICE Model
 - Good accuracy
 - Models are derived from transistor-level netlist and layout
 - Relatively long simulation time and sometimes convergence problems
 - Intellectual property protection concerns
- Use IBIS Model
 - Models are derived from measurements and/or full SPICE model simulations
 - Fast simulation run time
 - Difficult in Modeling complex transceiver buffers, as with Pre-emphasis and Equalizer processing
- Use Macro Model based on IBIS model
 - Fast simulation run time
 - Good accuracy
 - Complex process in Modeling

HSS' Tx&Rx structure



- SerDes-Serializer/Deserializer
- CDR-clock and data recovery
- Passive channel includes pkg of the IC and PCB interconnect based on Linecard or Backplane

AMI Tx/Rx Model example

```
("hss6_cu08.dml"  
(IbisIOCell  
(ideal_50term_pulldown  
(MacroModel  
(MacroType TDiffIO )  
(NumberOfTerminals 8 )  
(SubCircuits "
```

AMI Tx Model

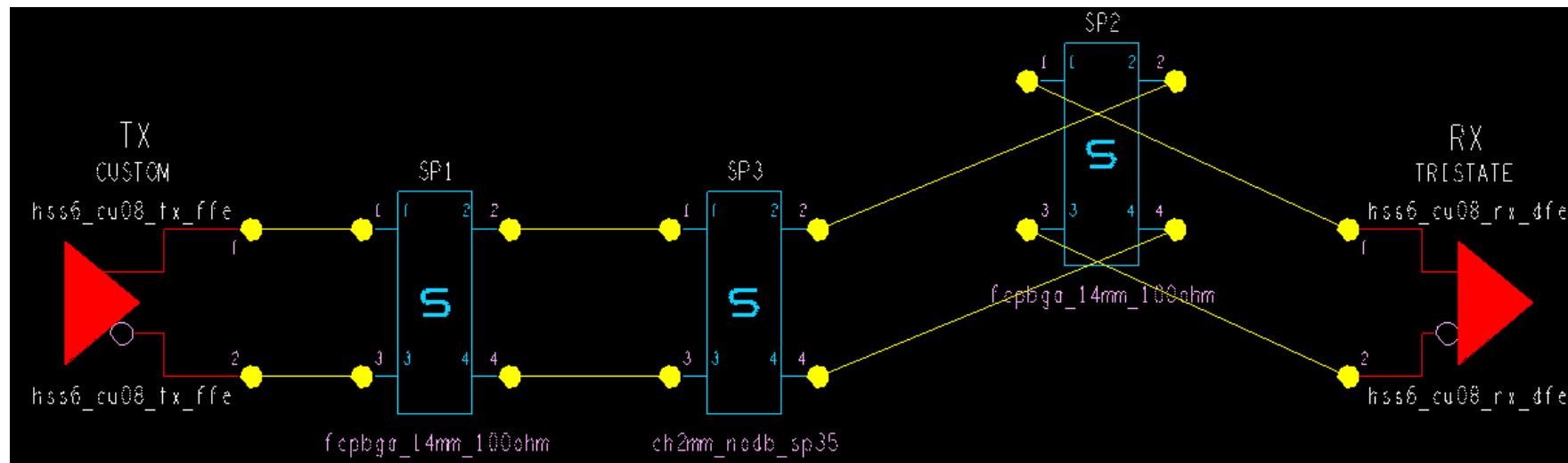
```
(hss6_cu08_tx_ffe  
(ami  
(ibmhsstx_104_win  
(path "D:\\put_in_full_path_to\\dll_lib" )  
(ibis 1 )  
(nffe 4 )  
(rffe 1 )  
(qffe 6 )  
(lffe  
(0.25 1.0 0.5 0.25 ) ) ) )
```

AMI Rx Model

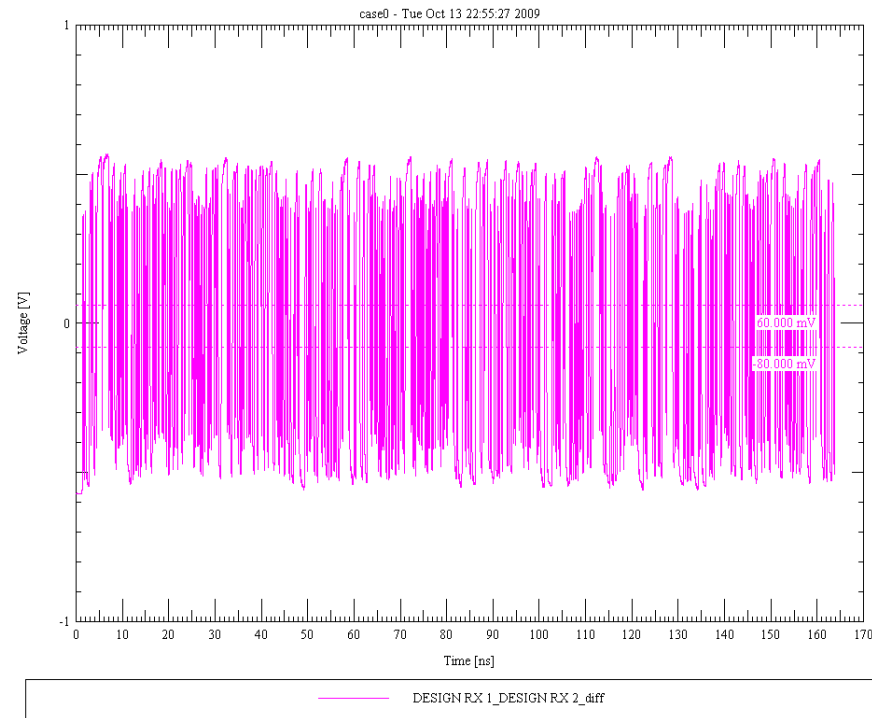
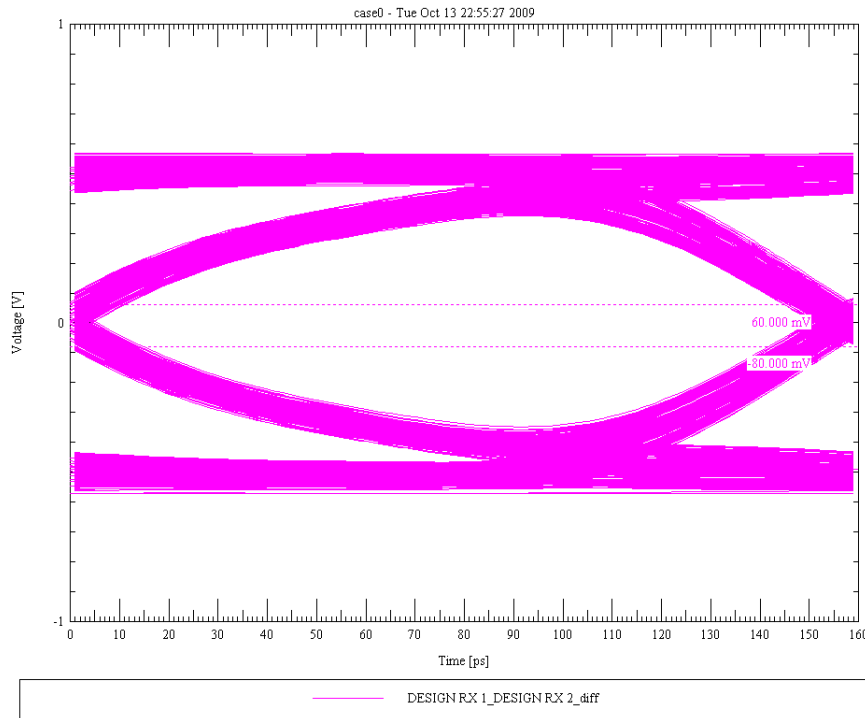
```
(hss6_cu08_rx_dfe  
(ami  
(ibmhssrx_115_win  
(path "D:\\put_in_full_path_to\\dll_lib" )  
(ibis 1 )  
(ndfe 5 )  
(dfelimit  
(0.5 0.25 0.125 0.125 0.125 ) )  
(dfe (0 0 0 0 0 ) )  
(rotlin "..\\..\\..\\..\\include_files/pr_ideal.dat" ) ) )
```

Application with IBIS AMI Model

- The datarate is 6.25Gbps;
- Tx and Rx package models included;
- CDR behavior model embedded in RX model;
- The EDA tool used is Cadence 16.2 SigXplorer;
- IBM AMI model hss6_cu08.dml includes 4-tap Tx FFE, 5-tap Rx DFE;



Simulation results with IBIS AMI Model

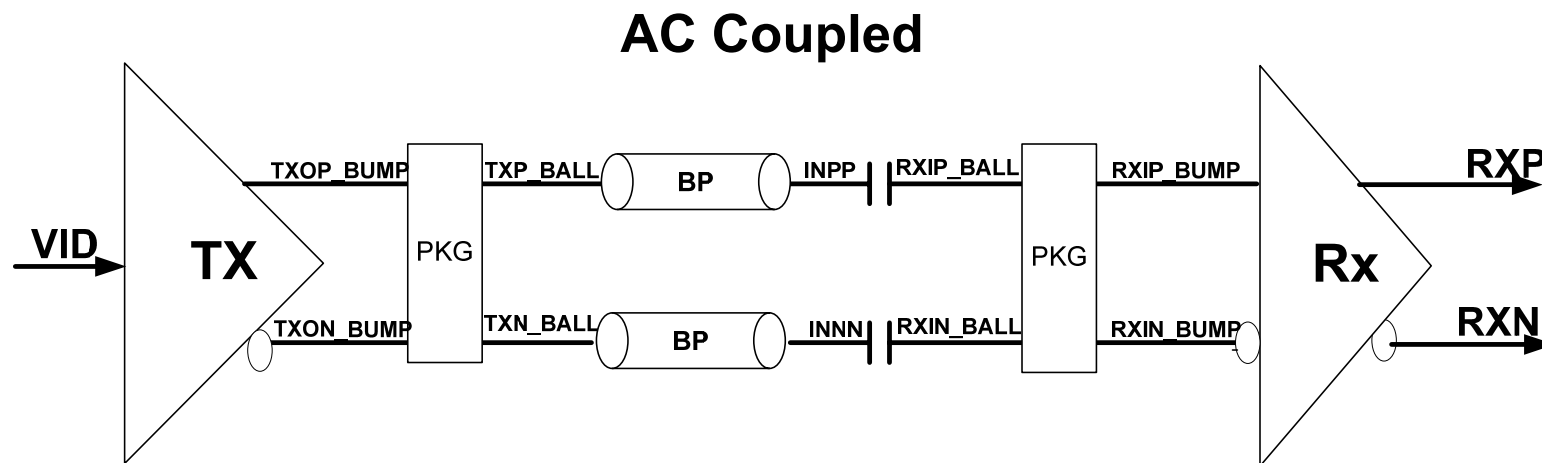


- Eye-Diagram in IBM AMI Model Simulation
- Through tuning the values of DFE and FFE, it is easy to get the good eye-diagram

Application with IBIS AMS Model

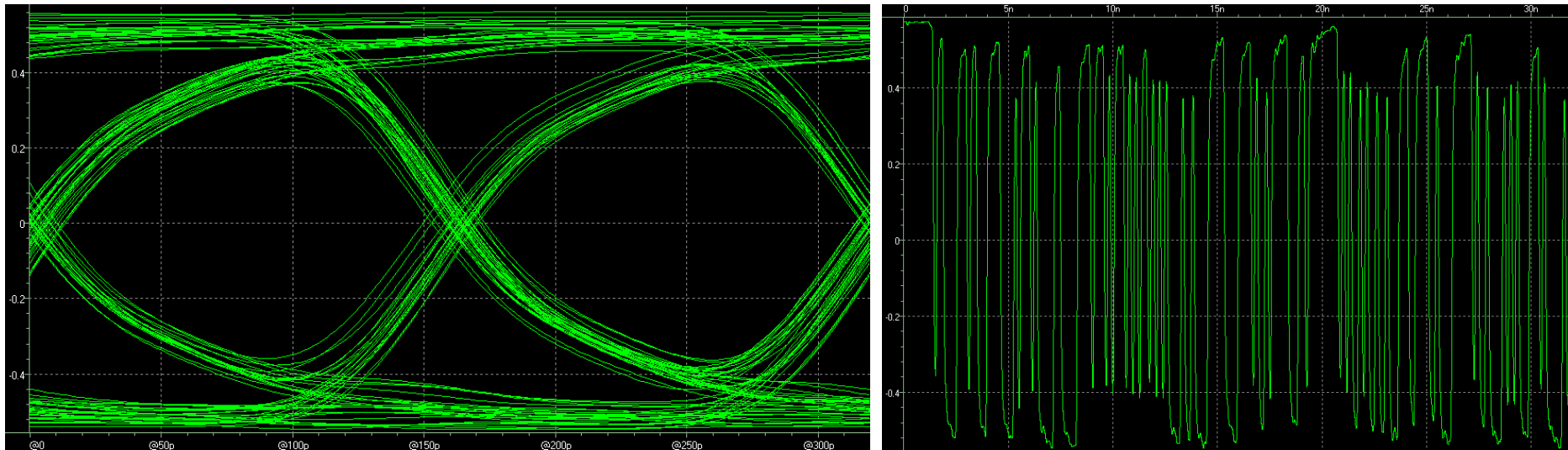
■ IBIS-AMS Modeling:

- The model of transmitters are the Verilog-AMS model;
- The model of receivers are the Verilog-AMS model;
- The following figure shows an example of an Altera TX driver driving an Altera RX receiver through a backplane and AC caps.



TX drives RX through a backplane and AC caps

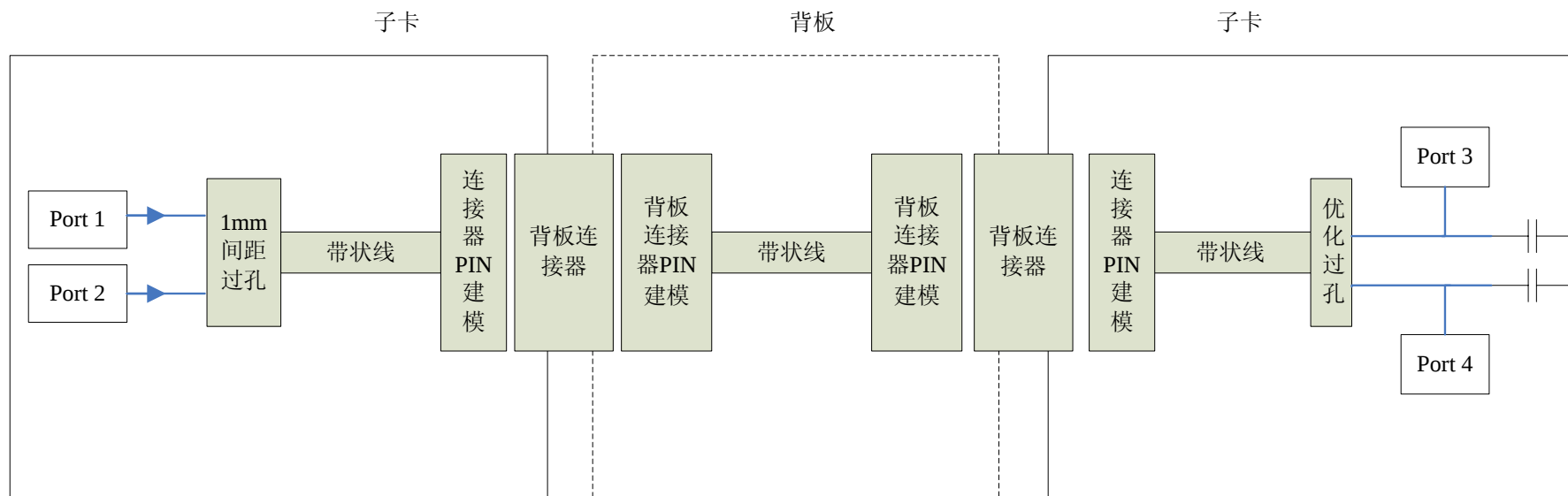
Simulation results with IBIS-AMS Model



- Eye-Diagram in Altera AMS Model Simulation
- The EDA tool used is Hspice, and 200 bits simulated, the consuming time is more than AMI Model Simulation in Cadence 16.2

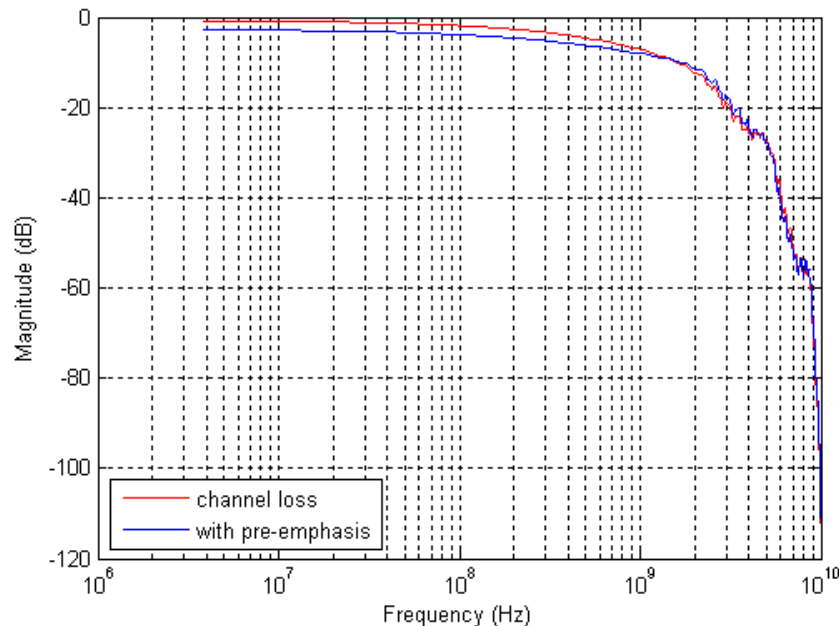
How set coefficients of DFE and FFE

- The S-parameter of the actual serial link channel
- Pre-emphasis and Equalization Link Estimator

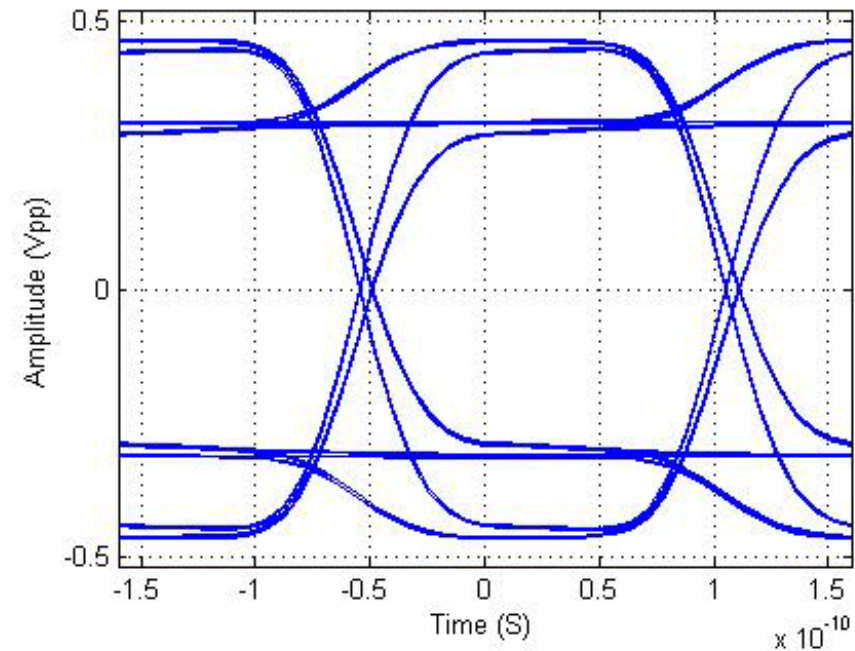


Example for estimating the coefficients of DFE and FFE

Frequency Response of BP ch2mm_nodb_sp35



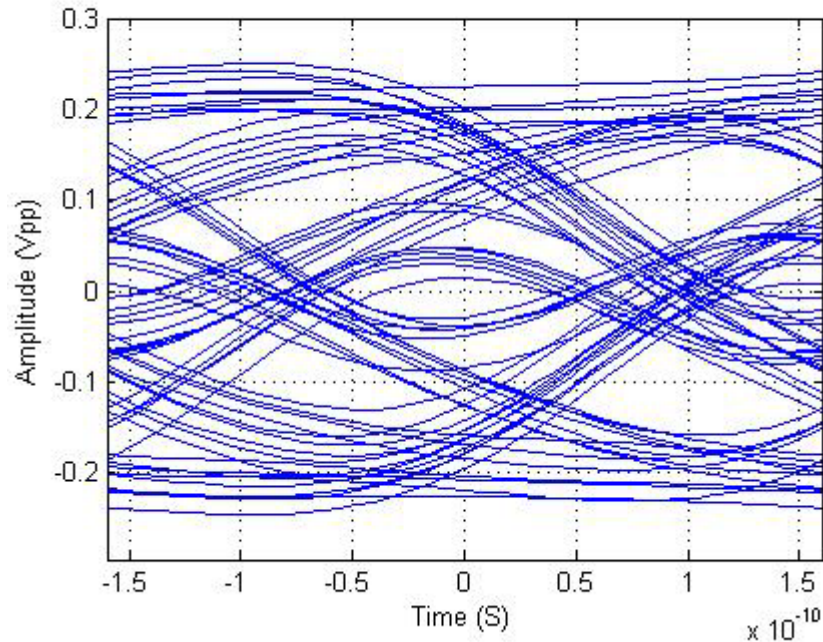
Eye-Diagram at the Near-end of BP ch2mm_nodb_sp35 with Pre-emphasis



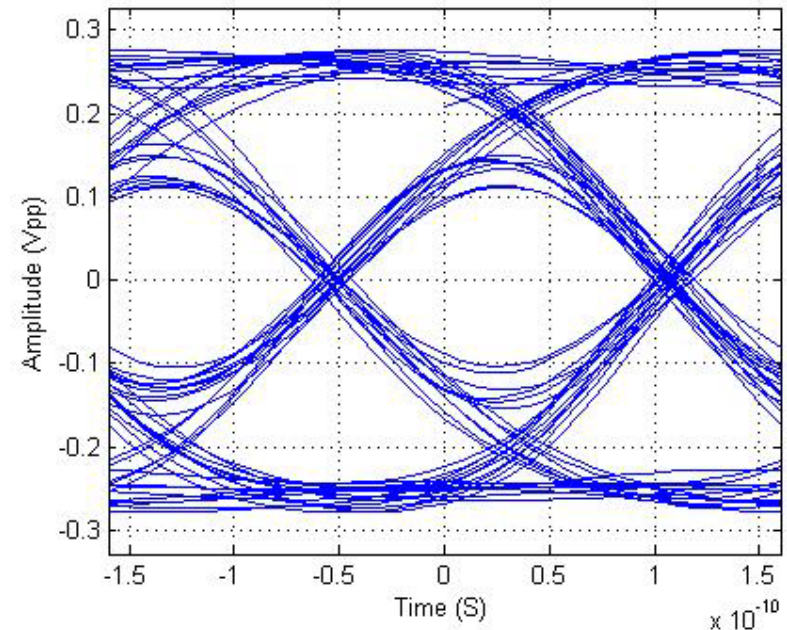
- Frequency Response of ch2mm_nodb_sp35
- Eye-Diagram at the Near-end of ch2mm_nodb_sp35 with Pre-emphasis

Example for estimating the coefficients of DFE and FFE (cont.)

Eye-Diagram at the far-end of BP ch2mm_nodb_sp35 with Pre-emphasis



Eye-Diagram at the Rx Equalizer Output of BP ch2mm_nodb_sp35



- Ch2mm_nodb_sp35 channel Eye-Diagram at the Far-end of Backplane with Pre-emphasis
- Eye-Diagram at the Rx Equalizer Output
- The result with Rx Equalizer is better than no Equalizer

Set the coefficients of DFE and FFE

```
=====
Stratix IV GX Tx pre-emphasis setting is # 4
Pre-emphasis settings are: pre-tap level: -12; post-tap1 level: 0; post-tap2 level: 0
Stratix IV GX Rx equalizer setting is # 4

The horizontal eye-opening is 0.8577 UI
The vertical eye-opening is 0.2141 Upp
Total simulation time is 1.985 min
```

- Quickly and easily narrow the solution space for pre-emphasis and equalization settings for a user defined channel S-parameter model
- Solution of estimating the coefficients of DFE and FFE is efficient
- Getting the open eye-diagram faster than before

HSS Core Vendor model profile

Core name	HSPICE Model	AMI Model	
		Cadence toolkit	Sissoft toolkit
3Gbps Wirebond	Available	Unavailable	Unavailable
ARM PCI-E	Available	Unavailable	Unavailable
ARM SATA	Available	Unavailable	Unavailable
4Gbps standards	Available	Unavailable	Unavailable
PCI-E Gen2	Available	Unavailable	Unavailable
6Gbps Wirebond	Available	Unavailable	Unavailable
6Gbps	Unavailable	Available	Unavailable
11Gbps	Unavailable	Available	Unavailable

- For the evaluating of the 6Gps+ data rate design, the SerDes vendor can't support the TX&RX spice model, the behavioral-level model may be provided, including AMI, Verilog-AMS model, etc.. But the model source isn't enough now. And expect HSS core vendor put more support to release the behavioral-level model.

Summary and expectation

- Behavioral Model Simulation is an efficient and fast method to evaluate the feasibility of designing the multi-gigabit interconnect system.
- Solution with IBIS AMI model and Verilog-AMS model are available for detailed Hardware system design.
- Pre-emphasis and Equalization Link Estimator by HSS vendor used to set the Emp&Eq is complementary to above detailed design solution, but the results of the eye-margin is overoptimistic.
- The research on the HSS simulation with Behavioral Model will go on deeply from ZTE.
- Expect chip vendor put more efforts on generating more effective and accurate IBIS Model for circuit-level's designer as some features contained in IBISv5.0. And EDA vendor can develop corresponding tool to support the simulation based on the models.
- It is expected by chip vendor and circuit-level's designer that develop a conversion tool that can generate IBIS model of higher version from SPICE model;

Thanks

Talking to the future