WELCOME FROM BOB ROSS, TERASPEED CONSULTING GROUP

The IBIS Open Forum welcomes you to our fifth Asian IBIS Summit meeting in the Peoples Republic of China. Based on local interest in signal integrity and related technical issues, we recognized the potential for holding IBIS Summit meetings here. With strong local support, the first Asian IBIS Summit occurred in 2005, and we have continued having successful meetings every year since then.

Thank you for your continued interest during an economically difficult time. We now have 12 co-sponsors, whose financial support and involvement have made these meetings possible.

In addition to working on the well-established IBIS standard, the IBIS Open Forum continues to explore new directions in response to global challenges. This meeting represents part of our global outreach, where we seek and share ideas, experiences and challenges with China and other Asian companies.

We hope you find this meeting a rewarding experience.

Bob Ross
Past Chair 1996-2001
Current IBIS Open Forum Chair

欢迎各位参加第五届亚洲IBIS开放论坛在中国人民共和国的会议。基于中国信号完整性和相关的技术问题，我们认识到在这里举行的IBIS会议的潜力。从2005年第一次亚洲IBIS会议，到之后每年我们成功的会议，都得到了大力的支持。

在目前全球经济困难时期，我们特别感谢您的继续关注和支持。这次会议我们有12个赞助单位，有他们在财政上的支持和参与，我们的会议才能继续下去。

除了现有的IBIS标准的普及工作以外，IBIS开放论坛继续探讨应对全球技术挑战的新方向。这次会议代表了我们向全球拓展，寻求和交流新的思路，经验与中国和其他亚洲公司所面临的挑战。

我们希望您能在本次会议上有所收益。

鲍勃罗斯（Bob Ross）
前任主席 1996-2001
当前的IBIS开放论坛主席

WELCOME FROM LI JINJUN, HUAWEI TECHNOLOGIES

Dear Ladies and Gentleman,
Welcome to the fifth annual Asian IBIS Summit (China). I would like to express my appreciation to IBIS group and all the sponsors, for co-organizing this event.

Since 2005, IBIS Asian Summit in China has been the top-level international conference in high speed digital design society in China. I am looking forward to working with IBIS members in China, and to expanding our base of participation in the region.

Huawei has been actively involved in all IBIS society's events both regionally and globally. Last year, we made some progresses in IBIS model simulation, such as IBIS model qualification by measurement. Your comments and suggestion will be deeply appreciated!

Welcome all of you to Shanghai! Hope you enjoying all the technical discussions and sharing throughout the meeting, and having a nice journey!

Thank you!
Li Jinjun
Huawei Technologies

各位专家，各位来宾：

欢迎大家来参加第 5 届亚洲 IBIS 技术研讨会，衷心地感谢 IBIS 协会组织本次活动。

自从 2005 年以来，IBIS 技术研讨会已经成为了中国高速设计领域的一次盛会。我很高兴有机会与 IBIS 协会一起促进和扩大在该领域的分享。

华为积极参与各项 IBIS 活动。在过去一年中，我们也取得了一些进步，测试验证模型等，欢迎大家讨论和建议。

欢迎 IBIS 专家来到上海，希望你们能够喜欢所有的技术讨论和会议分享，度过美好一天。

谢谢大家
华为公司 厉进军

Shanghai 2008

AGENDA AND ORDER OF THE PRESENTATIONS

(The actual agenda might be modified)

I B I S S U M M I T M E E T I N G A G E N D A

8:15 REFRESHMENTS & SIGN IN
- Vendor Tables Open at 8:30

9:00 Welcome
- Li, JinJun
  (Huawei Technologies, China)
- Ross, Bob
  (Chair, IBIS Open Forum, Teraspeed Consulting Group, USA)

9:20 **Recent IBIS Activities 5**
Ross, Bob (Teraspeed Consulting Group, USA)

9:35 **C_comp Extraction Methods for High-Speed I/O Buffers . . . 9**
Wang, Lance (IO Methodology, USA)

10:05 BREAK (Refreshments and Vendor Tables)

10:25 **IBIS Quality Review, A Status Review of the IBIS . . . . 22 Quality Specification**
Ekholm, Anders* and LaBonte, Mike** (*Ericsson, Sweden and **Cisco Systems, USA)

10:55 **Huawei's IBIS Model Quality Speciification and . . . . . 30 Technology**
Li, Jun (Huawei Technologies, China)

11:25 **The Use of Optimization in Signal Integrity . . . . . 39 Performance Centric High Speed Digital Design Flows**
Bensalem, Brahim**##, Wang, Lihau*#, Gupta, Sanjeev*# and Yuan, XuLiang*## (*Agilent Technologies and **Intel Corporation, #USA and ##China)

12:00 FREE BUFFET LUNCH (Hosted by Sponsors)
- Vendor Tables

AGENDA AND ORDER OF THE PRESENTATIONS (Continued)

Recent IBIS Activities

Bob Ross
Asian IBIS Summit
Shanghai, China
November 4, 2009
bob@teraspeed.com

New IBIS Logo

New IBIS Officers 2009 - 2010

- Chair: Bob Ross, Teraspeed Consulting Group, (past Chair 1996-2001)
- Vice-Chair: Lance Wang, IO Methodology
- Librarian: Anders Ekholm, Ericsson
- Secretary: Randy Wolff, Micron Technology
- Webmaster: Syed Huq, Cisco Systems
- Postmaster: Mike LaBonte, Cisco Systems

- Thank you Michael Mirmak, Intel Corporation for 6 successful years as Chair and host of previous Asian IBIS Summits

TERASPEED CONSULTING GROUP

IBIS Active Since 1993

- Regular IBIS meetings
  - Teleconference/Web meetings every 3 weeks
  - Several standards and documents and parsers
- IBIS Summits (about 5 per year)
  - China, Japan, Europe, and USA (2)
- Active task groups with leading experts
  - **Advanced Technology Modeling** - AMI work
  - **Quality** - IBIS Quality Specification
  - **Interconnect** (ad hoc) - Touchstone Spec., ICM
  - **IBIS Model Review** – Free review service

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"ibischk5" Parser Released

- Ibischk5, Version 5.0.0 for IBIS Version 5.0
  - Free executables: http://www.eda.org/pub/ibis/ibischk5/
  - Source code licenses available for purchase
  - Supports IBIS Version 5.0 (ratified 2008)
    - Algorithmic model interface for Serdes analysis
    - Power delivery system SSO and gate modulation
    - EMI parameters
    - Other – (area based thresholds)
- Checks all [IBIS Ver] versions of IBIS files

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New Flags in ibischk5

```
Usage: ibischk5       <IBS filename>
     : ibischk5  -ebd <EBD filename>
     : ibischk5  -pkg <PKG filename>
     : ibischk5  -ami <AMI filename>
Usage: ibischk5  -caution -numbered      <IBS filename>
     : ibischk5  -caution -numbered -ebd <EBD filename>
     : ibischk5  -caution -numbered -pkg <PKG filename>
     : ibischk5  -caution -numbered -ami <AMI filename>
The flags prior to the file name can be in any order,
and the -caution and/or -numbered flags are optional.
```

- **–ami** for <file_name>.ami (algorithmic model interface control file)
- **–numbered** for numbered **E**rror, **W**arning, **N**otes and **C**aution messages

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ibischk5 {–numbered} –ami file4.ami

```
Checking file4.ami for IBIS 5.0 Compatibility...

ERROR - Illegal Usage value A specified for Param1
ERROR - Illegal Type value B specified for Param1
ERROR - Illegal Format value C specified for Param1
ERROR - No Reserved_Parameters found

Errors  : 4

File Failed
```

```
Checking file4.ami for IBIS 5.0 Compatibility...

E4627 - Illegal Usage value A specified for Param1
E4627 - Illegal Type value B specified for Param1
E4627 - Illegal Format value C specified for Param1
E4622 - No Reserved_Parameters found

Errors  : 4

File Failed
```

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Released or Current Projects (Some covered in Agenda*)

- Touchstone Version 2.0 ratified in April 2009*
  - Public Touchstone parser "tschk2" by Agilent Technologies (2010)*
  - Future Version 2.1*
- IBIS Quality Specification Version 2.0 soon*
- Algorithmic model interface improvements*
- IBIS Interconnect Spice Subcircuit Specification – (IBIS-ISS) with Synopsys approval (2010)
- IBIS Version 5.1 maintenance and improvement
- IBIS remains active, attracts top talent, and has international participation

TERASPEED CONSULTING GROUP

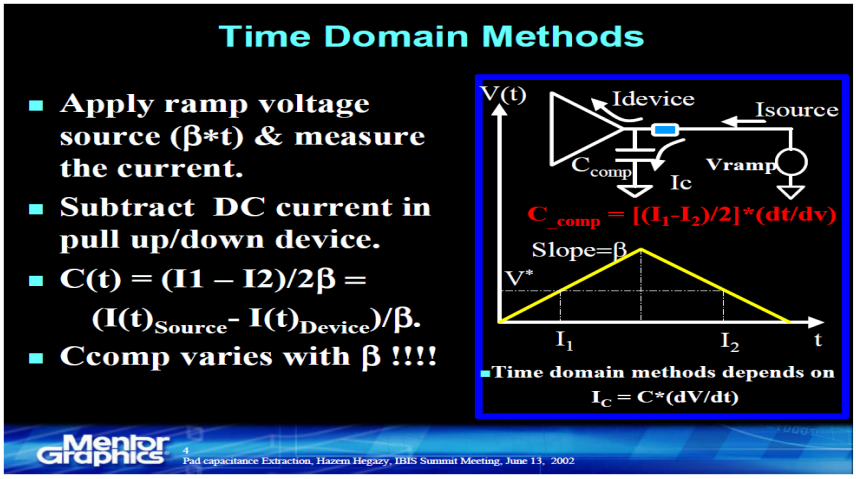
C-comp extraction methods for High-Speed I/O buffers

Lance Wang
(lwang@iometh.com)
Asian IBIS Summit 2009
Shanghai, P.R.China
November 4th 2009

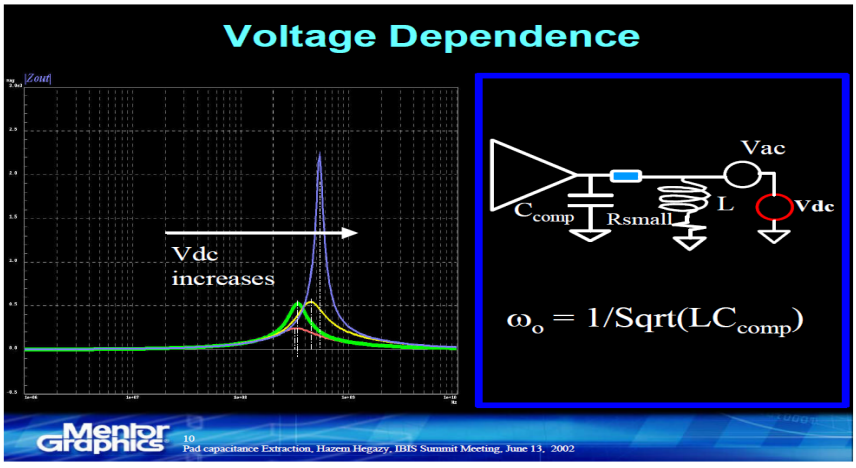
Outlines

- Review C-comp extraction methods
  - Time domain
  - Frequency domain
- Look into C-comp for pullup, pulldown, powerclamp and groundclamp
  - Frequency domain with voltage variables
- Define frequency and voltages
- Conclusions

Time domain

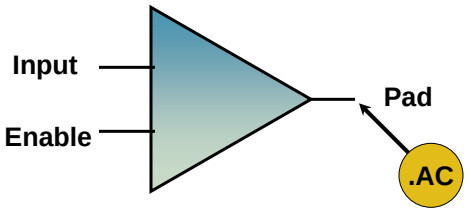


Frequency domain



C-comps for pullup, pulldown, powerclamp and groundclamp

- Pad DC levels
  - 3.3v, 2.2v, 1.1v, 0v
- Input DC levels
  - High, Low
- Enable DC levels
  - Enabled, Disabled

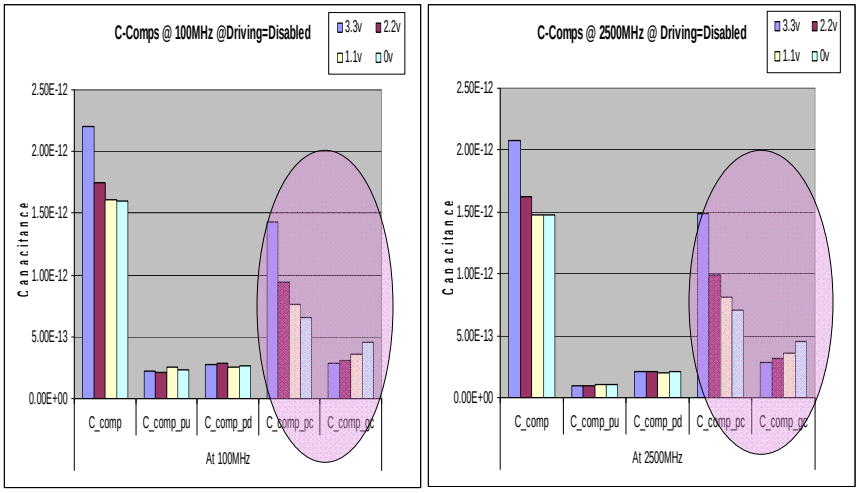


3 DC variables for C-comp frequency-domain extractions

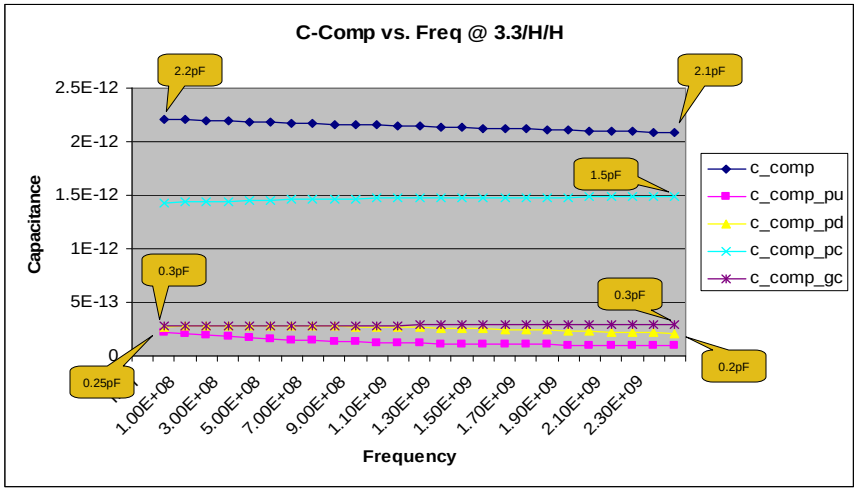
Non-driving mode summary

- Almost identical C-comp values for clamps when frequency changes
- Pad DC levels impact C-comp values for clamps
- For I/O buffers, C-comps values for Pullup and Pulldown may not be zero. They could change with frequency changes
- For I/O buffers, non-driving mode C-comp values are different than driving mode's. They could be big enough to affect your simulation analysis result

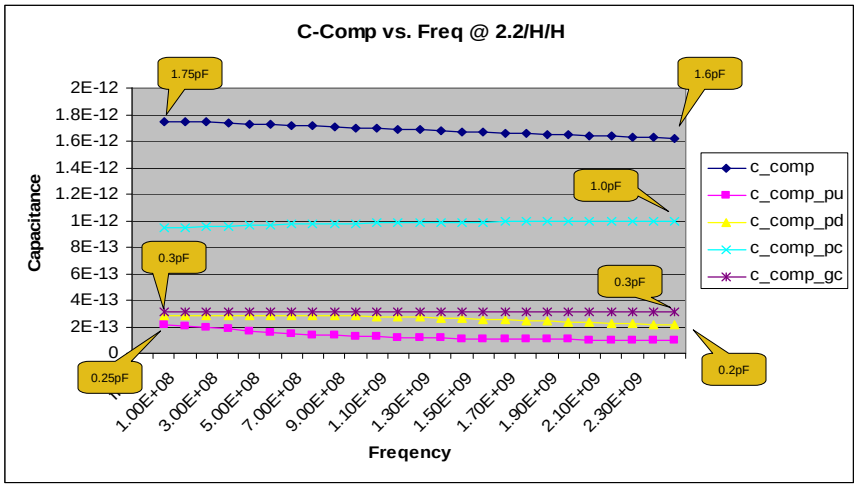
Non-driving mode
@ 100MHz and 2500 MHz



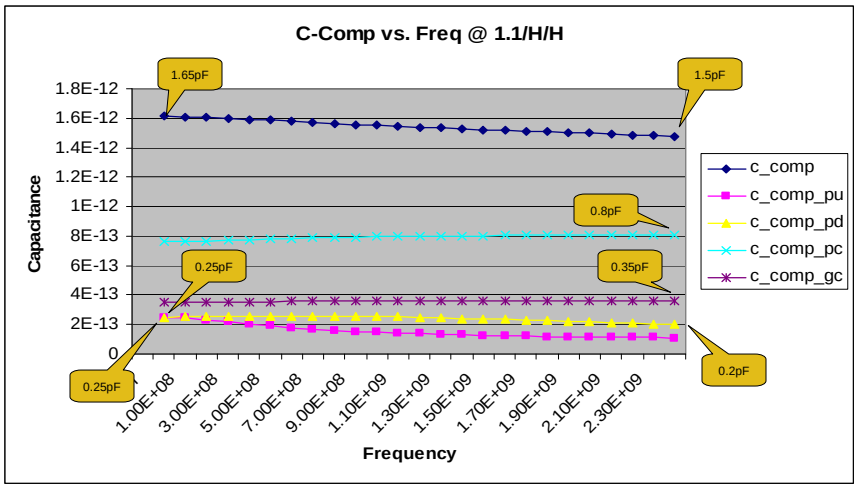
Pad DC = 3.3v
Driving mode = Disabled



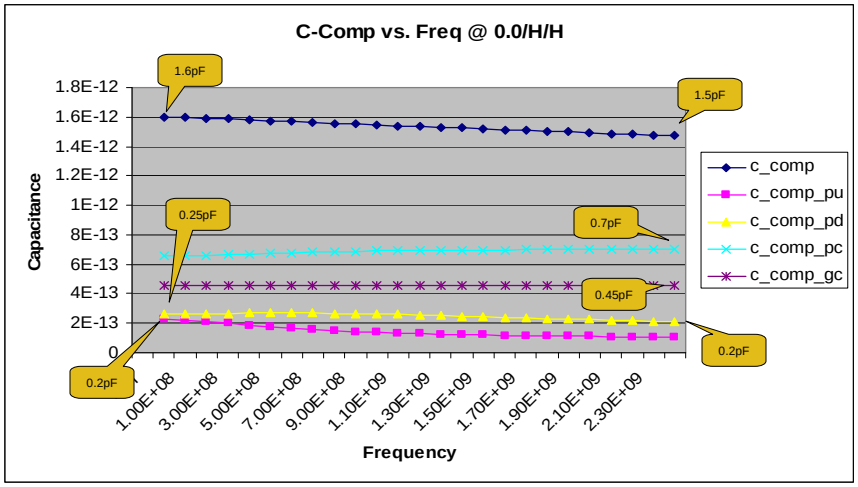
Pad DC = 2.2v
Driving mode = Disabled



Pad DC = 1.1v
Driving mode = Disabled



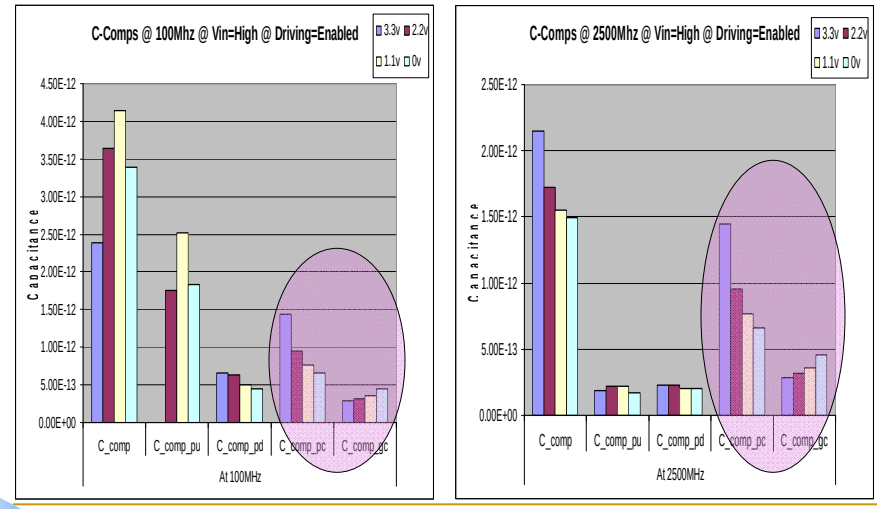
Pad DC = 0.0v
Driving mode = Disabled



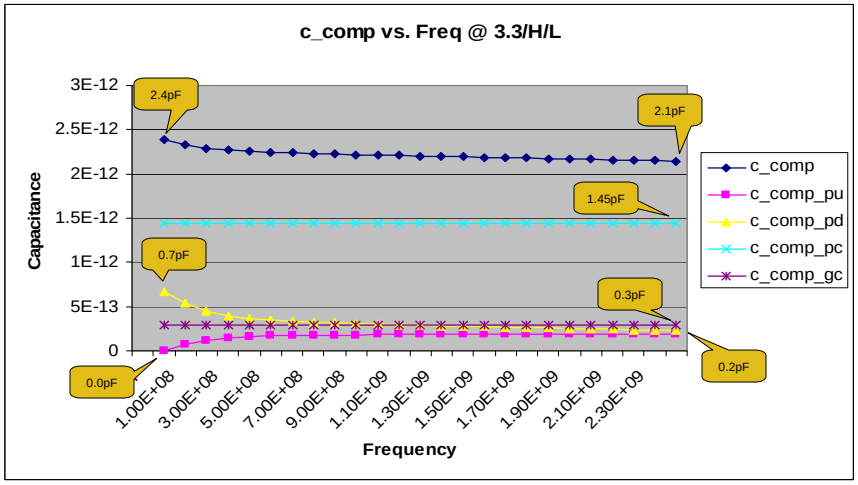
Driving mode summary

- Identical C-comp values for clamps with frequency changes
- Pad DC levels impact C-comp values for clamps
- Pullup and Pulldown C-comp values vary with frequency changes. But it settles at a frequency point and up (being flat)
  - Input DC (level = High) impacts more on Pullup
  - Input DC (level = Low) impacts more on Pulldown

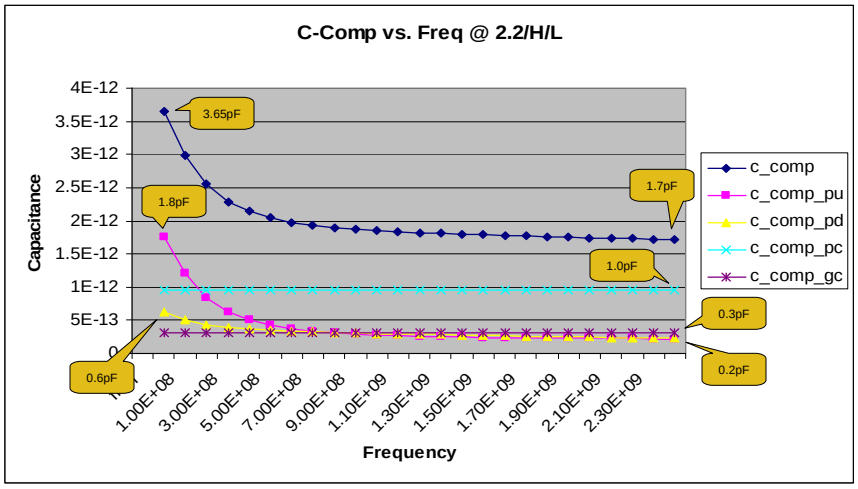
Driving mode with Vin=High @ 100MHz and 2500MHz



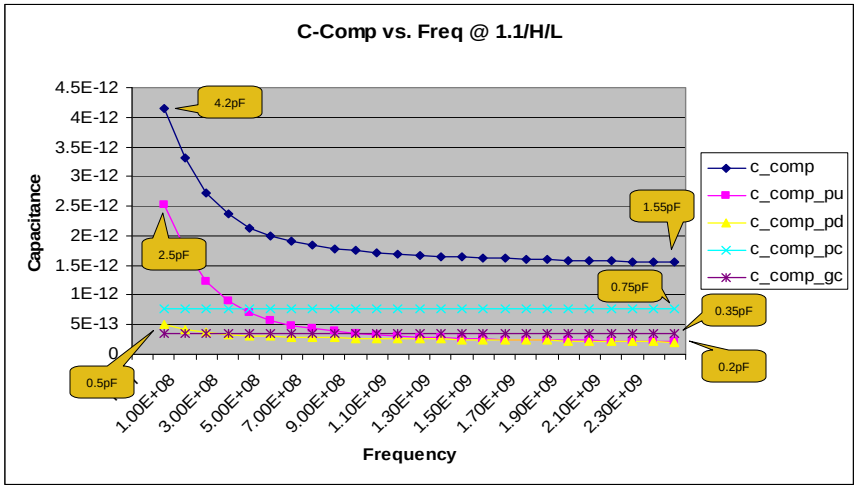
Pad DC = 3.3v, Input DC = High, Driving mode = Enabled



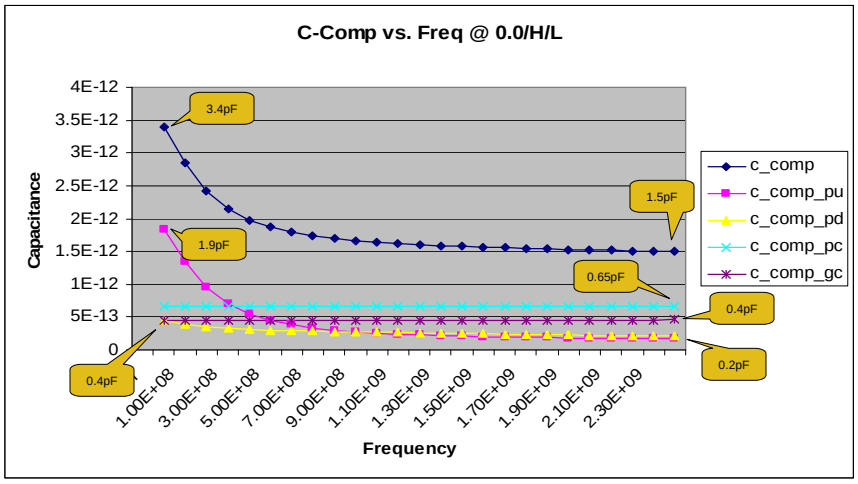
Pad DC = 2.2v, Input DC = High, Driving mode = Enabled



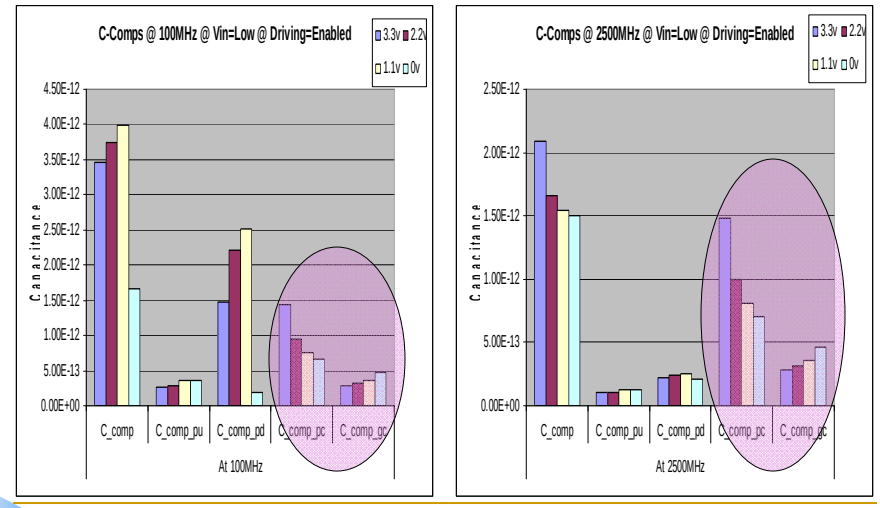
Pad DC = 1.1v, Input DC = High, Driving mode = Enabled



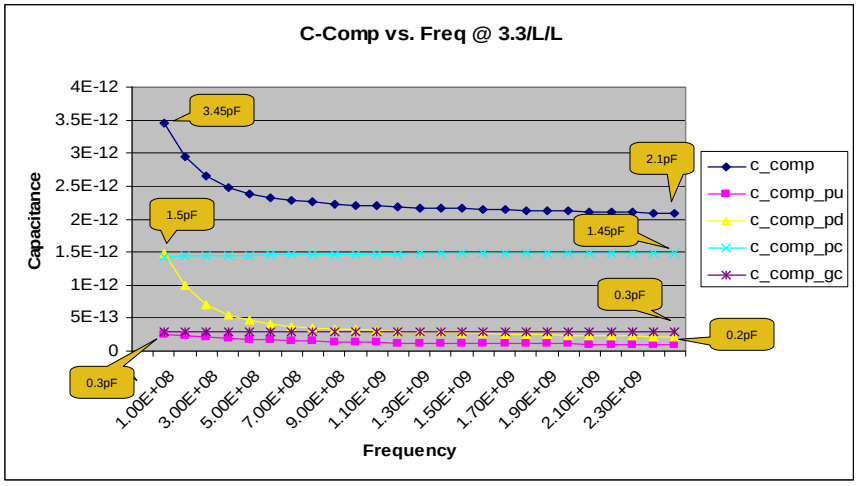
Pad DC = 0.0v, Input DC = High, Driving mode = Enabled



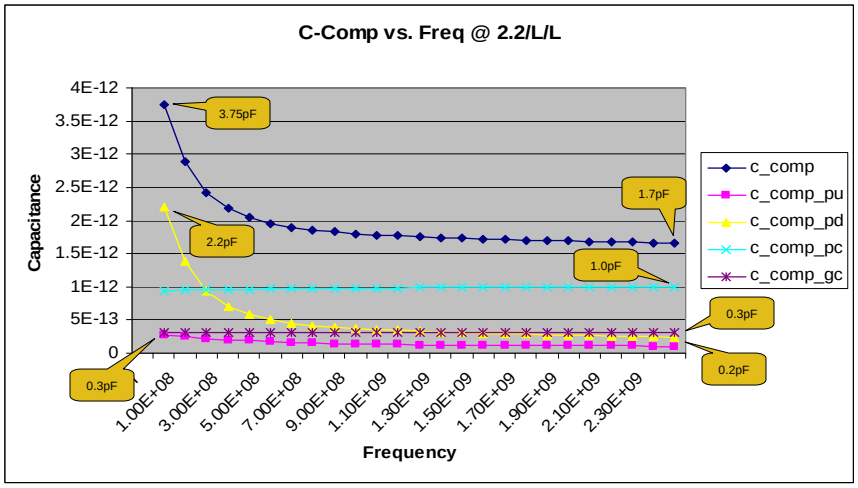
Driving mode with Vin=Low @ 100MHz and 2500 MHz



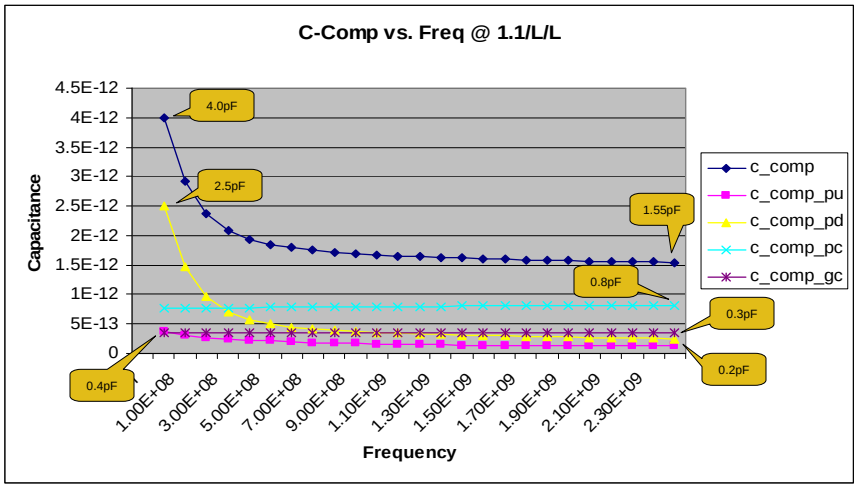
Pad DC = 3.3v, Input DC = Low, Driving mode = Enabled



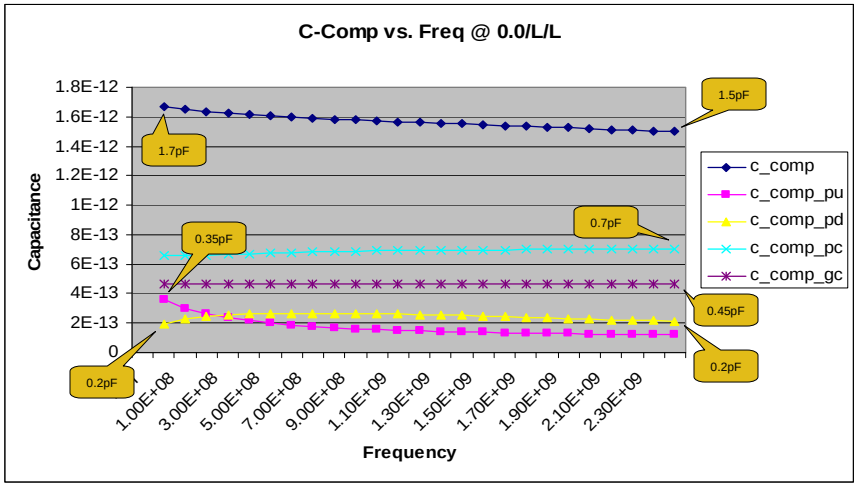
Pad DC = 2.2v, Input DC = Low, Driving mode = Enabled



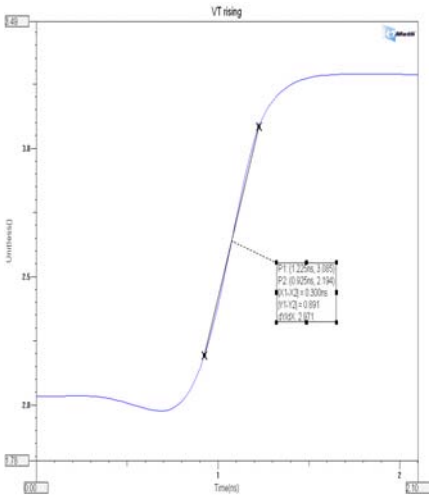
Pad DC = 1.1v, Input DC = Low, Driving mode = Enabled



Pad DC = 0.0v, Input DC = Low, Driving mode = Enabled



Define frequency and voltages



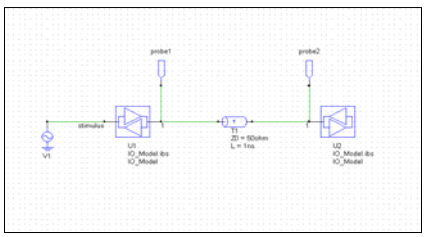
- Frequency
  - Use [Ramp] data as the reference
  - Buffer output frequency (Foutput)

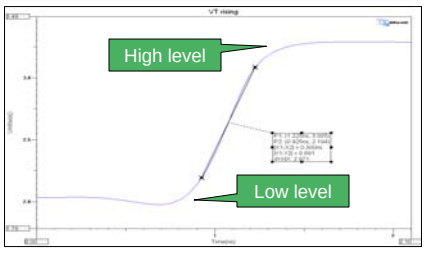
  Foutput = 1/(Rising_dt + Falling_dt)

  (for the most of high-speed buffer, the calculated output frequency point is in the settled region)
- Input buffer c-comp is not impacted much by output frequency changes. But suggest to use slightly higher frequency

Define frequency and voltages

- Voltages
  - Typical application settings
  - Operation voltage ranges
  - Using High and Low level DC settings
  - Averaging extracted C-comp values is a practical way for IBIS model
- Important to correctly define DC voltages





Conclusions

- C-comp (die capacitance) is important in high-speed buffers
- Understand your high-speed buffer die-capacitance arrangement is the first step for extractions
- Frequency domain with defined frequency and DC voltage settings is practical for accurate C-comp extractions
- IBIS specification improvements are required:
  - Separate driving and non-driving mode C-comp values for accurate high-speed simulations
  - Separate different DC level C-comp values for different applications

Thank You

谢谢

ありがとうございました

www.iometh.com

IBIS Quality Review

A status review of the IBIS Quality specification

Asian IBIS Summit, Shanghai China
November 4, 2009

Anders Ekholm, Ericsson & Mike LaBonte, Cisco Systems

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TAKING YOU FORWARD

IBIS Quality Task Group

- **Web:**
  - http://www.vhdl.org/pub/ibis/quality_wip
- **Email list:**
  - http://www.freelists.org/list/ibis-quality
  - Or send email
  - To: ibis-quality-request@freelists.org
  - Subject: subscribe
- **Meetings:**
  - Tuesdays from 11:00am to 12:00pm Eastern Time
- **Questions? Mike LaBonte milabont@cisco.com**

Brief History

- 2002 March - Barry Katz started IBIS-Quality
- 2004 November - IQ 1.0 specification completed
- 2005 August - Parser bug 90 submitted and approved
- 2006 March - Parser bug 94 submitted and approved
- 2006 April - Book “Semiconductor Modeling” discusses IQ (Roy Leventhal, Lynne Green)
- 2006 August - IQ 1.1 specification initiated
- 2009 August - IQ 1.1 renamed IQ 2.0
- 2009 October - IQ 2.0 approval expected

Specification Version 1.0

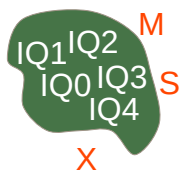
- IBIS Quality Levels
  - 0 Can be checked by IBISCHK, plus a few others
  - 1 Correctness, completeness, and simulation checks
  - 2a Simulation correlated
  - 2b Bench measurement correlated
  - 3 Simulation and measurement correlated

Issues with IQ Version 1.0

- Passing IQ Level 0 does not sound like much of an accomplishment
  - Is a non-compliant file level -1?
- There should be a strict level for “Passes IBISCHK”
- No other IQ check should duplicate IBISCHK
- Can’t have a correlated model without full IQ check
- Some checks are weak (“should” vs. “must”)
- Feedback from JEITA

Specification Version 2.0

- IBIS Quality Levels
  - IQ0 Not Checked
  - IQ1 Passes IBISCHK
  - IQ2 Suitable for Waveform Simulation
  - IQ3 Suitable for Timing Analysis
  - IQ4 Suitable for Power Analysis * (defined, but no checks)
- Special Designators
  - S Simulation correlated
  - M Measurement correlated
  - X Exceptions
  - G Has Golden Waveforms



The Only LEVEL 1 Check (IBISCHK)

2.1 {LEVEL 1} IBIS file passes IBISCHK

Checking a123_test.ibs for IBIS 4.1 Compatibility...

ERROR (line 446) - [Receiver Thresholds] should be specified immediately after all the subparameters of a model and before the other keywords of a model except [Model Spec]
ERROR - Model DQ_FULL Receiver Thresholds: Tslew_ac must be specified for single ended receivers
WARNING - Model DQ_HALF Pullup Typical data is non-monotonic
WARNING - Model DQ_HALF Pulldown Minimum data is non-monotonic
WARNING - Model DQ_HALF Pullup Minimum data is non-monotonic
WARNING - Model DQ_HALF Pullup Maximum data is non-monotonic
WARNING - Model DQ_FULL Pullup Typical data is non-monotonic

Errors : 2
Warnings: 5

File Failed

Example LEVEL 2 Checks (Waveforms)

5.3.7. {LEVEL 2} Combined I-V tables are monotonic
5.3.8. {LEVEL 2} [Pulldown] I-V tables pass through zero/zero
5.3.9. {LEVEL 2} [Pullup] I-V tables pass through zero/zeroI-V
5.3.10. {LEVEL 2} No leakage current in clamp tables
5.3.11. {LEVEL 2} I-V behavior not double-counted

Example LEVEL 3 Checks (Timing)

3.2.2. {LEVEL 3} [Pin] RLC parasitics are present and reasonable
3.3.1. {LEVEL 3} [Diff Pin] Vdiff and Tdelay_* complete and reasonable
5.2.1. {LEVEL 3} [Model] Vinl and Vinh reasonable
5.2.2. {LEVEL 3} [Model Spec] Vinl and Vinh reasonable

Level 4 (Power) Checks for future releases

- A [Pin Mapping] Complete and Correct check was proposed
- Power analysis really needs new features:
  - BIRD95 - Power Integrity Analysis using IBIS
  - BIRD98 - Gate Modulation Effect (table format)
- IBIS 5.0 adoption still in progress
  - IBIS 5.1 may be submitted for EIA/ANSI standardization
  - IBISCHK 5.0 parser released October 2009
  - Have not yet seen IBIS 5.0 power keywords in IBIS files
- Level 4 checks are planned for future IQ 2.x

Notes on IQ Version 2.0

- "Possible Errors" section removed
  - Some items made into regular checks
- "Correlation" section minimized
  - Refers to IBIS Accuracy Handbook for details
- IC vendor push-back on overshoot parameters
  - Not many IBIS files have this
  - Buffer developers simply do not measure it
  - Difference between functional and destruction limits
  - BIRD103 D_overshoot parameters may work better

IQ Version 2.0 Status

- 44 draft revisions posted
- In review phase for IBIS Open Forum acceptance vote
  - Review phase in 3 consecutive Open Forum meetings.
  - Acceptance vote scheduled for October 30, 2009.

After Version 2.0

- File parser bug reports
- Update the IBIS Accuracy Handbook
  - Emphasis on feature-selective correlation
- Begin drafting IQ 2.x
  - Level 4 power analysis checks

Regular 2009 IQ Meeting Participants

- Cisco Systems
- Ericsson
- Huawei Technologies
- Micron Technology *
- Nokia Siemens Networks
- Texas Instruments *
- Teraspeed Consulting Group *
- Xilinx *

* IBIS model makers

Future IQ expectations

- IQ adoption by IC vendors
- Adoption by library flow in system companies
- IBIS modeling tools implementing the IQ checks

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TAKING YOU FORWARD

2009-9-30

Huawei's IBIS model quality specification and technology

Asian IBIS Summit, Shanghai China
November 4, 2009

Lijun
Huawei Technologies Co., LTD
june_lee@huawei.com

www.huawei.com

HUAWEI TECHNOLOGIES CO., LTD.

Overview

Huawei's model quality process

- Golden model specification
- Model quality report

IBIS model Correction

- Correction methodology
- Correction case

Golden Model Specification

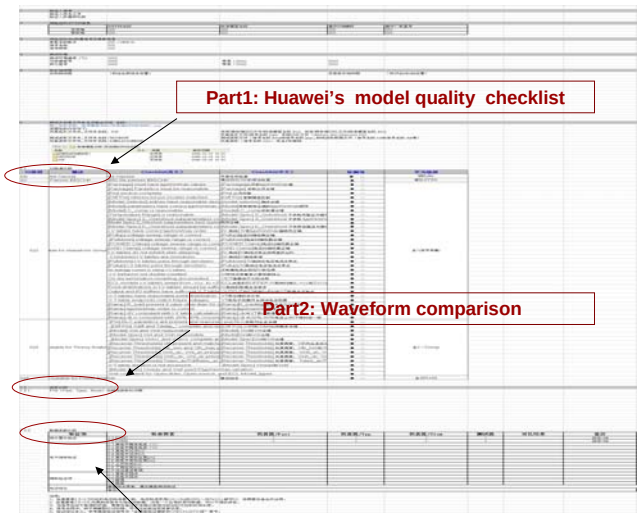
Background:

- IBIS model provided by many different chip vendors;
- System vendor's requirement should be considered in IQ spec

Huawei's specification:

- Huawei follows the IQ Spec, but more detailed;
- Actual PCB measurement based correlation;
- Model level: Copper model
  Silver model
  Golden1 model (for signal reflection)
  Golden2 model (for timing)
  Golden3 model (for SI+PI co-design)

Huawei IBIS Quality report



If passed , Huawei model level will be set as followed:

- Copper model
- Silver model
- Golden1 model (for signal reflect)
- Golden2 model (for timing)
- Golden3 model (for SI+PI co-design)

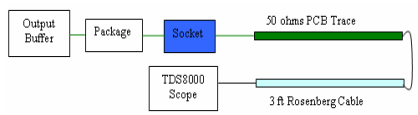
Golden Model Specification

Part1: Huawei's model quality checklist

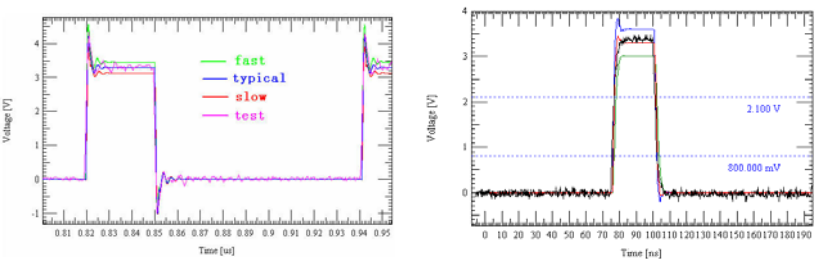
IQ级别	概述	Checklist(英文)	Checklist(中文)	检测项	华为级别
IQ0	Not Checked	Not Checked	未做任何检查	■ □	例Buffer
IQ1	Passes IBISCHK	IBIS file passes IBISCHK	通过IBISCHK的语法检查	■ □	铝BUFFER
		[Package] must have typ/min/max values	[Package]必须有typ/min/max值	■ □	
		[Package] Parasitics must be reasonable	[Package] 参数必须合理	■ □	
		[Pin] section complete	[Pin] 必须完整	■ □	
		[Diff Pin] referenced pin models matched	[Diff Pin] 管脚模型匹配	■ □	
		[Model Selector] entries have reasonable desc	[model selector] 描述合理	■ □	
		[Model] parameters have correct typ/min/max	[Model]参数都有正确的typ/min/max顺序	■ □	
		[Model] C_comp is reasonable	[model] C_comp参数值合理	■ □	
		[Temperature Range] is reasonable	[Model Spec] S_Overshoot 干参数完整且与器件	■ □	
		[Model Spec] S_Overshoot subparameters cor	[Model Spec] S_Overshoot 干参数 typ/min/ma	■ □	
		[Model Spec] S_Overshoot subparameters track typ/	顺序正确	■ □	
		[Model Spec] D_Overshoot subparameters cor	[Model Spec] D_Overshoot 干参数完整且与器件	■ □	
		I-V tables have correct typ/min/max order	[IV 曲线] IV表typ/min/max值顺序正确	■ □	
		[Pullup] voltage sweep range is correct	[Pullup]电压扫描范围正确	■ □	
		[Pulldown] voltage sweep range is correct	[Pulldown]电压扫描范围正确	■ □	
		[POWER Clamp] voltage sweep range is corre	[POWER Clamp]电压扫描范围正确	■ □	
		[GND Clamp] voltage sweep range is correct	[GND Clamp]电压扫描范围正确	■ □	
IQ2	ible for Waveform Simu	I-V tables do not exhibit stair-stepping	[IV 曲线]IV 曲线没有出现明显的台阶	■ □	金1(信号质量)
		Combined I-V tables are monotonic	[IV 曲线]IV 曲线单调	■ □	
		[Pulldown] I-V tables pass through zero/zero	[Pulldown] IV 曲线过电压电流点零点	■ □	
		[Pullup] I-V tables pass through zero/zero	[Pullup] IV 曲线过电压电流点零点	■ □	
		No leakage current in clamp I-V tables	没有漏电流出现在IV表仪表	■ □	
		I-V behavior not double-counted	IV特性没有重复计算到曲线上	■ □	
		On-die termination modeling documented	ODT被模拟行文档说明	■ □	
		ECL models I-V tables swept from -Vcc to +2	ECL类型的BUFFER IV 曲线行扫从-Vcc到2Vcc右	■ □	
		Point distributions in I-V tables should be suffic	IV 曲线的放置点足够多	■ □	
		Output and I/O buffers have sufficient V-T tab	OUTPUT和IO类型buffer的VT放置点足够多	■ □	
		V-T tables have reasonable point distribution	VT表台理的点分布	■ □	
		V-T table endpoints match fixture voltages	VT表电平范围符合测试电压范围	■ □	
		[Ramp] R_load present if value other than 50 o	[Ramp]R_load为电阻值不是50OHM	■ □	
		[Ramp] typ/min/max order is correct	[Ramp]typ/max/min顺序正确	■ □	
		[Ramp] dV consistent with I-V table calculation	[Ramp] dv与VT表计算值一致	■ □	
		[Ramp] dt is consistent with 20%-80% crossin	[Ramp] dt 与20%-80%电压上升/下降时间一致	■ □	

Golden Model Specification

Part2: Waveform comparison: FTS (Fast/typical/slow) simulation VS measurment



Channel S-parameter test

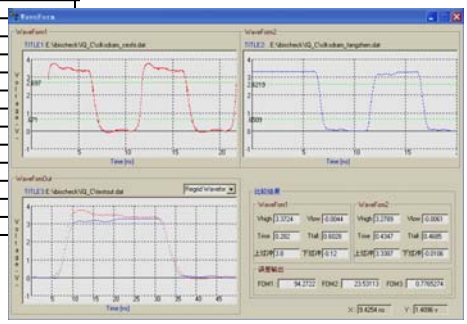


actual PCB measurement VS simulation

Model Quality report

Part3: Electrical Specifications: simulation VS measurement

验证项	检查要素
统计量化验证	1.1 FOM1
	1.2 FOM2
电气指标验证	2.1 高电平稳定电压（V）
	2.2 低电平稳定电压（V）
	2.3 高电平过冲(V)
	2.4 低电平过冲(V)
	2.5 高电平有效位宽(ns)
	2.6 低电平有效位宽(ns)
	2.7 上升时间(ns)
	2.8 下降时间(ns)
	2.9 边沿是否单调
辅助验证项	3.1 高电平回冲
	3.2 低电平回冲
	3.3 眼宽
	3.4 眼高



FOM:

$$FOM1 = 100 \cdot \left[1 - \frac{\sum_{i=1}^{N} |Y1_i - Y2_i|}{YW \cdot N}\right]$$

$$FOM2 = 100 \cdot \left[\frac{\max|Y1_i - Y2_i|}{YW}\right]$$

$$FOM3 = \max|Y1_i - Y2_i|$$

Overview

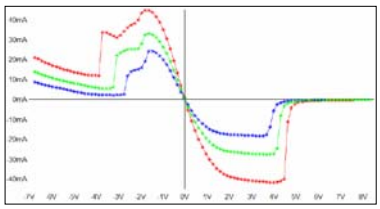
Huawei's model quality process

- Golden model specification
- Model validation/quality report

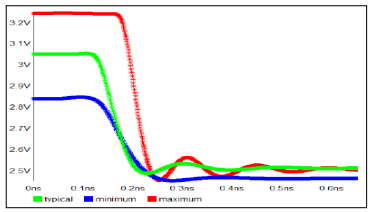
- **IBIS model Correction**
- Correction methodology
- Correction case

Background

- **Once there are some data issues in IBIS model :**



Non-monotonic VI table



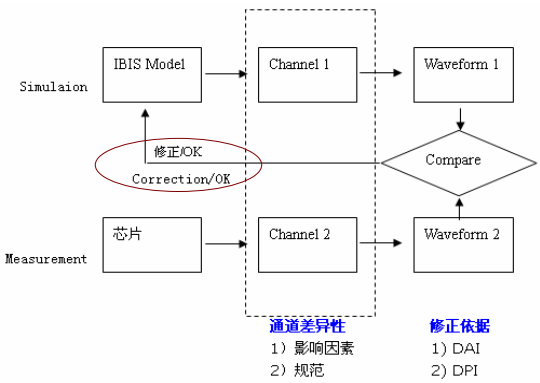
Non-monotonic Vt table

What can we do ?

Correction Methodology

Topology. :

Driver → Interconnect → Receiver



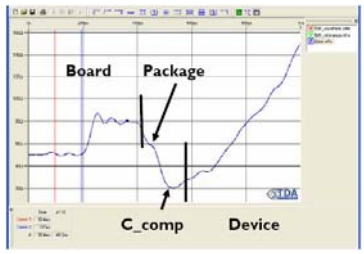
■ It's important to keep consistent with the channel1 and channel2

Correction Methodology

（1） PKG correction

- ✓ PKG and C_comp parameters should match the datasheet
- ✓ PKG and C_comp model should match the TDR curves

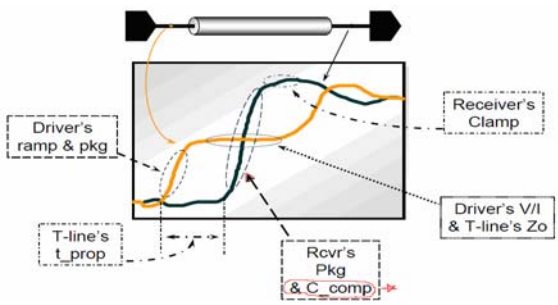
		IBIS		Datasheet (DDR3-1333)	
		Min	max	min	max
DQ	C_comp	1.66pF	1.95pF		
	C package	0.20pF	0.26pF		
	C_total	1.86pF	2.21pF	1.5pF	2.5pF
INPUT	C_comp	0.93pF	1.20pF		
	C package	0.17pF	0.36pF		
	C_total	1.10pF	1.56pF	0.75pF	1.3pF
CLK	C_comp	0.97pF	1.19pF		
	C package	0.20pF	0.21pF		
	C_total	1.17pF	1.40pF	0.8pF	1.4pF



Correction Methodology

（2）VI/VT data table correction

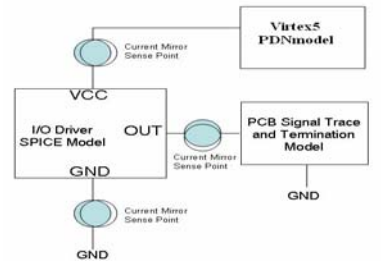
- ✓ VI/VT data is not really accuracy, should be adjusted sometimes;
- ✓ Rubbish VI/VT data in, rubbish waveform out.

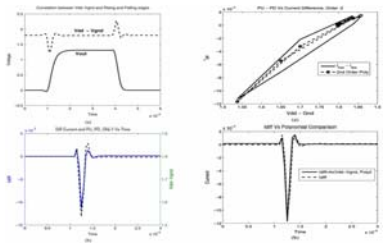


Correction Methodology

（3） Macro model Correction

- ✓ More faster rising edge, more SSN，
- ✓ Traditional IBIS could not support SSN modeling

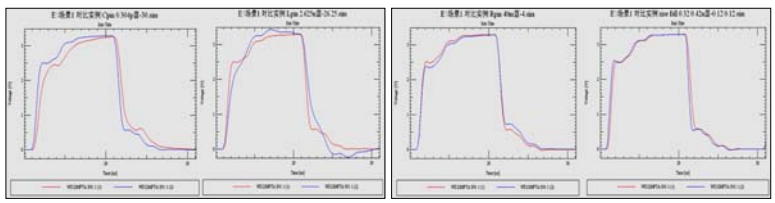




- ■ **We add a behavioral current source in IBIS, modeling the SSN.**
- ■ **Would Improve the simulation accuracy**

Correction case

Correction case：



吻合度参数： 35% → 15% → 10% → 5%

- ■ The correction technology improved the model quality significantly

Conclusion

- Huawei follows the IQ Spec, but more detailed;
- Actual PCB measurement based correlation is significance;
- Model correction technology is a good way to improve model quality;
- Expect to release IBIS correction technology specification

References

● **Official IBIS Website, including tools, articles, specifications**
– http://www.eigroup.org/ibis/

● **iq_ver_2_0.pdf**
– http://www.eda.org/pub/ibis/quality_wip/iq_ver_2_0.pdf

● **IBIS Summit presentations 2007~2008**
– http://www.eda-stds.org/ibis/summits/index-bydate.htm

● **Micron model quality report**
– http://www.micron.com/products/partdetail?part=MT18JSF25672AY-1G1

● **Altera model quality**
– http://www.altera.com/literature/wp/signal-integrity_s2-v4.pdf

● **Mark Alexander Xilinx Corp. 《ssn master circuit》**
– http://www.xilinx.com/products/virtex4/pdfs/virtex-4_power_system_performance.pdf

Thank you

www.huawei.com

The use of Optimization in Signal Integrity Performance Centric High Speed Digital Design Flow

Asian IBIS Summit, Shanghai China
November 4, 2009

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Agenda

- Channel Complexity and Gaps in Current Design Flow
- Advantage of End to End Eye Centric Design Flow
- Why an Eye Diagram ? And Eye Diagram Measurements
- Optimization of DDR2 Channel.
- Introduction to Batch Mode Simulation
- DDR Compliance

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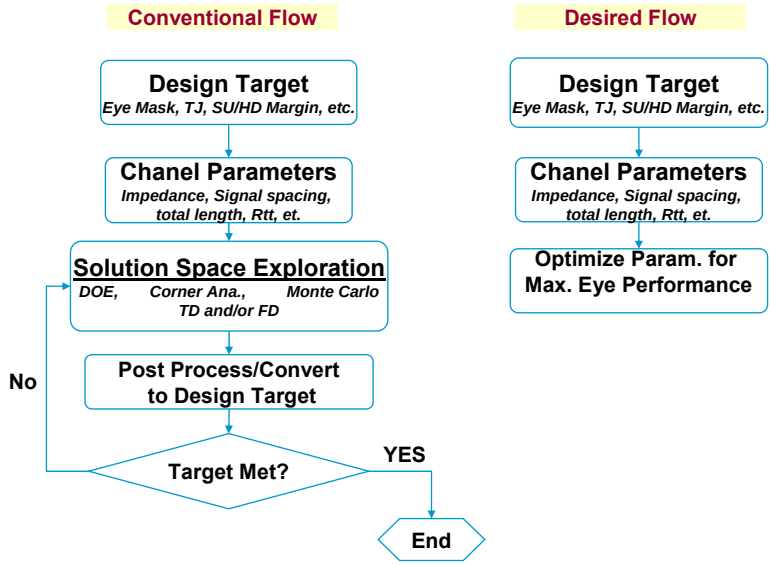
Gap in Channel Design Flow

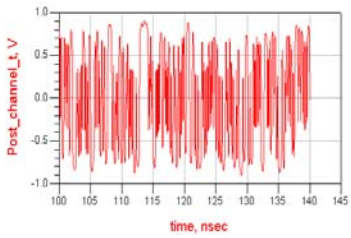


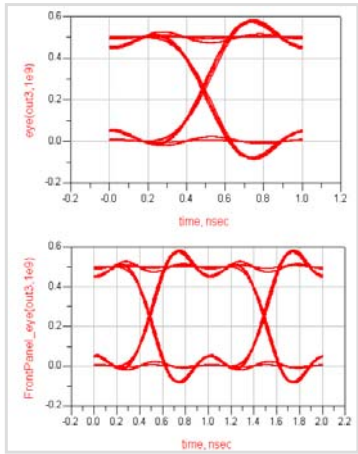
Advantage of Eye Centric Design Flow

- Substantial gain in Channel Design Time (More than 3 weeks in our DDR2 case)
- Design is more robust since channel is optimized toward end to end channel performance
- Reduces risk of marginal design or opportunity loss due to over design

Different Eye Diagrams Functions

Why Eye Diagram is Important?

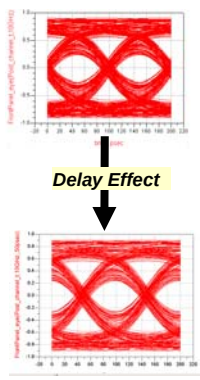




Characterizing an Eye Diagram

Most commonly used eye diagram measurements

- Eye level 1 & level 0
- Eye rise/ fall time
- Eye opening
- Eye width
- Eye height
- Eye amplitude
- Peak to peak & RMS jitter

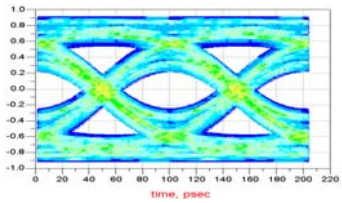


Most of the measurements are statistical in nature

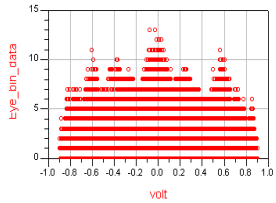
Slice and Dice

Eye Binning

Eye Diagram



Binning Data



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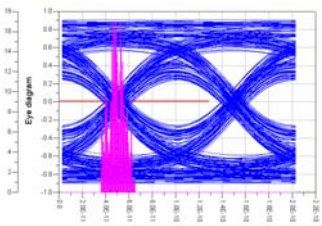
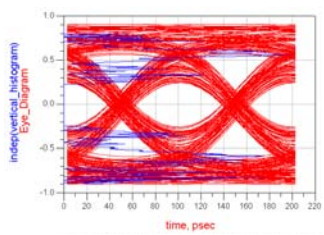
Histogram Plots

Histogram can be created for any portion of eye diagram



Histogram across timing axis provide peak to peak jitter



Histogram across amplitude axis provide distribution around level one and zero

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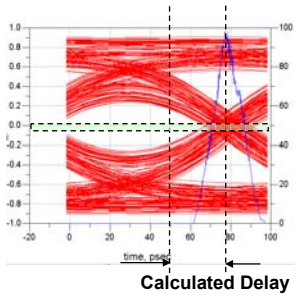
Eye Delay

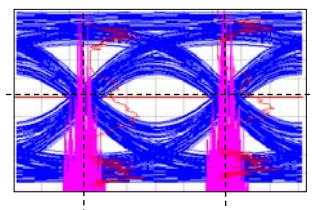
Why delay calculation is required

- Delay calculation is required for automated eye parameter measurements
- Binning the eye diagram makes this calculation easy

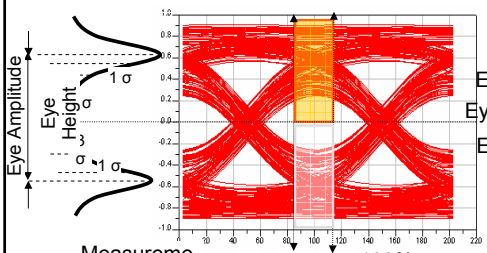


Automated Eye Crossing Detection

- Mean value of horizontal histogram provide crossing time value
- Mean value of amplitude histogram provides crossing amplitude value



Measurements of Eye Level One/Zero



Eye Amplitude = Level One – Level Zero

Eye Height = (Eye level one- 3σ)- (Eye level zero+3

$$\text{Eye S/N} = \frac{\text{(Eye level one-Eye level zero)}}{1\sigma_{\text{level one}} + 1\sigma_{\text{level zero}}}$$

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Eye Measurements

```
MeasEqn
GetEye
sc_single_eye=eye(Diff0,Rate)
sc_get_delay=FrontPanel_eye_delay(Diff0,Rate,"NRZ")
sc_get_eye=eye_binning(FrontPanel_eye(Diff0,Rate,1,sc_get_delay),451,321)
MeasEqn
Levels
sc_get_max_voltage=max(Diff0)
sc_get_min_voltage=min(Diff0)
sc_get_avg_voltage=(sc_get_max_voltage-sc_get_min_voltage)
sc_level_40=0.2*sc_get_avg_voltage
sc_level_60=0.8*sc_get_avg_voltage

MeasEqn
Waveform
sc_amplitude_histogram_data=FrontPanel_eye_amplitude_histogram(sc_get_eye)
sc_waveform_topbase=FrontPanel_wave_topbase(sc_amplitude_histogram_data,"NRZ")
sc_waveform_top=sc_waveform_topbase[0]
sc_waveform_base=sc_waveform_topbase[4]
sc_eye_crossing=FrontPanel_eye_crossings(sc_get_eye,sc_waveform_topbase[7],sc_waveform_topbase[2],"NRZ")
sc_eye_top_base=FrontPanel_eye_topbase(sc_get_eye,sc_eye_crossing,40,60,"NRZ")

MeasEqn
Eye_Measurements
sc_frontpanel_eye=eye_density(FrontPanel_eye(Diff0,Rate,1,sc_get_delay),451,321)
sc_eye_Amplitude=sc_eye_Level_One-sc_eye_Level_Zero
sc_eye_Height=sc_eye_top_base[9]-sc_eye_top_base[8]
sc_eye_Width=FrontPanel_eye_width(sc_get_eye,sc_eye_crossing,Rate)
```


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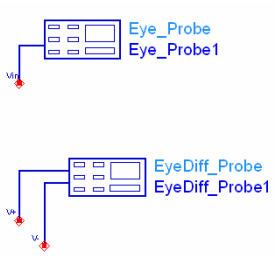
Simplified Eye Measurements

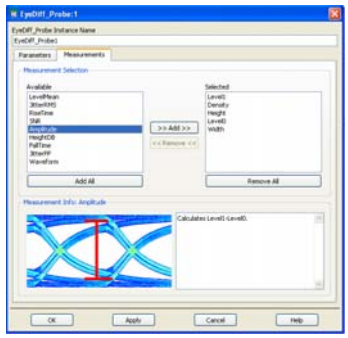
Fast and Easy

Concept of Eye Probe



Any number of Eye probes could be used in a design

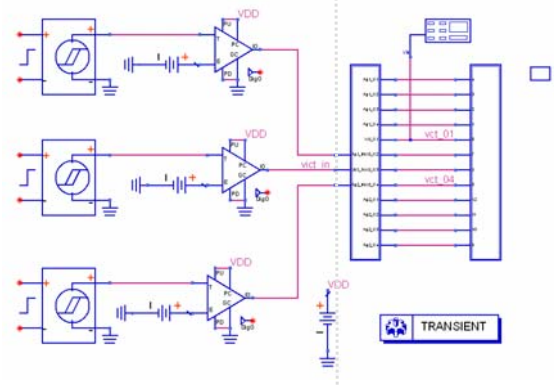
Measurements which needs to be performed



DDR2 Simulation

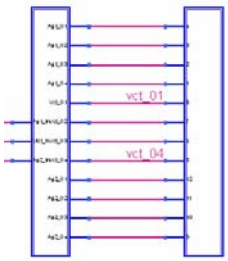
IBIS drivers and triggers

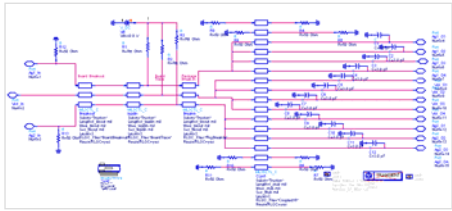
Memory Module & Eye Probe



Memory Bus Simulation Details

- X8 Un-buffered Memory Down Channel
- 8 SDRAM Devices per signal
- Signal Group : CMD/ADD





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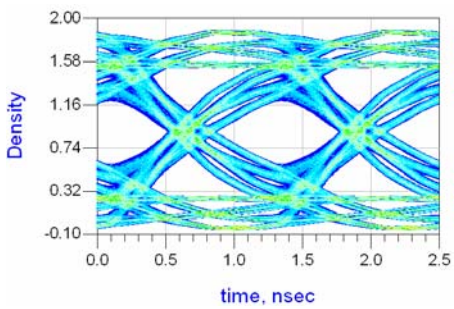
Memory Performance at DRAM



permute(Height)
0.472

permute(Width)
9.050E-10

How to improve channel performance?

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- Introduction to Optimization
- Time domain Optimization and why it is difficult
- Optimization of DDR2 Channel

Introduction to Optimization

Modify your Designs Automatically to Achieve Required Performance

Why Optimization?

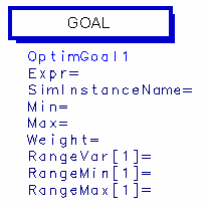
- Parameter sweep often doesn't lead to an optimized designs
- Parameter sweeps requires usually large number of simulation when number of variables are large

The use of Optimizers in a design process

- Automatically change design parameter to meet design goals
- Categorized by their error function formulation
- Coarse design stages: Random optimizer, Random Minimax optimizer and Simulated Annealing optimizer
- Fine design stages: Gradient optimizer, Gradient Minimax optimizer, Quasi-Newton optimizer and Minimax optimizer

Issues with Time Domain Optimization

– Time domain optimization goals are often difficult to define



– Changes in any reactive component during optimization will effect channel delay and optimization goals may no longer be applicable

DDR2 Channel Design

X8 Un-buffered Memory Down Channel

8 SDRAM Devices

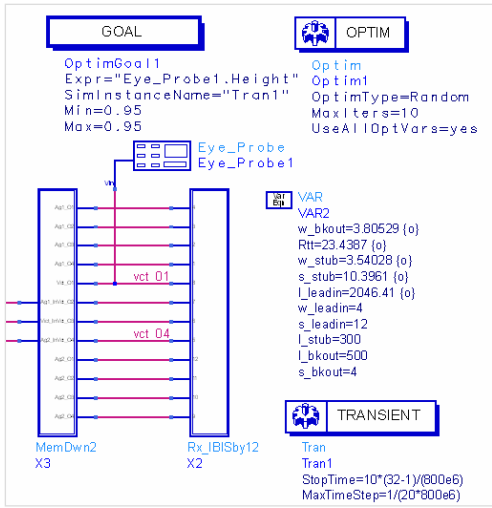
Signal Group to Optimize: CMD/ADD

Design Parameters:

Leadin	Escape	W leadin	S Breakout	Trace Spacing	Rtt	L Brkout
2-4 in	0.3-0.8 in	3.5-5.5 mils	3-5 mils	8-15 mils	20-100 Ω	0.3-0.8in

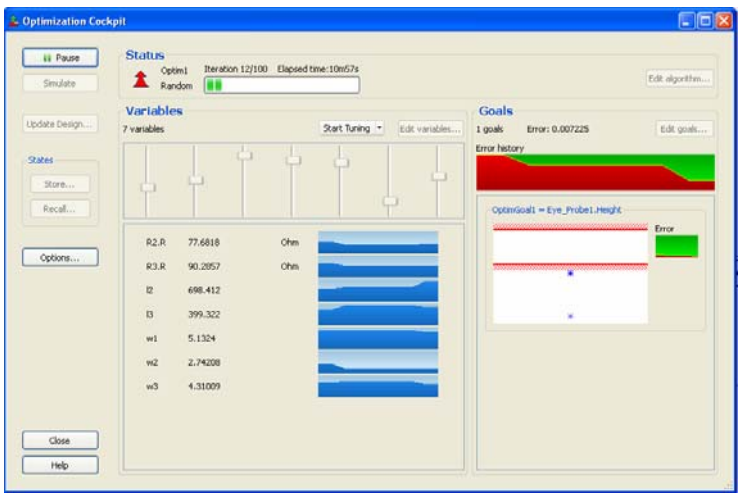
Eye Diagram Optimization

- Which all eye measurements can be optimized
- How many nodes can be optimized simultaneously
- Can optimization be performed easily



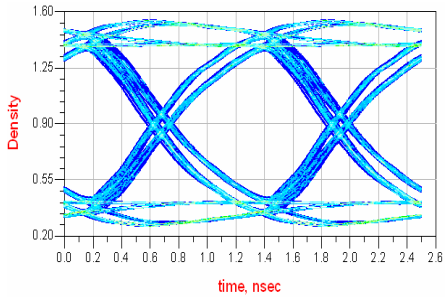
Optimization Cockpit

What are the benefits of such a cockpit?



Optimized Eye Diagram Performance

Eye Diagram after Channel Optimization



Optimizer Type : Random
Number of iteration : 20
Optimization time : 25 minutes

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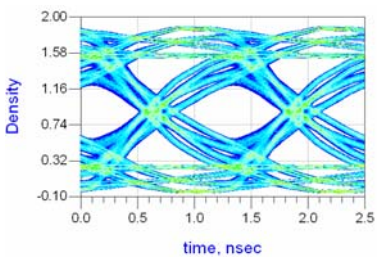
Performance Comparison

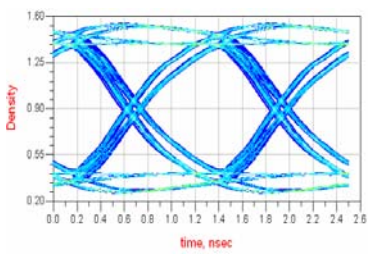
Before



permute(Height)
0.472

permute(Width)
9.050E-10

After



permute(Height)
0.700

permute(Width)
1.078E-9

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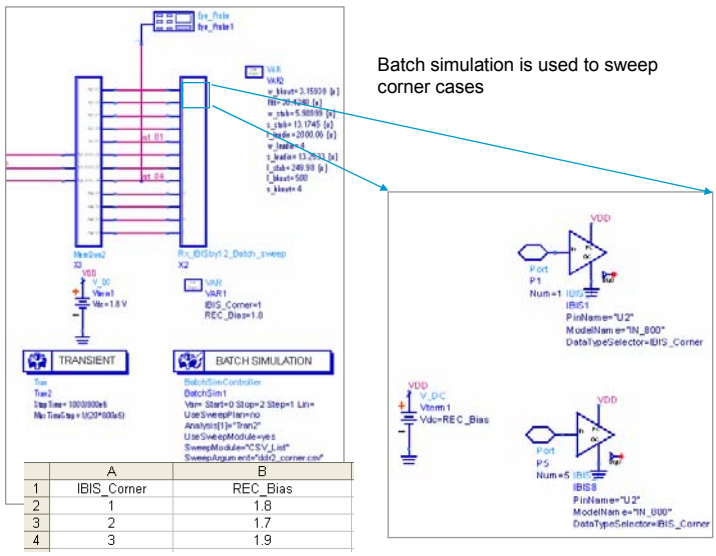
Sweeping Corner Case



	A	B
1	IBIS_Corner	REC_Bias
2	1	1.8
3	2	1.7
4	3	1.9

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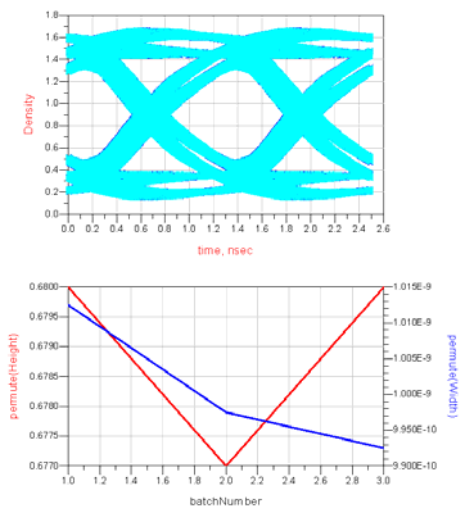
Simulation Results



Here only Rx corner cases was swept.

Batch mode allows simulation of any combination of Tx/Rx corner cases and IBIS models

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Time Domain Optimization Discussed

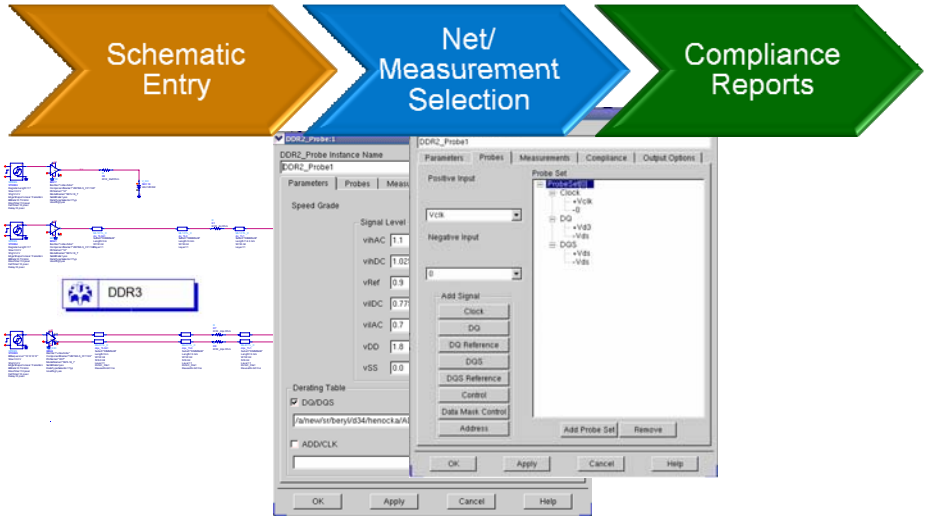
- Works well even if the flight time delay is changed due to change in the reactive element value.
- Automatically calculates delay required for eye positioning
- Automatically detects eye crossing point and 40-60% region
- Optimize eye diagram performance
- Corner case simulation performance was determined

Any eye diagram parameter such as eye opening factor, eye height, peak to peak jitter, rise time … can be used as an optimization goal.

Will make your design work without running 1000's of parameter sweep

DDR Mesurements

Memory Compliance Toolkits



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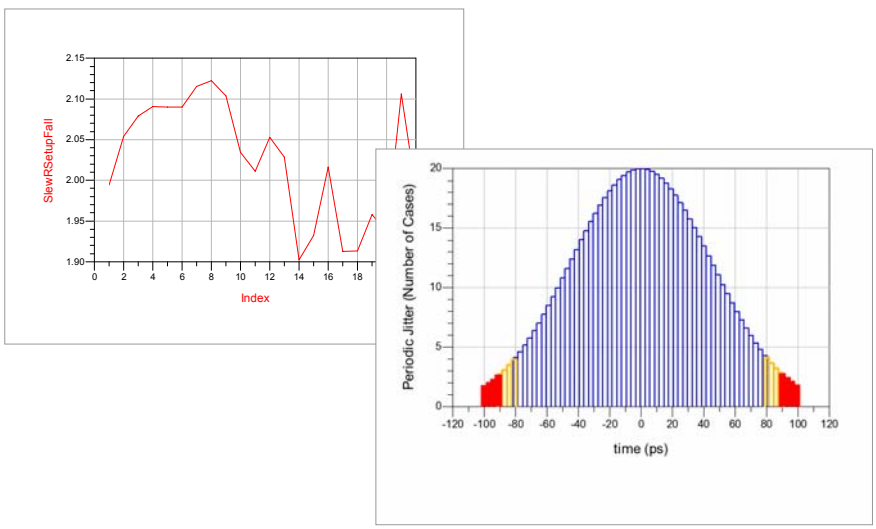
Memory Compliance Toolkits-Features



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Conclusion

- Time Domain optimization of eye diagram provides a powerful methodology to improve high speed memory design and to extract even fraction of the psec of timing margin buried in interconnects
- Substantial reduction in time needed to design and optimize of memory platform design is made (from weeks to hours)
- Guaranteed maximal channel robustness
- Minimize Over/Under design risks

Opportunities for future development

Need to demonstrate IBIS model optimization such as driver strength, ODT etc.

ZTE中兴

Behavioral Model Application in HSS Simulation

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High-Speed System Lab, ZTE Corporation

Talking to the future

Asian IBIS Summit
Shanghai, China
November 4 , 2009

Agenda

- Overview
- Application with IBIS AMI Model
- Application with IBIS AMS Model
- Summary and expectation

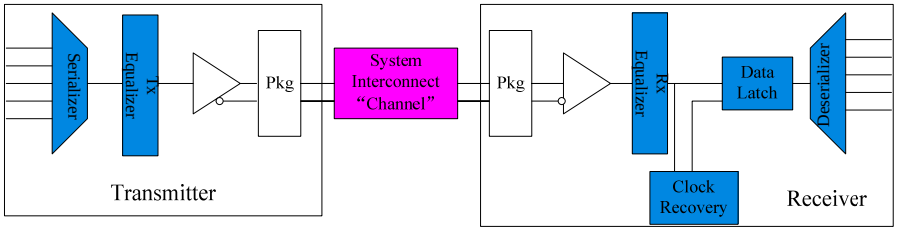
Overview

- The High-Speed Serial (HSS) link Signal Integrity simulation is more important with more uses of Serdes devices.
- Sometimes, the SerDes vendor can't provide the TX&RX spice model for Signal Integrity Simulation for 6Gps+ data rate. Even the models may be provided, the simulation time may be not acceptable.
- SerDes vendor tools always haven't compatibility, so the transceivers must be the same vendor, i.e., the simulation method isn't enough to used for engineering design with different SerDes vendors. Besides, the results is overoptimistic.
- Now, the most effective method to analyze the serial link is through SI and BER test, but it may be too late for finding the questions and the SI test is infeasible.
- For multi-gigabit interconnect system design, the simulation method based on behavioral-level model settles for the simulation time and the precision in engineering compared to other analysis method.

Behavioral-level model

- Use SPICE Model
  - Good accuracy
  - Models are derived from transistor-level netlist and layout
  - Relatively long simulation time and sometimes convergence problems
  - Intellectual property protection concerns
- Use IBIS Model
  - Models are derived from measurements and/or full SPICE model simulations
  - Fast simulation run time
  - Difficult in Modeling complex transceiver buffers, as with Pre-emphasis and Equalizer processing
- Use Macro Model based on IBIS model
  - Fast simulation run time
  - Good accuracy
  - Complex process in Modeling

HSS’ Tx&Rx structure



- SerDes-Serializer/Deserializer
- CDR-clock and data recovery
- Passive channel includes pkg of the IC and PCB interconnect based on Linecard or Backplane

AMI Tx/Rx Model example

```
("hss6_cu08.dml"
 (IbisIOCell
  (ideal_50term_pulldown
   (MacroModel
    (MacroType TDiffIO )
    (NumberOfTerminals 8 )
    (SubCircuits “
```

AMI Tx Model

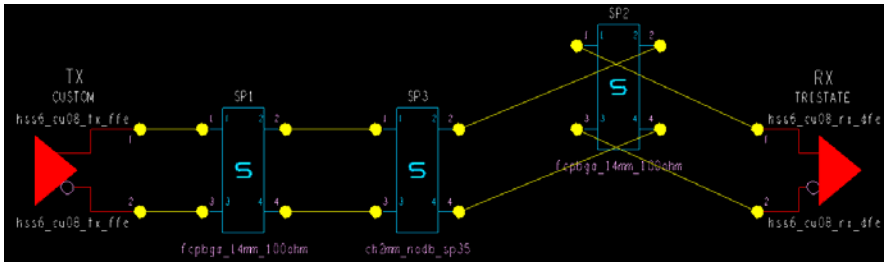
```
(hss6_cu08_tx_ffe
 (ami
  (ibmhsstx_104_win
   (path "D:\\put_in_full_path_to\\dll_lib" )
   (ibis 1 )
   (nffe 4 )
   (rffe 1 )
   (qffe 6 )
   (lffe
    (0.25 1.0 0.5 0.25 ) ) ) )
```

AMI Rx Model

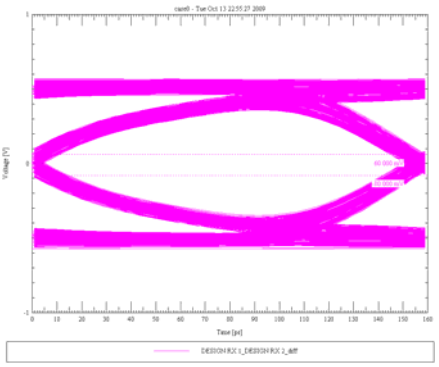
```
(hss6_cu08_rx_dfe
 (ami
  (ibmhssrx_115_win
   (path "D:\\put_in_full_path_to\\dll_lib" )
   (ibis 1 )
   (ndfe 5 )
   (dfelimit
    (0.5 0.25 0.125 0.125 0.125 ) )
   (dfe (0 0 0 0 0 ) )
   (rotlin "../../../../../include_files/pr_ideal.dat" ) ) )
```

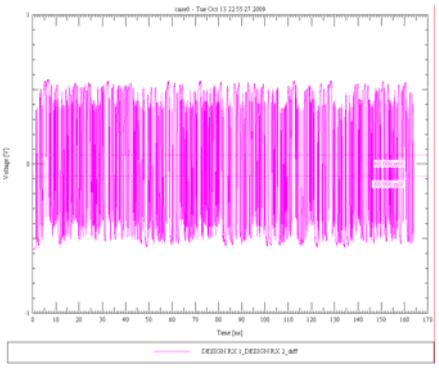
Application with IBIS AMI Model

- The datarate is 6.25Gbps;
- Tx and Rx package models included;
- CDR behavior model embedded in RX model;
- The EDA tool used is Cadence 16.2 SigXplorer;
- IBM AMI model hss6_cu08.dml includes 4-tap Tx FFE, 5-tap Rx DFE;



Simulation results with IBIS AMI Model

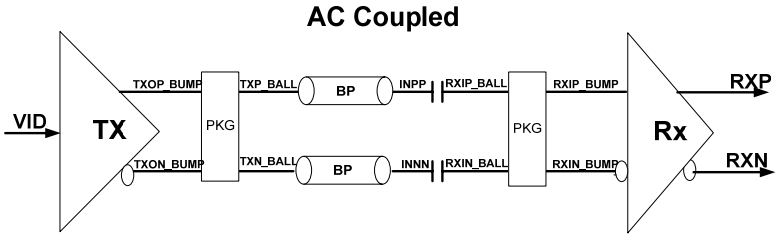




- **Eye-Diagram in IBM AMI Model Simulation**
- **Through tuning the values of DFE and FFE, it is easy to get the good eye-diagram**

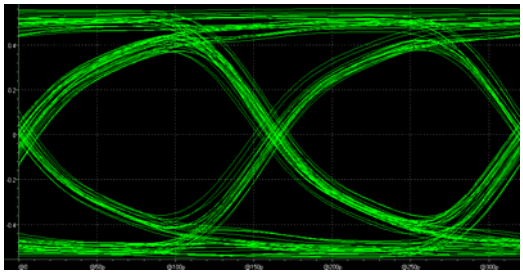
Application with IBIS AMS Model

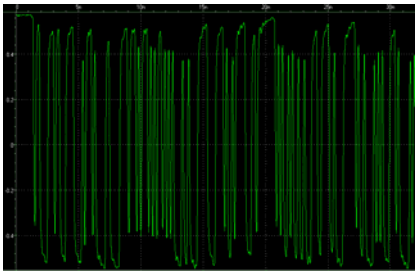
- **IBIS-AMS Modeling:**
  - **The model of transmitters are the Verilog-AMS model;**
  - **The model of receivers are the Verilog-AMS model;**
  - **The following figure shows an example of an Altera TX driver driving an Altera RX receiver through a backplane and AC caps.**



TX drives RX through a backplane and AC caps

Simulation results with IBIS-AMS Model

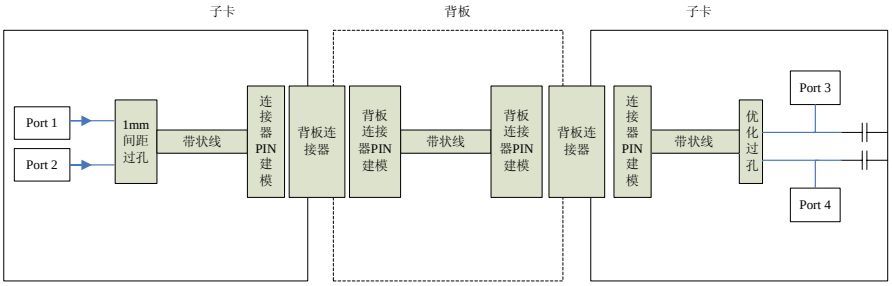




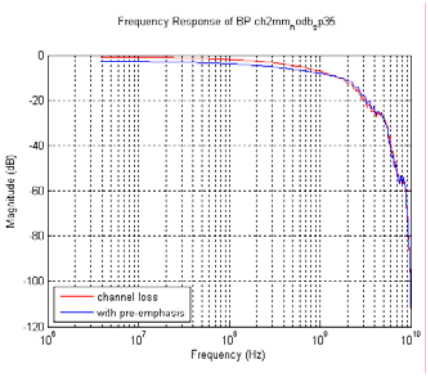
- **Eye-Diagram in Altera AMS Model Simulation**
- **The EDA tool used is Hspice, and 200 bits simulated, the consuming time is more than AMI Model Simulation in Cadence 16.2**

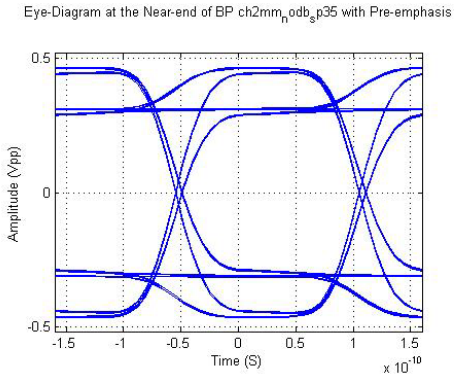
How set coefficients of DFE and FFE

- The S-parameter of the actual serial link channel
- Pre-emphasis and Equalization Link Estimator



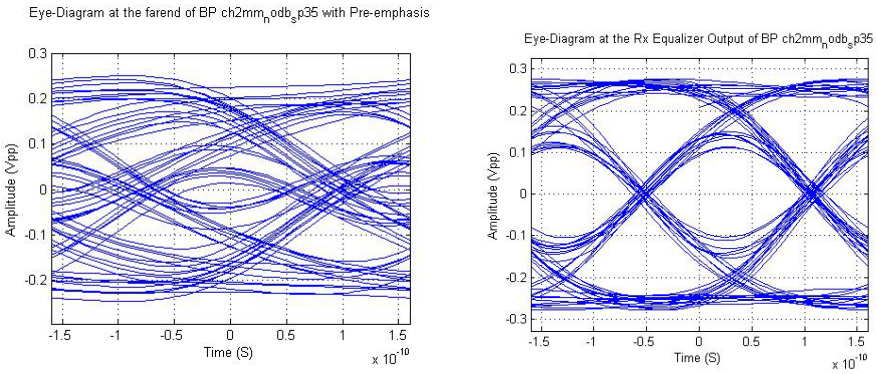
Example for estimating the coefficients of DFE and FFE





- Frequency Response of ch2mm_nodb_sp35
- Eye-Diagram at the Near-end of ch2mm_nodb_sp35 with Pre-emphasis

Example for estimating the coefficients of DFE and FFE (cont.)



- Ch2mm_nodb_sp35 channel Eye-Diagram at the Far-end of Backplane with Pre-emphasis
- Eye-Diagram at the Rx Equalizer Output
- The result with Rx Equalizer is better than no Equalizer

Set the coefficients of DFE and FFE

```
Stratix IV GX Tx pre-emphasis setting is # 4
Pre-emphasis settings are: pre-tap level: -12; post-tap1 level: 0; post-tap2 le
el: 0
Stratix IV GX Rx equalizer setting    is # 4

The horizontal eye-opening is 0.8577 UI
The  vertical  eye-opening is 0.2141 Vpp
Total simulation time is 1.985 min
```

- Quickly and easily narrow the solution space for pre-emphasis and equalization settings for a user defined channel S-parameter model
- Solution of estimating the coefficients of DFE and FFE is efficient
- Getting the open eye-diagram faster than before

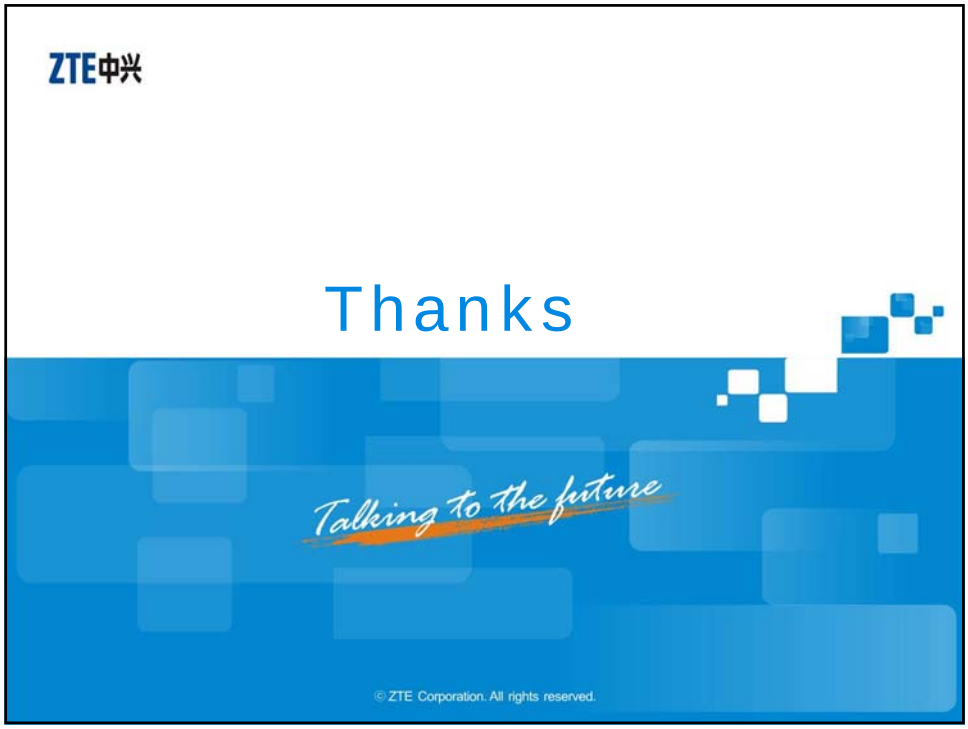
HSS Core Vendor model profile

Core name	HSPICE Model	AMI Model	
		Cadence toolkit	Sisoft toolkit
3Gbps Wirebond	Available	Unvailable	Unvailable
ARM PCI-E	Available	Unvailable	Unvailable
ARM SATA	Available	Unvailable	Unvailable
4Gbps standards	Available	Unvailable	Unvailable
PCI-E Gen2	Available	Unvailable	Unvailable
6Gbps Wirebond	Available	Unvailable	Unvailable
6Gbps	Unvailable	Available	Unvailable
11Gbps	Unvailable	Available	Unvailable

- For the evaluating of the 6Gps+ data rate design, the SerDes vendor can't support the TX&RX spice model, the behavioral-level model may be provided, including AMI, Verilog-AMS model, etc.. But the model source isn't enough now. And expect HSS core vendor put more support to release the behavioral-level model.

Summary and expectation

- Behavioral Model Simulation is an efficient and fast method to evaluate the feasibility of designing the multi-gigabit interconnect system.
- Solution with IBIS AMI model and Verilog-AMS model are available for detailed Hardware system design.
- Pre-emphasis and Equalization Link Estimator by HSS vendor used to set the Emp&Eq is complementary to above detailed design solution, but the results of the eye-margin is overoptimistic.
- The research on the HSS simulation with Behavioral Model will go on deeply from ZTE.
- Expect chip vendor put more efforts on generating more effective and accurate IBIS Model for circuit-level's designer as some features contained in IBISv5.0. And EDA vendor can develop corresponding tool to support the simulation based on the models.
- It is expected by chip vendor and circuit-level's designer that develop a conversion tool that can generate IBIS model of higher version from SPICE model;


ZTE中兴
Thanks
Talking to the future
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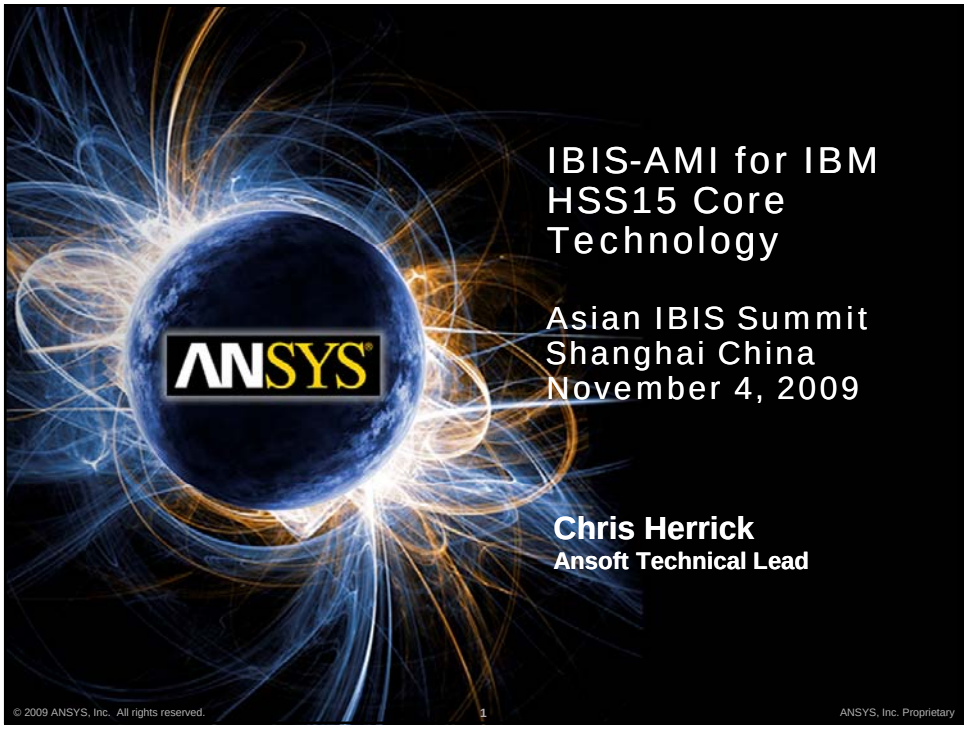


Agenda

- AMI Standards Overview
- AMI Usage
- Design Kit Overview
- HSSCDR Comparison
- Case Studies
- Conclusions

SI Today

- **High Speed Serial channels are pushing the current limits of simulation. Models/Simulator need to handle current challenges**
  - Need to accurately handle very high data rates
  - Simulate large number of bits to achieve low BER
  - Non-linear ,Time Variant Systems
  - TX/RX equalization and vendor specific device settings
  - Specific Data patterns and coding schemes
  - All types of jitter: RJ, DJ, UJ, PJ, etc.
  - XTLK
  - Clock Data Recovery circuits
  - TX and RX may come from different vendors

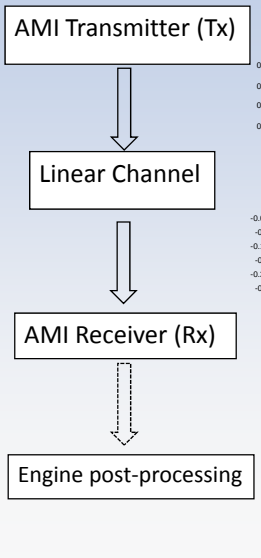
Comparison of Simulations

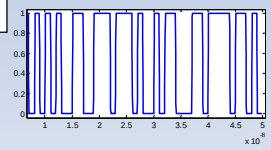
Analysis Method	Advantages	Disadvantages
Traditional IBIS	Fast	Not accurate
Transistor Level	Potentially Accurate Handles Non-Linear	Very Slow No Rx Eq IP Liability Not interoperable
Fast Convolution	Very Fast Handles EQ Includes Bit Patterns	Not Silicon Specific LTI Assumption
Statistical	Very Fast Handles EQ	Not Silicon Specific No Bit Patterns LTI Assumption
IBIS-AMI	Fast Handles Vendor EQ Includes Bit Patterns Not LTI limited	Implementations vary

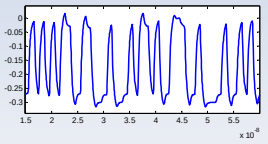
IBIS AMI

- **AMI stands for Algorithmic Modeling Interface**
- **It allows users to specify their own transmitter and receiver models as C-interface compiled libraries**
  - faster signal processing algorithms
  - intellectual property protection
- **Mainly used in convolution transient engines for channel simulation**
  - Designed to be used with fixed time step data
- **Introduced in IBIS 5.0 specs**
  - http://eda.org/pub/ibis/ver5.0/ver5_0.txt
  - IBIS stand for "I/O Buffer Information Specification"; high-level buffer specification for circuit modeling
  - In these specs the library is specified inside the IBIS wrapper and the interface is called IBIS-AMI
  - In fact, AMI concept is independent of IBIS

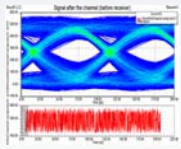
Data flow

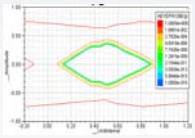


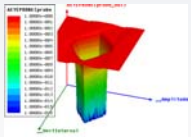




- **Very similar to Fast Convolution**
  - No backward dependency
- **Transmitter and receiver are based on user supplied libraries.**
- **Channel is characterized with impulse response function(s)**
- **All signals are sampled with the constant time step and handled in blocks.**



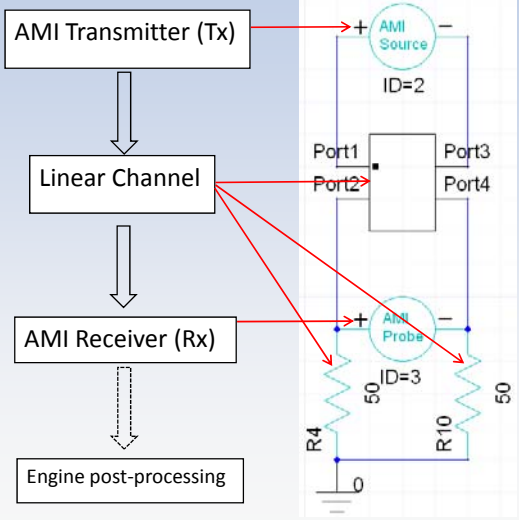




AMI Analysis flow

- **Compute impulse response of the channel (as well of aggressor impulse responses)**
  - Regular transient analysis
- **Initialize AMI libraries with the channel response**
  - Libraries can modify impulse responses
- **In a cycle**
  - Generate a block of transmitted bits
  - Convert a list of bits into a piecewise-linear rise-fall signal
  - Push the signal through the transmitter
  - Convolve the signal with the channel
  - Push the signal through the receiver
  - Post-process the results (eye and bit-error-rate plots)

Simple Circuit Schematic

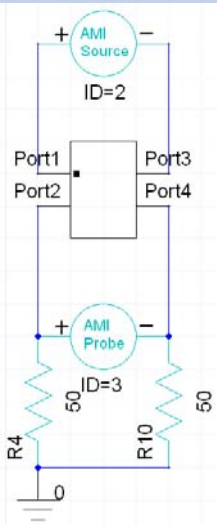


- **Random number generator and jitter added externally to AMI Tx model**
- **In this example, linear channel is represented as 4-port s-parameter block**
- **Additional linear parts of transmitter and receiver are treated as a part of the channel**

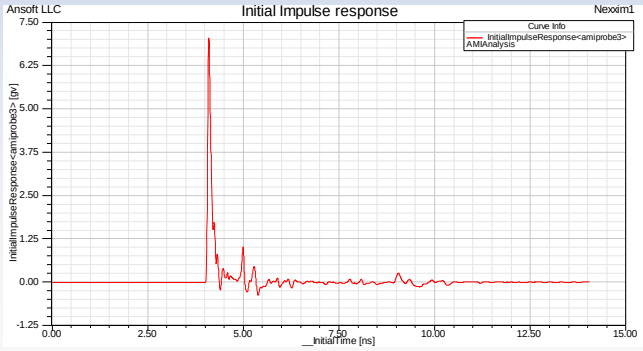
Inside AMI devices

- **AMI libraries define three (optional) functions with C interface**
- **AMI_Init()**
  - Impulse response for channel and aggressors
    - Can modify channel impulse response
  - Bit period (unit interval)
  - Time step
  - Number of aggressors
  - Whatever information user puts in .ami parameters text file
- **AMI_GetWave()**
  - Called for each block of incoming data
  - Input signal (wave) for the channel and aggressors
  - Can generate additional clock tics if the user needs to
- **AMI_Close()**

Generating Impulse Response

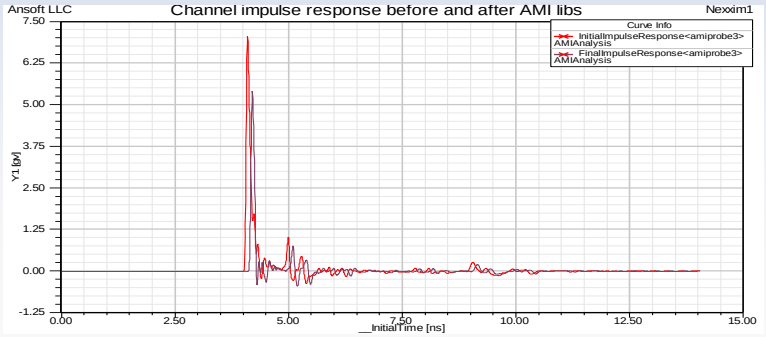


- **AMI source becomes an "impulse source"**
- **AMI probe becomes an empty device**
- **Full-scale transient analysis**
  - All transient options are valid



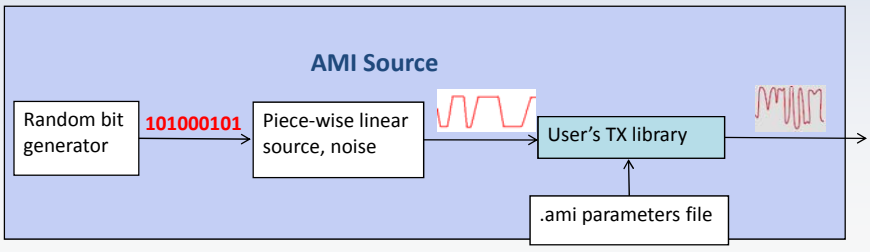
Initializing AMI devices with channel impulse response

- **AMI model receives impulse response and some other parameters**
  - Bit period, time step
  - Whatever text info user keeps in .ami file
  - If there are aggressors, AMI devices have access to their impulse responses too
- **AMI devices can modify the impulse response of the channel**
  - It could be modified on the initialization stage only



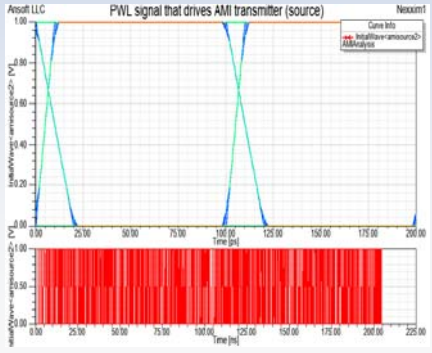
Example AMI Source Structure

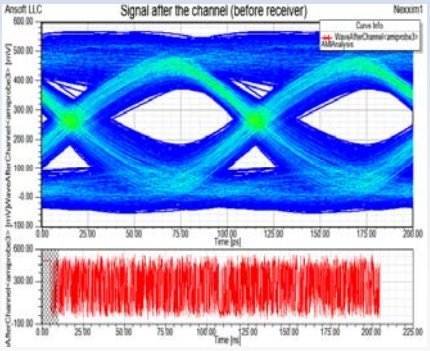
- **AMI source serves as a wrapper for the AMI library**
- **Generate random bit sequence**
  - Unlimited user defined encoding schemes are available
- **Construct piece-wise linear signal**
  - Separate Rise/fall, high/low
  - Several types of noise – DCD, RJ, PJ, UJ
- **Push the signal through the user's transmitter (TX) library**



AMI channel

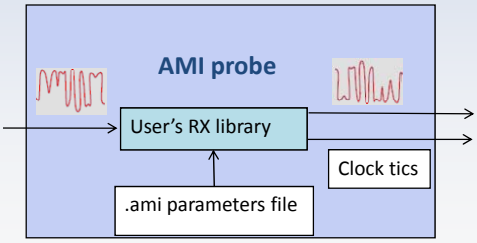
- **Straightforward convolution with the modified impulse response**
  - Engine has to keep history , because the data is handled in blocks
- **Contributions from the aggressors are added linearly**

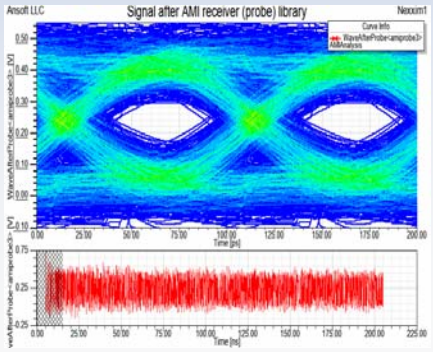




AMI probe structure

- **User's libraries have exactly the same interface as AMI transmitters**
- **User can compute the clock ticks internally and provide it to the simulator for post-processing and plotting**





AMI Challenges

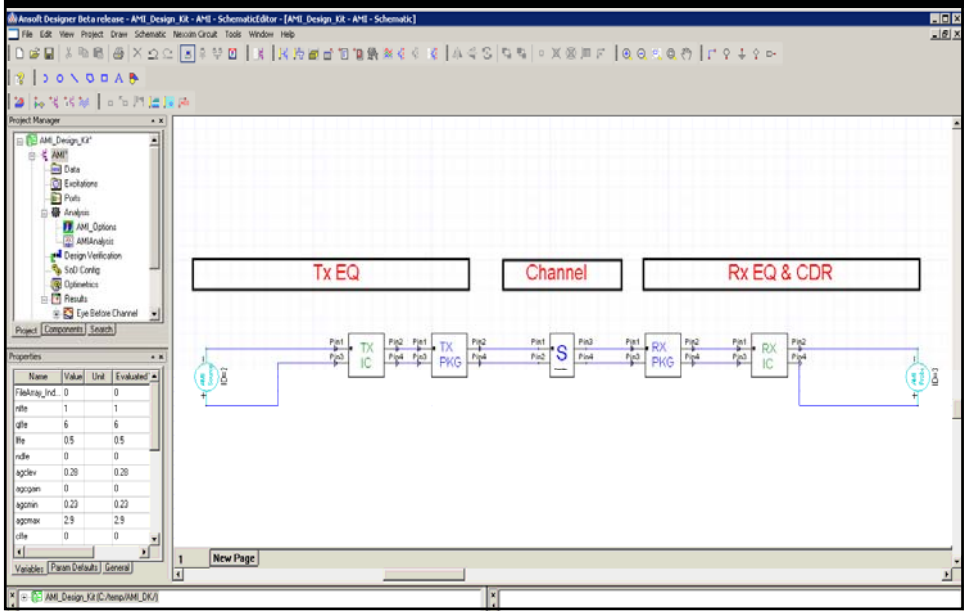
- **AMI models are compiled DLLs and text files**
  - No graphical representation
- **Package model standard not finalized**
  - User needs to manually add IC/package parasitics to channel model
- **Each IC vendor has different parameter set**
  - No standards set
  - Each vendor must document their models
- **No standard way to sweep parameters**
  - Need to create multiple .AMI files
  - EDA tools need to parse arbitrary .AMI parameters

AMI Design Kit Goals

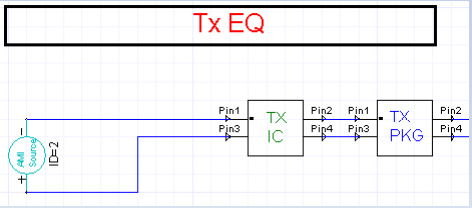
Design Kits provide another level of abstraction outside the AMI standard. They can be used by specific models to compensate for limitations of standardization.

- **Provide a quick start channel simulation**
  - Simply replace channel s-parameters with desired channel
- **Fully parameterized models**
  - Easily sweep variables
  - Bypass different components
- **Link IC and Package parasitics to core AMI models**
  - Automatically reference correct corner cases
- **Fully documented features**
  - All parameters are explained and linked with simulator
- **Common Plots already created**
  - Results automatically plotted

Example Design Kit for IBM Models



Transmitter



TX .AMI File

```
(
(path G:\Projects\AMI_Design_Kit\dll_lib) Full path to libraries
(ibis 1 )                                Specifies IBIS-compliant AP
(nffe _subst_nffe )                      Number of FFE Taps: 1 for n
(cffe _subst_cffe )                      Sets FFE design algorithm c
(qffe _subst_qffe )                      Number of unsigned bits for
(rffe 1 )                                Sets resolution of FFE taps
(lffe 0.25 1.0 0.5 _subst_lffe _subst_lffe _subst_lffe _subst_lffe _s
(ffeout FFE_taps.txt)                    Writes out a file for savin
(cdrstepos 2)                            Select simulation steps per
(vtt 1.5)                                Set VTT for use in VTT depe
(txpow 115)                              Set Tx power register value
(txlev 600)                              Maximum peak level from Tx
)
```

Vendor-specific syntax, official IBIS-AMI syntax has additional required content

AMI source controls data rate, risetime, bit pattern and AMI parameters.

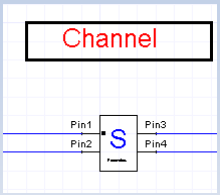
Source may point to different .AMI files and DLL libraries

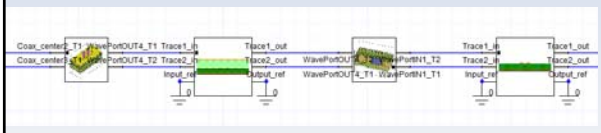
Transmitter generally controls output levels and FFE

Design Kit includes a .AMI file that has been parameterized _subst_ placeholders in the text file

IC and PKG files are selected based on the Driver type and Corner

Channel





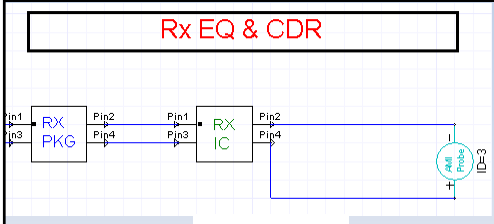
This block is modified by the user to represent his/her channel

Channel may be replaced by any user defined s-parameters

Multiple touchstone files may be swept.

Channel may also contain other spice circuitry or other include files for the transient analysis

Receiver



RX .AMI File

```
(
(path G:\Projects\AMI_Design_Kit\dll_lib) Path to DLL Folder
(ibis 1 )                    Specifies IBIS-Compliant API
(agcmax _subst_agcmax )      Max gain of Rx Variable Gain Amplifier fro
(agcmin _subst_agcmin )      VGA min gain of Rx VGA from 0.1 to 1.0 (de
(agclev _subst_agclev )      Differential target amplitude level (V)
(agcgain _subst_agcgain )    linear gain of Rx VGA:The gain range is fr
(am .015)                    minimum latch overdrive (V)
(dfealg 3 )                  DFE Algorithm:0 = adapt averaged dfe taps
(ndfe _subst_ndfe )          Number of DFE taps
(dfelimit _subst_dfelimit )  DFE coefficient limits: 0= Don't constrair
(cdrsteps 32 )               CDR steps per UI:27 and 32 are the valid s
(cdr 0 )                     CDR algorithm: 0 = cdrver[1] cdrclock[8](c
(cdrclock 8 )                Select CDR clock rate in UI/CDR clock:UI p
(cdrver 4 )                  Select CDR version: 0-255 are valid settir
(cdrstepos 2)                Select simulation steps per phase rotator
(lockwait _subst_lockwait )  Number of bits to wait before applying DFE
(rotlin G:\Projects\AMI_Design_Kit\include\pr_wc_6g4.dat ) rotator linea
(dfeadaptoff 0)              Turns off adaptive DFE
(dfeoff 0)                   Turns off DFE
)
```

AMI probe controls AMI parameters.

Source may point to different .AMI files and DLL libraries

Very similar to AMI Source but generally contains more parameters

Receiver controls DFE and CDR settings

Vendor-specific syntax, official IBIS-AMI syntax has additional required content

IBM HSSCDR

- **The HSSCDR (“High Speed SerDes/Clock Data Recovery”) program is a proprietary MATLAB based system-level signal integrity simulator that supports IBM’s HSS cores.**
- **Current standard for evaluating user channels with IBM ICs.**
- **This is a standalone program that does not integrate with other simulators, requires a single s-parameter block and does not allow IC models from outside vendors**
- **IBM is looking to translate the models into the more flexible IBIS-AMI format.**

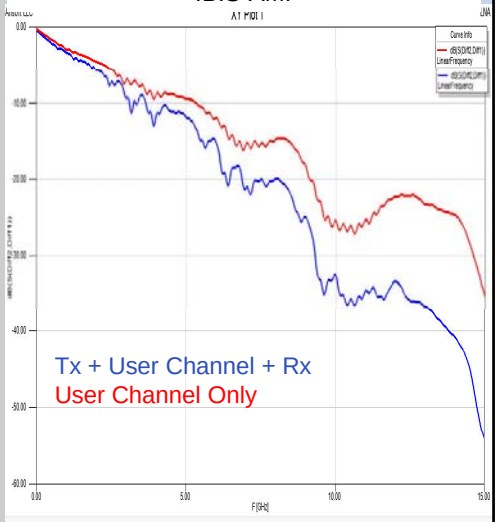
Channel Analysis Settings

- **Used a long channel consisting of two backplanes and a cable**
- **15.6 GB/s**
- **Used HSS15 CU045 technology**
- **Simulated 1 Million Bits – PRBS31**
  - Only plotted 8192 bits for HSSCDR (Maximum Limit)
- **Worst Case PKG and IC parameters**
- **Simulated on x86 Intel Xeon Quad Core 2.4 GHz**

Channel Comparison

HSSCDR

IBIS-AMI

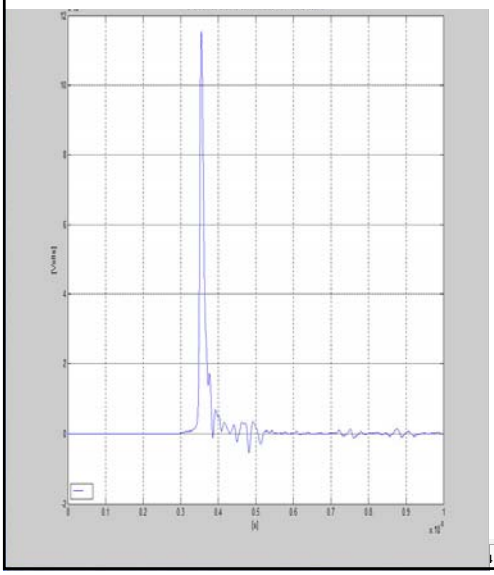


23

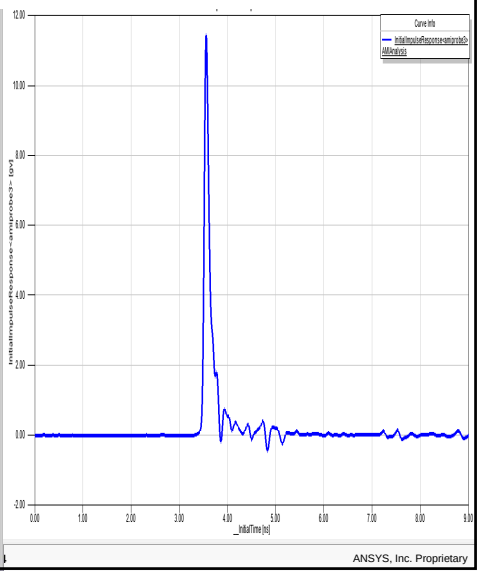
ANSYS, Inc. Proprietary

Impulse Response Comparison

HSSCDR



IBIS-AMI

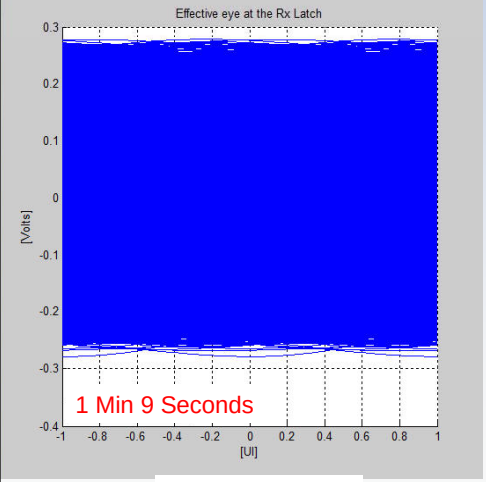


ANSYS, Inc. Proprietary

Full Channel, No FFE, No DFE

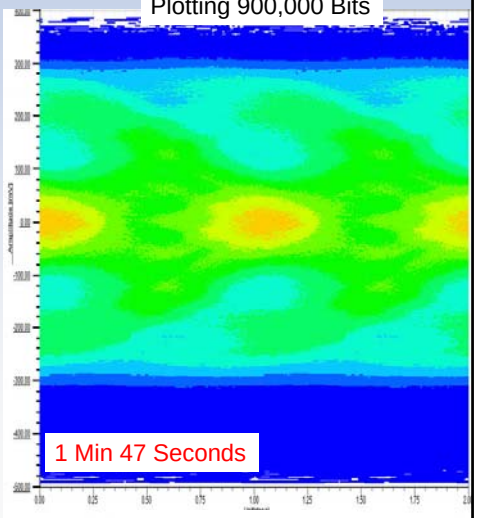
HSSCDR

Plotting 8192 Bits



IBIS-AMI

Plotting 900,000 Bits



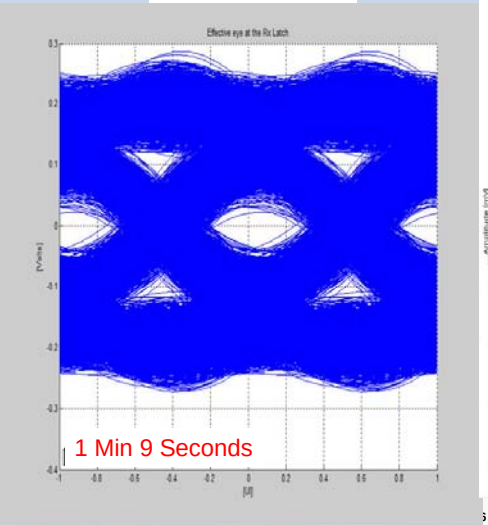
Plotting 8192 Bits

Plotting 900,000 Bits

Full Channel, 3 tap FFE, No DFE

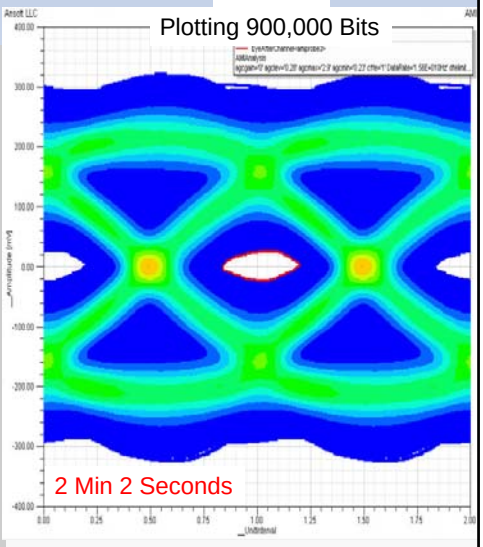
HSSCDR

Plotting 8192 Bits



IBIS-AMI

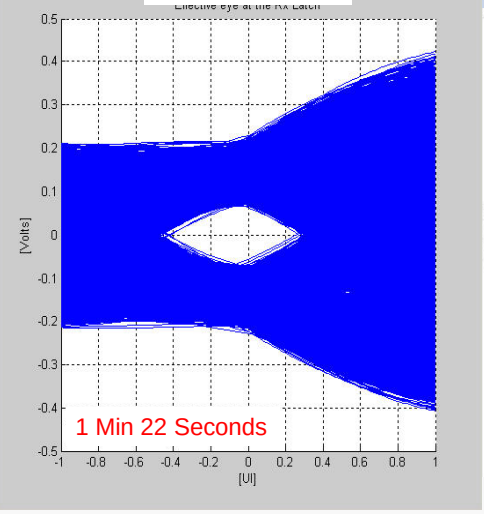
Plotting 900,000 Bits



Full Channel, No FFE, 10 Tap DFE

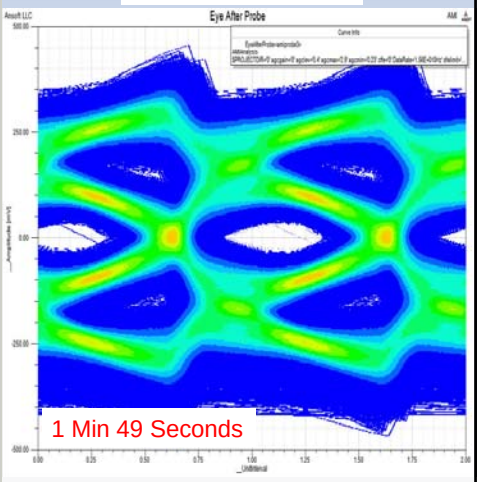
HSSCDR

Plotting 8192 Bits



IBIS-AMI

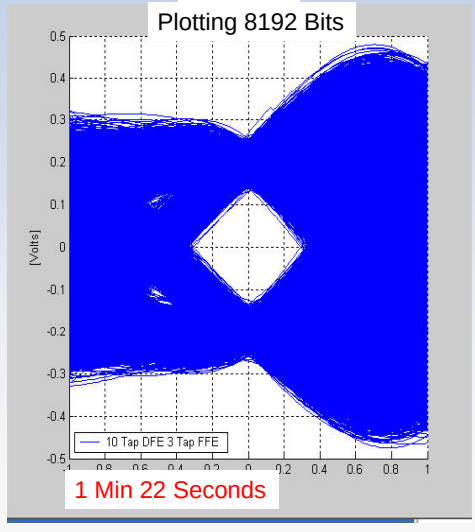
Plotting 900,000 Bits



Full Channel, 3 tap FFE, 10 Tap DFE

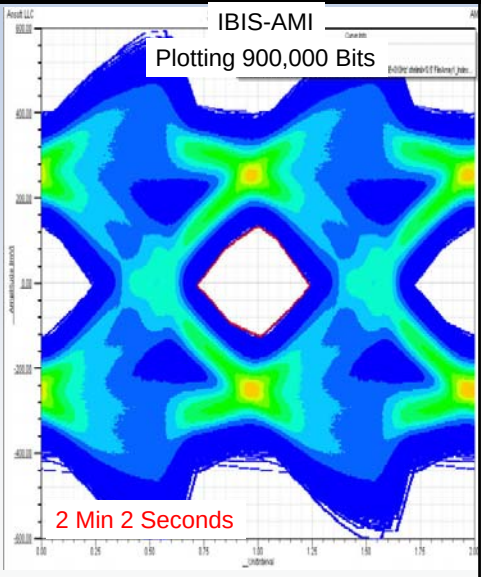
HSSCDR

Plotting 8192 Bits

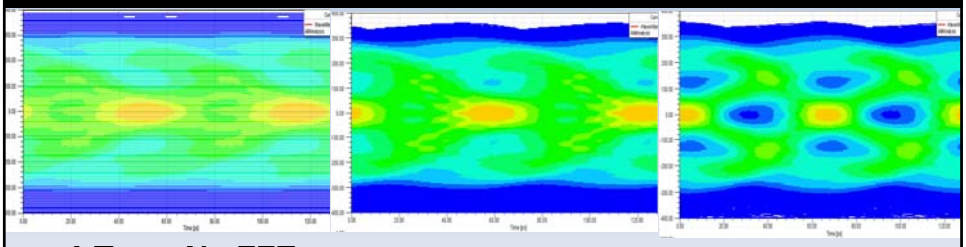


IBIS-AMI

Plotting 900,000 Bits

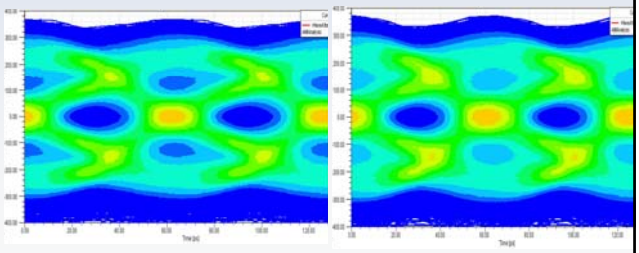


Sweeping FFE



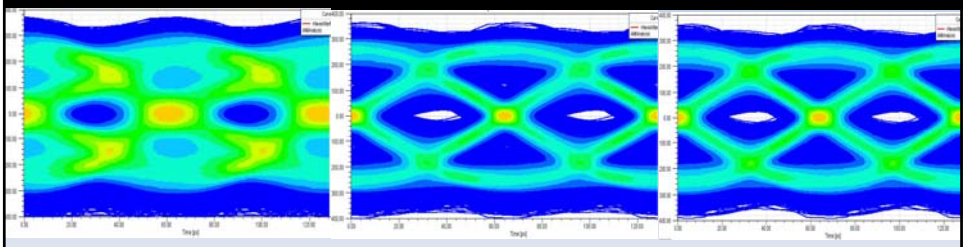
1 Tap = No FFE | **2 Taps** | **3 Taps**

FFE swept from 1 to 5 taps
CFFE = NFFE-1
DFE turned OFF
Data Rate 15.6 GB/s
PRBS31 used
1 Millions bits simulated
Eye Plotted after Rx



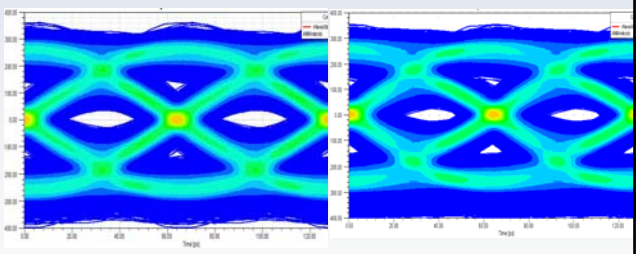
4 Taps | **5 Taps**

Sweeping CFFE (Cursor Lag)



CFFE = 4 | **CFFE = 3** | **CFFE = 2**

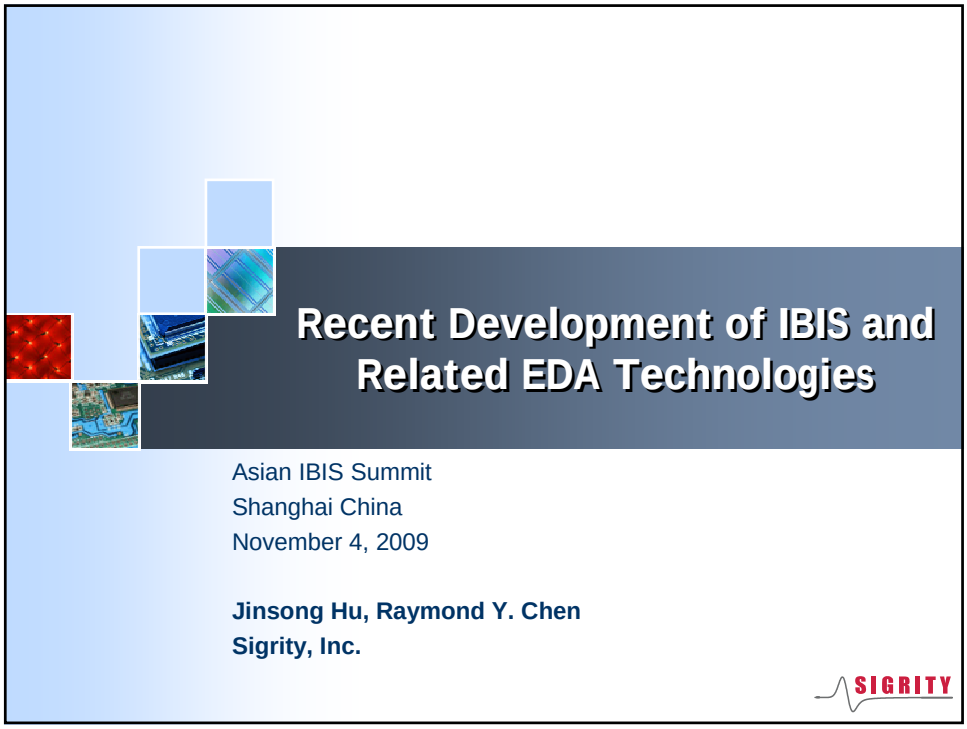
CFFE swept from 4 to 0
NFFE = 5 Taps
DFE turned OFF
Data Rate 15.6 GB/s
PRBS31 used
1 Millions bits simulated
Eye Plotted after Rx

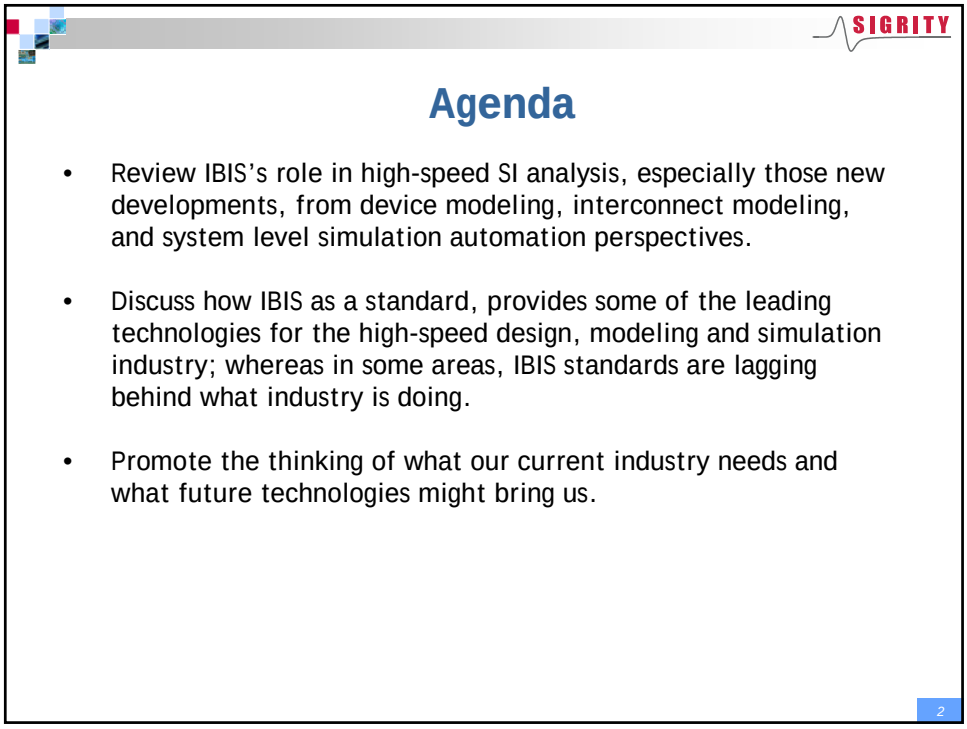


CFFE = 1 | **CFFE = 0**

Conclusions

- **Traditional models used in simulation are no longer feasible for the latest high speed serial designs**
- **IBIS – AMI offers a promising new means of modeling Transmit and Receiver equalization without compromising intellectual property.**
- **AMI Design Kits offers a quick start for successful simulation of IBM's HSS core technology**
- **For questions or additional information, please email Cherrick@ansoft.com**


Recent Development of IBIS and Related EDA Technologies
Asian IBIS Summit
Shanghai China
November 4, 2009
Jinsong Hu, Raymond Y. Chen
Sigrity, Inc.
SIGRITY


SIGRITY
Agenda
• Review IBIS's role in high-speed SI analysis, especially those new developments, from device modeling, interconnect modeling, and system level simulation automation perspectives.
• Discuss how IBIS as a standard, provides some of the leading technologies for the high-speed design, modeling and simulation industry; whereas in some areas, IBIS standards are lagging behind what industry is doing.
• Promote the thinking of what our current industry needs and what future technologies might bring us.
2

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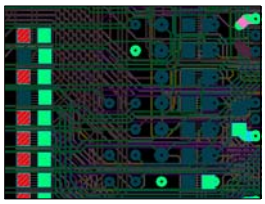
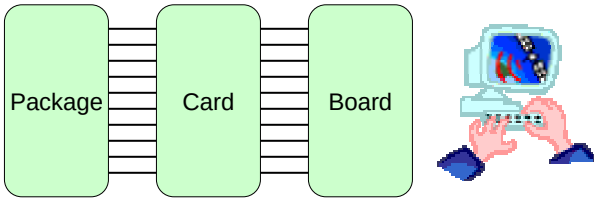
IBIS's Role in High-Speed SI Analysis

Device Modeling



Interconnect Modeling



System Level Simulation Automation

3

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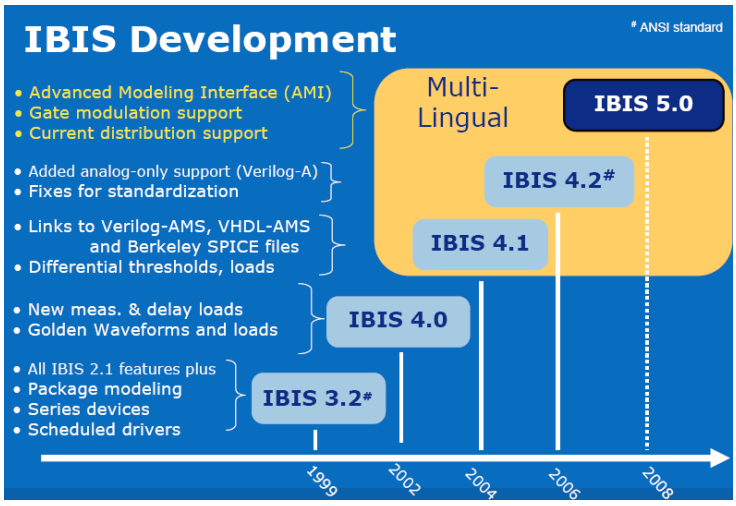
IBIS Evolution



➢ Reference: New Table-based Keywords in IBIS 5.0, Michael Mirmak, 2008 IBIS Summit China

4

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IBIS Latest Status in 2009

- Device modeling enhancement
  - BIRDs for IBIS 5.0
    - BIRD74.6 – EMI Parameters
    - BIRD95.6 – Power Integrity Analysis using IBIS
    - BIRD97.2/98.1 – Gate Modulation Effect
    - BIRD103.1 – [Model Spec] DDR2 Over/Undershoot
    - BIRD104.1 – Algorithmic Modeling API
    - BIRD107.2 – Update to Algorithmic Modeling API
    - BIRD108 – Fixing Algorithmic Modeling API Impulse Matrix Nomenclature
- Interconnect modeling enhancement
  - Touchstone 2.0 completed and released
    - Sparse matrices and node-port matching now under development
    - Parser development about to begin

5

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IBIS Device Modeling – AMI Development

6

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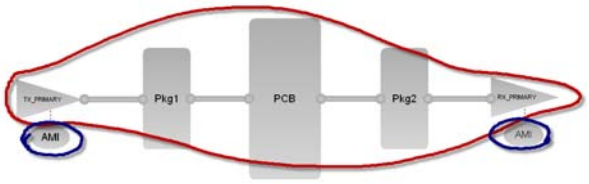
IBIS AMI Device Model Key Concepts

- Device models for high-speed channel simulations that need sophisticated FFE and DFE algorithms
  - The Tx –to– Rx pathway is composed of 3 separate entities Tx algorithmic part, Analog channel, Rx algorithmic part



- Model delivered as a dynamically linked library (DLL)
  - Executable models contain and conceal IC company's advanced device algorithms

7

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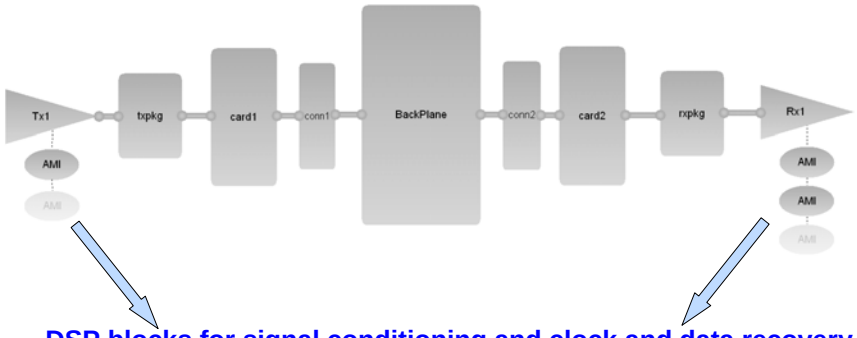
Observations

- IBIS AMI, a novel idea and technical approach that meets current and future modeling and simulation needs, and also fits the business model for IC company (who provides) and system company (who uses)
- IC technology advances fast, which requires more advanced IBIS AMI models beyond current standard to support existing designs
- The provided IBIS AMI models from some IC Companies are just part of the product line, not complete
- Many IC companies are yet to have the practice or know-how to deliver IBIS AMI models

8

SIGRITY

Advanced feature needed - Cascaded AMI



DSP blocks for signal conditioning and clock and data recovery

Cascaded AMI → Allows flexible Modeling and debug
Example: cascade equalizer model with stand alone CDR

9

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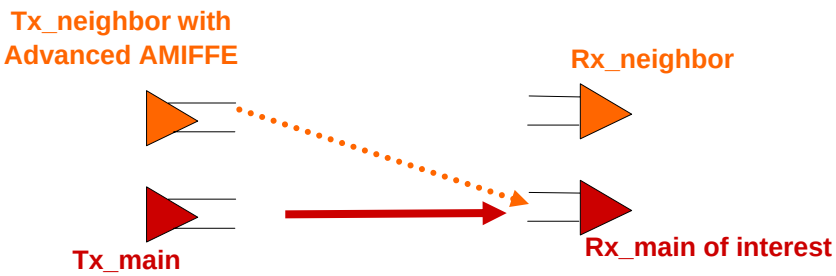
Advanced feature needed: Xtalk aware

- Standard IBIS AMI models are only required to filter the main channel
- Advanced AMIFFE models will optimize the filter coefficients for the main channel, and has the capability to filter the xtalk channel using those coefficients



10

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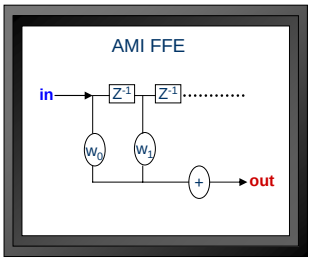
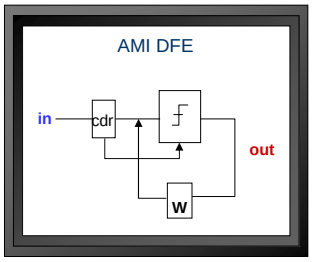
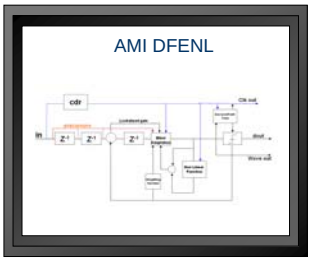
Advanced IBIS AMI Function Blocks

Advanced AMI implementations with highly customizable configurations can model the real world devices

- AMI CDR2 – Stand alone clock data recovery
- AMI FFE – Feed forward filter model (tap optimization)
- AMI CTF – Analog filter model
- AMI DFE – DFE with blind adaption
- AMI DFENL – DFE with look ahead equalizer







11

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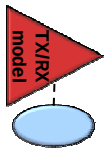
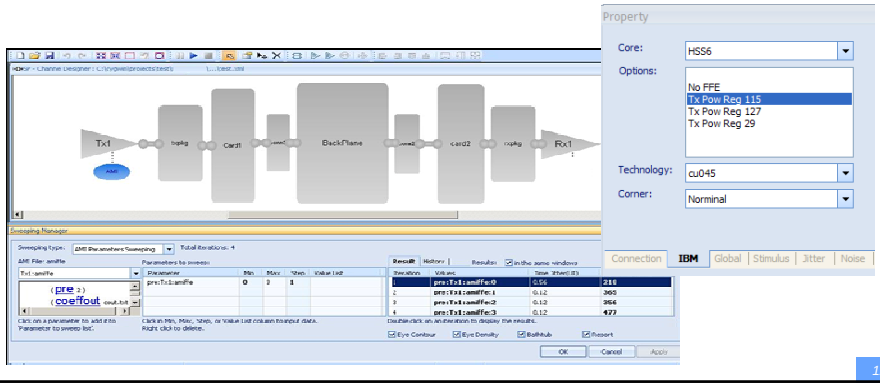
Beyond IBIS AMI - Hybrid Model Support

- **IBIS-AMI**
- **IBIS with driver schedule**
- **HSPICE/Encrypted HSPICE**
- **Verilog-A**
- **IC companies' proprietary models (C or Matlab based), such as those in IBM HSSCDR**

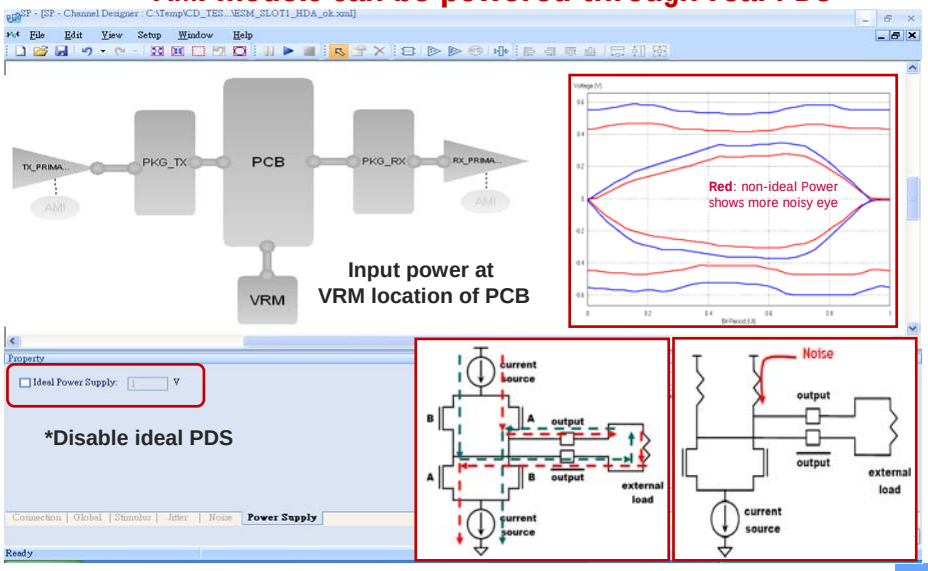




12

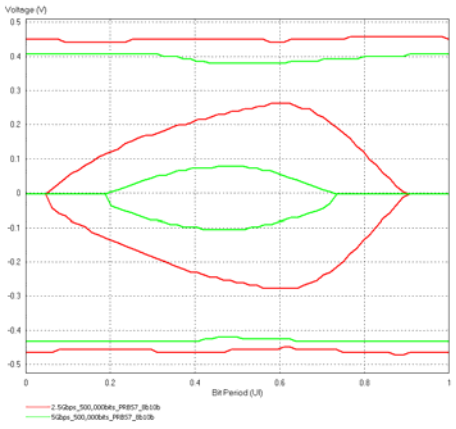
Beyond IBIS AMI – Non-Ideal PDS SI Analysis

AMI models can be powered through real PDS

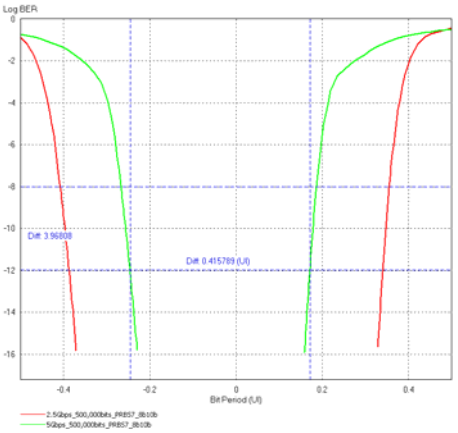


13

High-speed Gigabit Serial Simulation with AMI models (2.5Gbps Vs 5Gbps)



Eye Contour

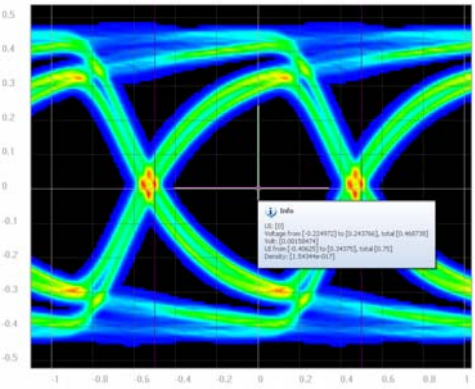


Bathtub

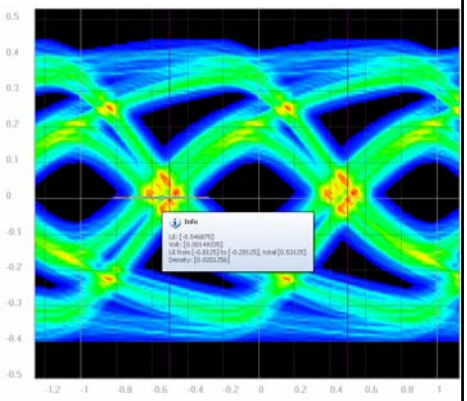
14

SIGRITY

High-speed Gigabit Serial Simulation with AMI models (2.5Gbps Vs 5Gbps)



2.5Gbps Eye Diagram



5Gbps Eye Diagram

15

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IBIS Interconnect Modeling – S Parameters

16

SIGRITY

Package RLC models, EBD and S Parameters

- IBIS **PKG** (IC Package Model) RLC (per pin matrix) is OK for electrical short structures such as IC packages and the frequency response is needed within a few GHz.
  see reference paper at IBIS Shanghai 2006
  http://www.vhdl.org/pub/ibis/summits/oct06a/chitwood.pdf

- IBIS **EBD** (Electrical Board Description) is designed for electrical long structures but the lack of coupling and return path descriptions makes it unsuitable for high-speed SI
  see reference paper at IBIS Shanghai 2008
  http://www.vhdl.org/pub/ibis/summits/nov08a/xu.pdf

- **S-Parameter**
  widely used for accurate high frequency simulation, though has its own issues, is the most popular for interconnect model
  see reference paper at IBIS Shanghai 2008
  http://www.vhdl.org/pub/ibis/summits/nov08a/huang.pdf

17

SIGRITY

IBIS Touchstone ver2.0 for S-Parameters

- Complete backward compatibility with Touchstone 1.0, released in July 2009.

- Mixed-mode support (single ended + diff. signals), which enables SI analysis with the impact of the PDS

- Per-port impedance references. This facilitates power to signal port modeling of coupling and Power Integrity simulation.

- Removal of upper limits on number of data points and number of ports. This facilitates modeling of large ICs.

- Some minor fixes and clarifications. In Touchstone 1.0, Z and Y were normalized with respect to Z0. In Touchstone 2.0, Z and Y are non-normalized and independent of Z0.

  - Reference: http://www.semiconductorsimulation.com/IBIS%20Committee.pdf

18

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Beyond Touchstone 2.0

- For a large S matrix (model for many signal and/or power/ground nets), the Touchstone data file could be huge (few hundreds of MB)
- New format under IBIS task team investigation – Pole/Zero format
  - Extreme compact, only store poles and residues for the rational function approximation
  - Highly efficient simulation, using recursive convolution
  - S-parameter data are stored as vector fitted curve so it is an approximation
- Proprietary format – Sigrity BNP API for S-parameter
  - Very Compact and extremely accurate
  - Do not store tabulated data, provides raw data on demand

19

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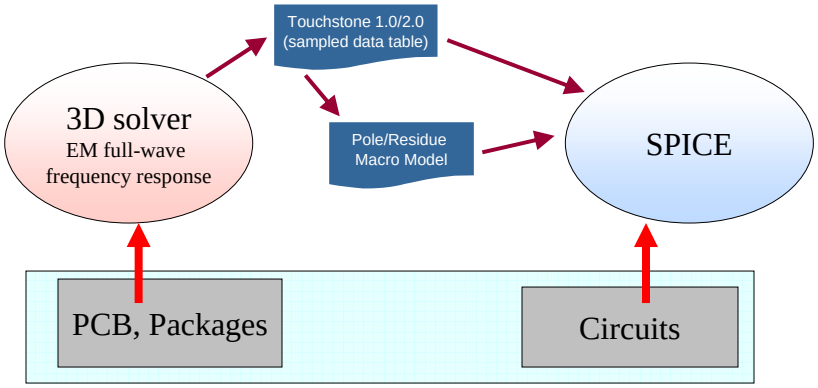
Current Simulation Flow

- Through TouchStone (TS) S-parameter file



20

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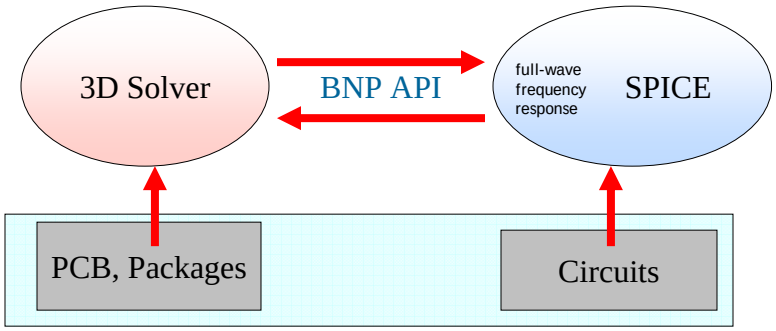
Proprietary Flow for Enhanced Integration

- Frequency domain data exchange through API with broadband response
  - BNP data file does ***not*** store the frequency data points as does in a Touchstone file. It calculates any requested frequency point whenever the API is called within the simulation band. Therefore, the need to interpolate S-parameter tabulated data is completely eliminated. Since the API transports raw data, no pole/zero approximation needed.



21

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S-Parameter Usage Example

Using S-Parameter in both TouchStone and BNP formats in HSPICE

.model Smodel_name S TSTONEfile=file or BNPfile=file

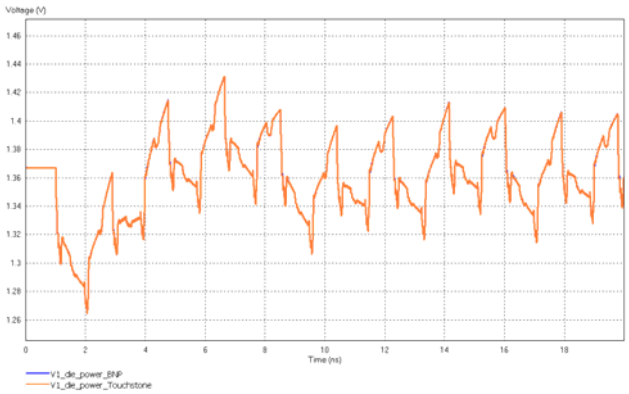
TS file: xyz.snp BNP file: xyz.bnp

BNP file is much smaller than TS file, but yields higher simulation accuracy and convergence

Test Case	Freq #	Touchstone File	Touchstone File Zipped	BNP File
psi_pkg_wb_pre-layout.spd (example folder)	646	1,388 KB	406 KB	24 KB
mixed_extraction.spd (advanced training)	886	10,211 KB	2,771 KB	62 KB
mixed_extraction.spd (all nets enabled)	886	311,105 KB	116,306 KB	1,920 KB

22

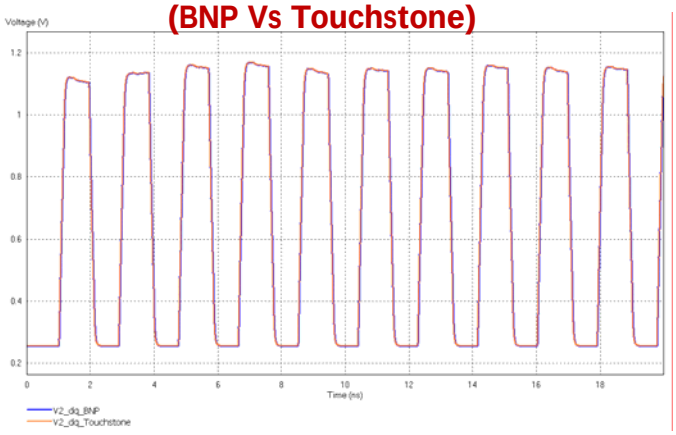
High-speed 1066Mbps Source Synchronous Simulation (BNP Vs Touchstone)



- VCC Power @ Die waveform with BNP Vs Touchstone model
- BNP model simulation has higher efficiency, better convergence and accuracy

23

High-speed 1066Mbps Source Synchronous Simulation (BNP Vs Touchstone)



- DQ @ Board waveform with BNP Vs Touchstone model
- BNP model simulation has higher efficiency, better convergence and accuracy

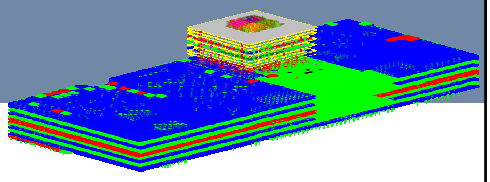
24

Summary

- Reviewed IBIS device model - AMI and its support
- Reviewed S-parameter as the interconnect model, introduced IBIS Touchstone 2.0 and Sigrity BNP
- Next review will be on how device models and interconnect models are connected for system level simulation automation.

25

Thank You!



26

Sparse Matrix Mapping in Future Touchstone 2.1

Bob Ross
Asian IBIS Summit
Shanghai China
November 4, 2009
bob@teraspeed.com

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Topics

- Brief Touchstone background through Version 2.0
- [Sparse Matrix Mapping] for Touchstone Version 2.1
  - Physical symmetry
  - Coincidentally identically data
  - Extrapolate to more ports based on physical symmetry

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Touchstone Background and Update

- Touchstone issued 1984 by EEsof
  - Now part of Agilent Technologies
- Touchstone "Version 1.0" is widely used
- Touchstone Version 2.0 ratified by IBIS April 2009
  - Format rules relaxed
  - Resistance per port option for PDS
  - Mixed mode features for differential setups
  - http://www.eda.org/pub/ibis/touchstone_version2.0/
- Agilent Technologies contracted to produce tschk2 parser – available soon, free

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Version "1.0" Block Arrangement

Option Line
For example, # GHZ S MA R 50

N-port Data Block
(rigid format rules)

Officially for Single-Ended Data

Optional Noise Data Block
(n=2 only)

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"Version 1.0" Fixed Format Examples (f = frequency, s = data-pair)

S1P
f s
f s
f s
f …

S2P
f s s s s
f s s s s
f s s s s
f …

S3P
f s s s
s s s
s s s
f s s s
s s s
s s s
f …

S4P
f s s s s
s s s s
s s s s
s s s s
f s s s s
s s s s
s s s s
s s s s
f …

S5P
f s s s s
s
s s s s
s
s s s s
s
s s s s
s
s s s s
s
f …

S6P
f s s s s
s s
s s s s
s s
s s s s
s s
s s s s
s s
s s s s
s s
s s s s
s s
f …

Etc …

Formatting, frequency ordering, and end of file implies number of ports and frequency values.

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Touchstone Version 2.0 Thirteen IBIS-like Keywords -1

- Comments – starting with '!'
  - Start of line or in line until end of line
  - Within file or before [Version] or after [End]
  - Blank lines permitted
- Required keywords (and option line) – fixed order
  - **[Version]** 2.0
  - # (option line)
  - **[Number of Ports]** <n>

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Touchstone Version 2.0
Thirteen IBIS-like Keywords -2

- Keywords in any order
  - **[Number of Frequencies]** <nf>
    - (required)
  - **[Two-Port Data Order]** {21_12 | 12_21}
    - (required for n=2 only)
  - **[Reference]** <n reference resistances in port order>
  - **[Matrix Format]** {Full | Lower | Upper}
  - **[Mixed-Mode Order]** {Di,j, Ci,j, Si,j entries}
  - **[Number of Noise Frequencies]** <nnf>
    - (required if noise data, n=2 only)
  - **[Begin Information]/[End Information]**
    - (block reserved for future use)

Touchstone Version 2.0
Thirteen IBIS-like Keywords - 3

- Data block keywords
  - **[Network Data]**
    - (required to begin network data)
  - **[Noise Data]**
    - (required if noise data exists)
  - **[End]**
    - (required at end of data)

Version 2.0 Block Arrangement

[Version] 2.0
Option Line
[Number of Ports] <n>
plus keywords as needed

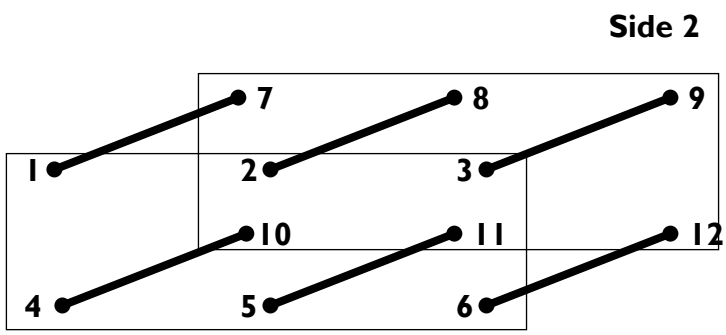
[Network Data]

More flexible formatted data

[Noise Data]
(optional for n=2 only)

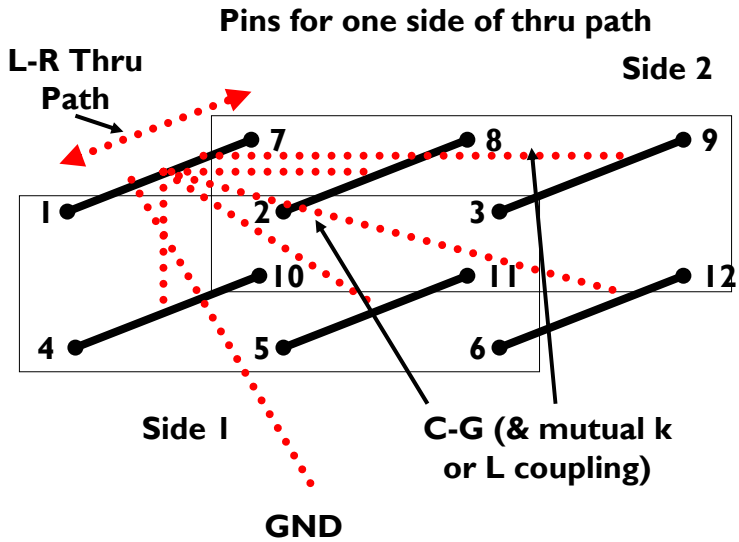
[End]

Example: PhysicallySymmetrical 2 by 3 Connector for Expansion



.pkg, .icm format
illustrated next

[Define Package Model] 6-pin LRC(G) from 1 to 6 and Thru Path 1-7



6 pins in [Define Package Model] Sparse_matrix: list of R, L, C …

[Capacitance Matrix] Sparse_matrix
[Row] 1
1 6pF
2 -1pF
3 -1pF
4 -1pF
5 -1pF
6 -1pF
[Row] 2 | etc … through [Row] 6
2 6pF
3 -1pF

Etc.

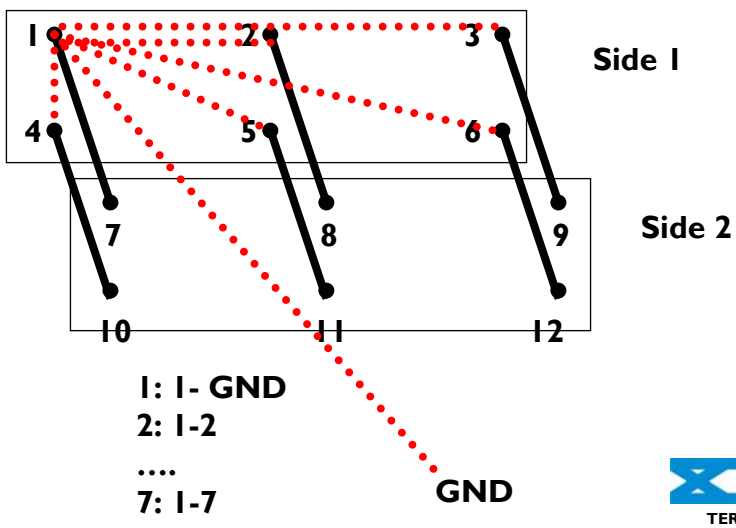
Common Format for .pkg and .icm for large package (e.g., 500 to 1000 pins)

Upper triangle (forward coupling) of single-frequency LRC(G) elements

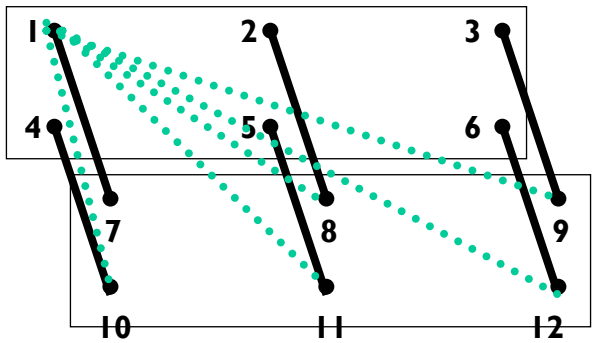
[Sparse Matrix Mapping] Proposed in Version 2.1

- Before [Network Data]
  - **[Number of Sparse Labels]** <nl>
  - **[Sparse Matrix Mapping]** {integer-labels, index-pairs}
    - After **[Matrix Format],** if entered
    - Each integer-label locates a data-pair that can be mapped into one or more index-pair (row,column) positions in the N-port
- Data block keywords
  - **[Network Data]**
    - One data-pair column for each integer-label
  - **[End]**
- Fewer data-pairs under [Network Data]
  - Other keywords have same meaning

12-port Coupling (1: to 7:) Physical Symmetry, Unique Coupling



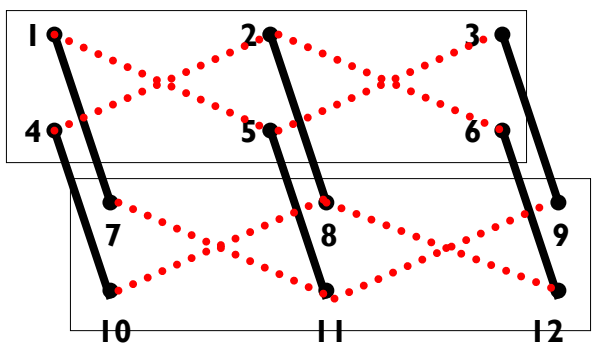
12-port Coupling (8: to 12:) Physical Symmetry, Unique Coupling



8: 1 – 8
9: 1 – 9
....
12: 1 - 12

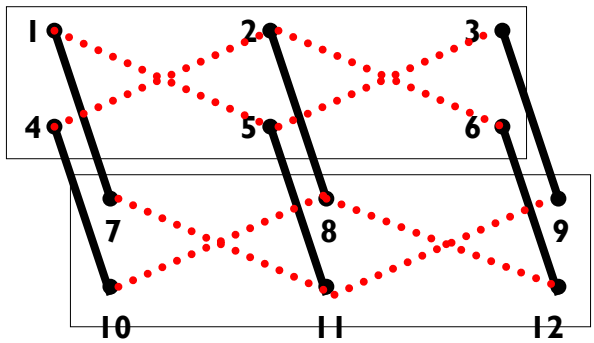
GND

Integer-label '5:' 16 'index-pairs' to map to (row,column) of N-port



5: (1,5) (5,1) (2,4) (4,2) (2,6) (6,2) (3,5) (5,3)
(7,11) (11,7) (8,10) (10,8) (8,12) (12,8) (9,11) (11,9)

[Matrix Format] {Full | Upper | Lower} ('index-pairs')



Upper

5: (1,5) (2,4) (2,6) (3,5) (7,11) (8,10) (8,12) (9,11)

(5,1) (4,2) (6,2) (5,3) (11,7) (10,8) (12,8) (11,9)

Full

Lower

2 by 3 Connector with 7 integer -labels and 7 data-pairs per Frequency

....

[Number of Ports] 12 ! Some keywords omitted

[Number of Sparse Labels] 7

[Matrix Format] Upper

[Sparse Matrix Mapping]

1: (1,1) (2,2) (3,3) (4,4) (5,5) (6,6) (7,7) (8,8) (9,9) (10,10) (11,11) (12,12)

2: (1,2) (2,3) (4,5) (5,6) (7,8) (8,9) (10,11) (11,12)

3: (1,3) (4,6) (7,9) (10,12) 4: (1,4) (2,5) (3,6) (7,10) (8,11) (9,12)

5: (1,5) (2,4) (2,6) (3,5) (7,11) (8,10) (8,12) (9,11)

6: (1,6) (3,4) (7,12) (9,10) 7: (1,7) (2,8) (3,9) (4,10) (5,11) (6,12)

[Network Data] ! Frequency and 7 data-pairs in MA format

<f1> <M1 A1> <M2 A2> <M3 A3> <M4 A4> <M5 A5> <M6 A6> <M7 A7>

[End]

6 Pin (12 Port) 2 by 3 Connector, Number of index-pairs per integer-label

[Matrix Format]	Upper or Lower		Full	
integer-labels	1: to 7:	1: to 12:	1: to 7:	1: to 12:
1:	12	12	12	12
2:	8	8	16	16
3:	4	4	8	8
4:	6	6	12	12
5:	8	8	16	16
6:	4	4	8	8
7:	6	6	12	12
8:		8		16
9:		4		8
10:		6		12
11:		8		16
12:		4		8
		[Sparse Matrix Mapping]		
index-pairs	48	78	84	144
(omitted)	30	0	60	0
		[Network Data]		
data-pairs	7	12	7	12
(available)	78	78	144	144

40 Pin (80 Port) 2 by 20 Connector

[Matrix Format]	Upper or Lower		Full	
integer-labels	1: to 7:	1: to 12:	1: to 7:	1: to 12:
1:	80	80	80	80
2:	76	76	152	152
3:	72	72	144	144
4:	40	40	80	80
5:	76	76	152	152
6:	72	72	144	144
7:	40	40	80	80
8:		76		152
9:		72		144
10:		40		80
11:		76		152
12:		72		144
		[Sparse Matrix Mapping]		
index-pairs	456	792	832	1504
(omitted)	2784	2448	5568	4896
		[Network Data]		
data-pairs	7	12	7	12
(available)	3240	3240	6400	6400

200 Pin (400 Port) 2 by 100 Connector

[Matrix Format]	Upper or Lower		Full	
integer-labels	1: to 7:	1: to 12:	1: to 7:	1: to 12:
1:	400	400	400	400
2:	396	396	792	792
3:	392	392	784	784
4:	200	200	400	400
5:	396	396	792	792
6:	392	392	784	784
7:	200	200	400	400
8:		396		792
9:		392		784
10:		200		400
11:		396		792
12:		392		784
		[Sparse Matrix Mapping]		
index-pairs	2376	4152	4352	7904
(omitted)	77824	76048	155648	152096
		[Network Data]		
data-pairs	7	12	7	12
(available)	80200	80200	160000	160000

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Connector: 5 banks of 2 by 20 pins [Matrix Format] Upper, 1: to 7:

200 pins, banks of 40 pins each

- 456 index-pairs per 40 pin bank
- 2280 index-pairs for 5 banks
  - About 5 pages of auto-generated index-pairs
  - Not needed – 13,920 index-pairs for zeroed data-pairs
- 7 data-pairs, 7 integer-labels for 200 pins, 400 ports
- Fewer data-pairs than a full 3-port !!

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Comments

- Format details still being discussed
- Port numbering shown in example was for simplicity
  - Any port ordering can be used
  - Some port orders simplify the expansion equations
- [Sparse Matrix Mapping] implies pre-processing step to move data into the full N-port
  - All other keywords apply to the N-port data
  - [Mixed-Mode Order] can also be used to re-order the ports

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Future [Sparse Matrix Mapping]

- Small files for large, physically symmetrical packages and connectors
- Advantages of N-port parameters
  - Many frequencies
  - More coupling modes and generality
  - One mapping for all frequencies
- Supports large packages with N-ports where the IBIS .pkg and .icm format is currently used
- For futureTouchstone Version 2.1

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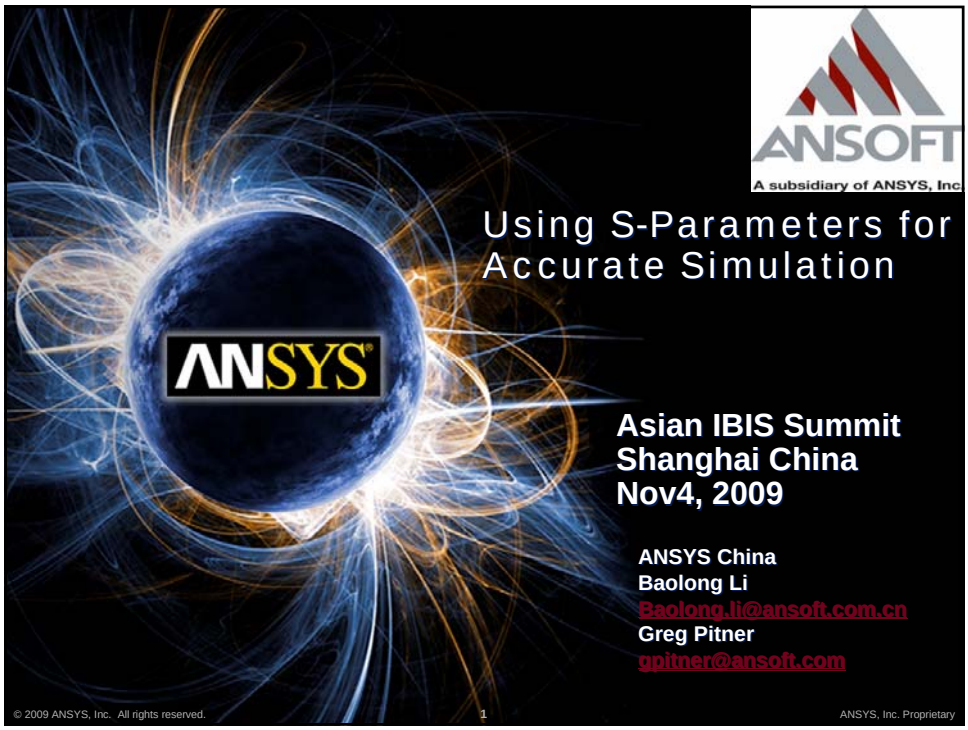


Background

ANSYS

- **S-parameter is becoming more and more popular in high speed simulation**
- **In Howard Johnson's book, we believe the F_{knee} is the upper limit of T-Line model**

$$F_{knee} = \frac{0.5}{Tr}$$

- **But is it accurate enough for transient analysis in GHz analysis?**

Fourier transform

- **Fourier transform provide mathematical mechanism for transforming frequency data to timing domain**

$$f(t) = \int_{-\infty}^{\infty} S(f)E(f)e^{2\pi jft}df$$

- **There are two approximations in real application**
  - Finite band width
  - Discrete data point

Finite bandwidth

- **Finite bandwidth S parameter like a "window" function** $W(f)$

$$W(f) = \begin{cases} 1 & -b \le f \le b \\ 0 & \text{ot her} \end{cases}$$

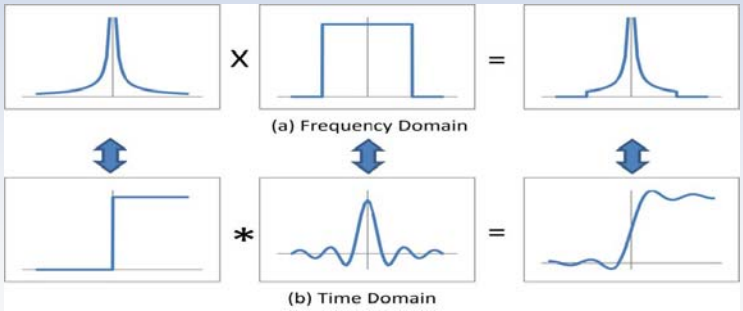
$$f(t) = \int_{-\infty}^{\infty} W(f)S(f)E(f)e^{2\pi jft}df$$

$$= \int_{-b}^{b} S(f)E(f)e^{2\pi jft}df$$

Finite bandwidth Problems

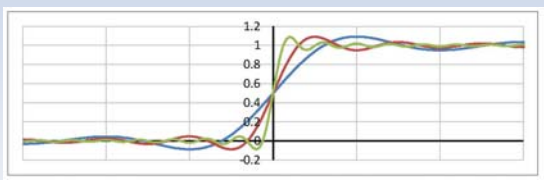
- **"Window" function will cause Oscillation**

$$W(f) \leftrightarrow 2bSa(\pi bt) = \frac{\sin \pi bt}{\pi t}$$



Finite bandwidth Problems

- **Increase bandwidth cause sharper oscillation, but never disappear**

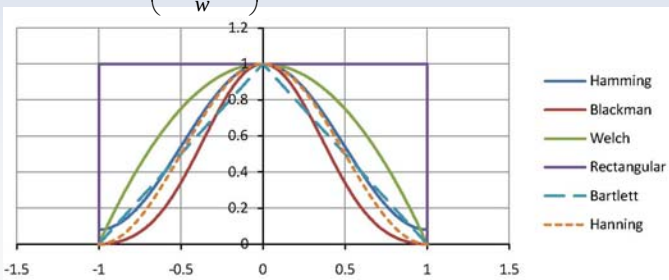


- **If expand bandwidth to infinite**

$$\lim_{b\to\infty} \frac{\sin(bt)}{\pi t} = \delta(t)$$

Using other "windows"

- **Hamming** $0.54 + 0.46\cos(\frac{2\pi f}{w})$
- **Hanning** $0.5\left[1+\cos(\frac{2\pi f}{w})\right]$
- **Blackman** $0.42 + 0.5\cos\left(\frac{2\pi f}{w}\right) + 0.08\cos\left(\frac{4\pi f}{w}\right)$
- **Welch** $1 - \left(\frac{2f}{w}\right)^2$
- **Bartlett** $1 - \left(\frac{2f}{w}\right)$



3. Window functions with a width of w=2

Results of other "windows"

- **Attenuate the spectrum near upper limit**
- **Trade-off between edge and oscillation**

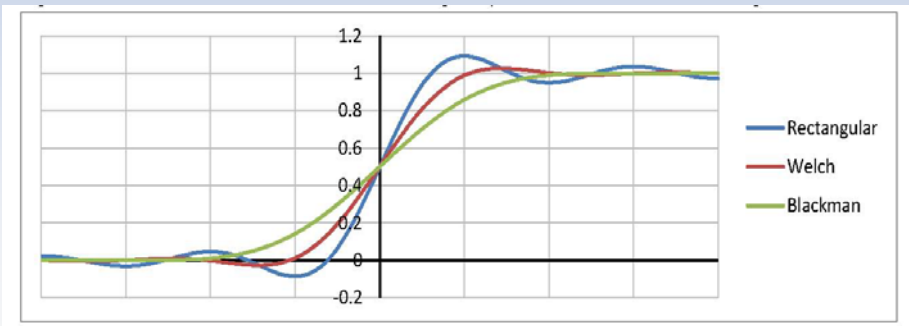


Figure 7. Step response for three different windows, each with the same bandwidth.

Idea step response of different "windows"

Table 1. Characteristics of selected window functions for continuous time

Window	*Step Response $f_s(t)$*	*10-90 Edge Rate*	*Max Overshoot*
Rectangular	$\frac{1}{2}+\frac{\mathrm{Si}(2\pi bt)}{\pi}$	$\frac{0.45}{b}$	8.95%
Welch	$\frac{1}{2}+\frac{\cos(2\pi bt)}{2\pi^2 bt}-\frac{\sin(2\pi bt)}{4\pi^3 b^2 t^2}+\frac{\mathrm{Si}(2\pi bt)}{\pi}$	$\frac{0.70}{b}$	2.70%
Hanning	$\frac{2\pi+2\mathrm{Si}(2\pi bt)-\mathrm{Si}(\pi-2\pi bt)+\mathrm{Si}(\pi+2\pi bt)}{4\pi}$	$\frac{0.97}{b}$	0.64%
Blackman	--	$\frac{1.19}{b}$	0.02%

$$Si(x)=\int_0^x \frac{\sin(a)}{a}da$$

Finite edge response of Rectangular "window"

- **Finite edge response of Rectangular "window"**

$$f(t)=\frac{1}{2}+\frac{Si(2\pi b(r-t))}{\pi}+\frac{\cos(2\pi bt)-\cos(2\pi b(t-r))+2\pi bt(Si(2\pi b(r-t))+Si(2\pi bt))}{2\pi^2 br}$$

$$f(0)=\frac{1}{2}+\frac{1-\cos(2\pi br)}{2\pi^2 br}-\frac{Si(2\pi br)}{\pi}$$

- **Rectangular "window" is Non-Causal system**

Finite edge response of Rectangular "window"

- **If increase br , $f(0)$ will closer to 0**

Table 2. Finite edge response for rectangular windows for continuous time

*Bandwidth*Risetime (**br**)*	*Edge Response at t = 0*	*Max Overshoot*
0.5	0.113	5.34%
0.75	0.056	2.41%
1	0.049	1.19%
2	0.025	0.72%
3	0.017	0.51%
5	0.010	0.32%
10	0.005	0.17%

Discrete data point

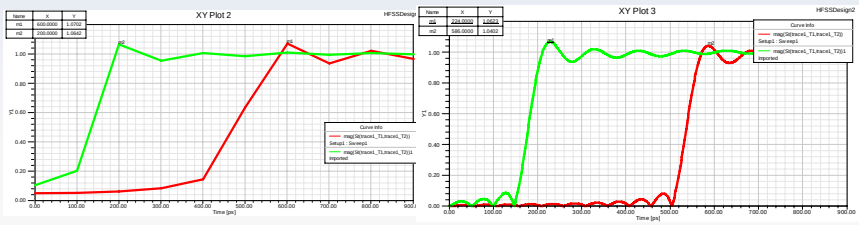
- **Simulation is discrete point data both in Timing domain and Frequency domain:**
- **Relationships of step**

$$T_{step} = \frac{1}{2F_{\max}} \qquad T_{\max} = \frac{1}{2F_{step}}$$

- **Minimum timing step is decided by the bandwidth which has been discussed**

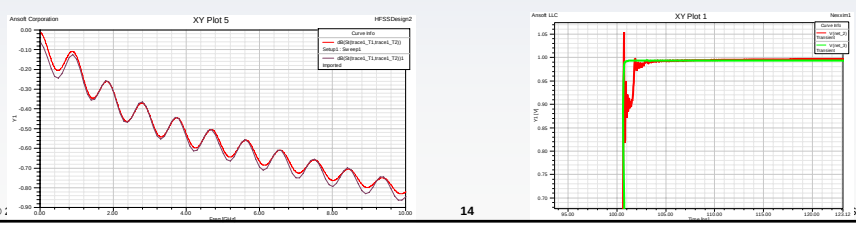
Timing step influence

- **1 inch and 3 inch matched T_line's step response using different timing step:**
- **Only different delay are expected, but different oscillation when bigger timing step**
- **Reduce timing step get correct results**



Frequency step influence

- **Discrete frequency point data convert to timing domain look like repeating series of long pulse.(Discrete Fourier transform)**
- **If frequency step is bigger, the repeating series pulse will interrupt each other**
  - Same T_line S21 using different frequency step and corresponding transient results



Different requirements of parallel and Serial signal simulation

- **Parallel signal is repeating of one bit.**
  - One rising and falling edge
  - Frequency step should be denser than 1/T
- **Serial signal is series of bit.**
  - Random bits for testing ISI
  - Frequency step should be denser than 1/n*UI

conclusion

- **Mathematical based simulation or testing have native limitation**
- **Serdes GHz simulation need broadband channel characteristic**
  - F_{knee} is limited, 5/Tr or 10/Tr
- **Discrete frequency point data is also critical for analysis**

$$T_{step} = \frac{1}{2F_{\max}} \qquad T_{\max} = \frac{1}{2F_{step}}$$

Thank you

谢谢

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INVENTIVE

Subckt Package Model in IBIS

Dr. Wenliang Dai (wldai@cadence.com)

Cadence Design Systems, Inc.

Asian IBIS Summit,
Shanghai, China,
November 4th 2009

Agenda

- **Standard IBIS Package Model Overview**
- **Requirements on IBIS Package Model in High Speed Circuit Analysis**
- **Proposed IBIS Subckt Package Model**
- **Summary**

2

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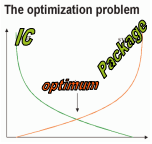
Standard IBIS Package Model Overview

- Existing Simplified IBIS Package Model
  - Single RLC value
- Customized IBIS Package Model
  - Segmented/Forked RLC value
- Coupled IBIS Package Model
  - RLC Matrix value
- Pin Mapping in Pin Numbers and Model Data Section
  - 1:1 mapping of die pins to package pins
  - Simple RLC for each signal, power and ground pin



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Agenda

- **Standard IBIS Package Model Overview**
- **Requirements on IBIS Package Model in High Speed Circuit Analysis**
- **Proposed IBIS Subckt Package Model**
- **Summary**

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Extracted Package Model by Field Solvers & Measurements

- Current Standard IBIS Package Model Format
  - Very simple RLC value with 1:1 mapping of BGA pins to Die pins
  - It makes little sense for each pwr/gnd pins
- Subckt Model for Coupling Signal, Power and Ground Nets from Field Solvers
  - Complex Spice subckt with high accuracy & efficiency by pwr/gnd pins group process
- Touchstone Format S Parameter Model from Field Solvers or Measurement
  - S/Y/Z parameter model and related Subckt model can be obtained conveniently
- Today's power & SSN analysis with lower voltage and higher current require high accurate power, ground (including decaps) and signal nets coupling circuit model for higher simulation accuracy and efficiency
  - ***Subckt or S parameter models are required***
  - ***Pin-Port Mappings are required by full system high speed circuit analysis***

Notes: **Current IBIS Package Model is NOT ENOUGH for high speed circuit analysis, especially for Power analysis & SSN simulation**

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How to Use the Extracted Subckt Package Model

- Create the Whole Circuit Netlist by Editing the Connection between the Extracted Spice Package Model and S Parameter Model in **Text File Format**
  - Good
- Create the Connection between the Package Model and other Models in GUI with additional **Pin-Node Mapping file** Manually
  - Better
- Create the Connection between Package Model and other Model automatically through **Enhanced IBIS Package Model**
  - Best and it's a Standard

Notes: **Consume complicated/coupled signal & power net subckt in IBIS models**

6

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Agenda

- Standard IBIS Package Model Overview
- Requirements on IBIS Package Model in High Speed Circuit Analysis
- Proposed IBIS Subckt Package Model
- Summary

7

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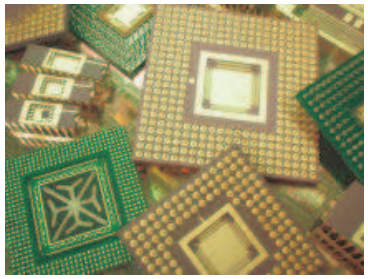
Existing IBIS Package Model in V5.0

```
[Define Package Model]
----------------------
|-- [Manufacturer]
|-- [OEM]
|-- [Description]
|-- [Number Of Sections]
|-- [Number Of Pins]
|-- [Pin Numbers]                Len, L, R, C, Fork, Endfork
|-- [Model Data]
|   ------------
|   |-- [Resistance Matrix]      Banded_matrix, Sparse_matrix,
|   |   -------------------      Full_matrix
|   |   |-- [Bandwidth]
|   |   |-- [Row]
|   |   |
|   |-- [Inductance Matrix]      Banded_matrix, Sparse_matrix,
|   |   -------------------      Full_matrix
|   |   |-- [Bandwidth]
|   |   |-- [Row]
|   |   |
|   |-- [Capacitance Matrix]     Banded_matrix, Sparse_matrix,
|   |   -------------------      Full_matrix
|   |   |-- [Bandwidth]
|   |   |-- [Row]
|   |   |
|   |-- [End Model Data]
|   |
|-- [End Package Model]
```



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What's New in the Enhanced IBIS Package Model

- [Define Package Model]
- [Manufacturer]
- [OEM]
- [Description]
- [Number Of Sections]
- [Number Of Pins]
- [Pin Numbers]
- [Model Data]
- [End Model Data]
- [End Package Model]

It also supports multiple Subckt models in one package with its pin node mapping

[Define Package Model]
[Manufacturer]
[OEM]
[Description]
[Number Of Pins]
[Number Of Sections]
[Pin Numbers]
[Model Data]
[End Model Data]
[Subckt Package Model]
[Pin-Node Mapping]
[End Pin-Node Mapping]
[Subckt Model Data]
[End Subckt Model Data]
[End Subckt Package Model]
[End Package Model]

9

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Keywords for Proposed IBIS Package Model

```
Keywords:
|
[Subckt Package Model]
|=============================================================================
|   Keyword:  [Subckt Model Data]
|   Required:  Yes
|   Description:  Indicates the beginning of the formatted subckt package model data,
|            that can include the spice subckt or s parameter model keywords.
|-----------------------------------------------------------------------------
[Pin-Node Mapping]
[End Pin-Node Mapping]
[Subckt Model Data]
[End Subckt Model Data]
|=============================================================================
|    Keyword:  [End Subckt Package Model]
|    Required:  Yes
|    Description:  Indicates the end of the formatted model data.
|    Other Notes:  In between the [Subckt Package Model] and [End Subckt Package Model]
|            keywords is the pin node mapping, data itself of subckt package model.
|-----------------------------------------------------------------------------
[End Subckt Package Model]
|
```

Notes: The goal is to specify a complicated spice-like subckt package model instead of standard simple RLC package model to be used by the keyword Subckt Package Model.

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Keywords for Proposed IBIS Package Model

- Keywords:
- |==========
- | Keyword: [Pin-Node Mapping]
- | Required: Yes
- | Description: Indicates the beginning of the formatted Pin Node mapping data for
- | subckt package model data.
- |----------
- [Pin-Node Mapping]
- |
- |==========
- | Keyword: [End Pin-Node Mapping]
- | Required: Yes
- | Description: Indicates the end of the formatted pin port mapping data.
- | Other Notes: In between the [Pin-Node Mapping] and [End Pin-Node Mapping]
- | keywords is the pin port mapping data itself. The data is a set of subckt node
- | name like N001, pin name like VDD01 and net name like Net1 as below
- | N001 VDD01 Net1
- | N002 VDD02 Net1
- | N003 VDD03 Net2
- | N004 VSS01 Net3
- | The net name like Net1 is "OPTIONAL"
- |----------
- [End Pin-Node Mapping]
- |

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Keywords for Proposed IBIS Package Model

- Keywords:
- |
- [Subckt Model Data]
- |==========
- | Keyword: [Subckt Model Data]
- | Required: Yes
- | Description: Indicates the beginning of the formatted subckt package model data,
- | that can include the subckt or s parameter model keywords.
- |----------
- |==========
- | Keyword: [End Subckt Model Data]
- | Required: Yes
- | Description: Indicates the end of the formatted subckt model data.
- | Other Notes: In between the [Subckt Model Data] and [End Subckt Model Data]
- | keywords is the data itself for subckt package model.
- | The data is a set of spice subckt or S parameter model as below
- | Spice: ".subckt PowerModel N001 N002 N007 N008 ... .ends PowerModel"
- | Or S parameter: ".MODEL name sp [DATA=(npts ...)] [DATAFILE=filename]
- |----------
- [End Subckt Model Data]
- |

12

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Agenda

- **Standard IBIS Package Model Overview**
- **Requirements on IBIS Package Model in High Speed Circuit Analysis**
- **Proposed IBIS Subckt Package Model**
- **Summary**

13

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Summary

- Requirements on IBIS Package Model
  - Accurate Power/SSN analysis with a complex package model
- Proposed Subckt Type in IBIS Package Model
  - Spice circuit or S parameter data
- Applications for IBIS Subckt Package Model
  - IC-Package-Board co-design flow and Design Link

14

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Action items

- Add the proposed subckt package model keywords into standard IBIS package part
- IBIS parser parses the subckt package keywords
  - Similar use model to existing lumped package model
- EDA tools consume the subckt package model to create circuit netlist

15

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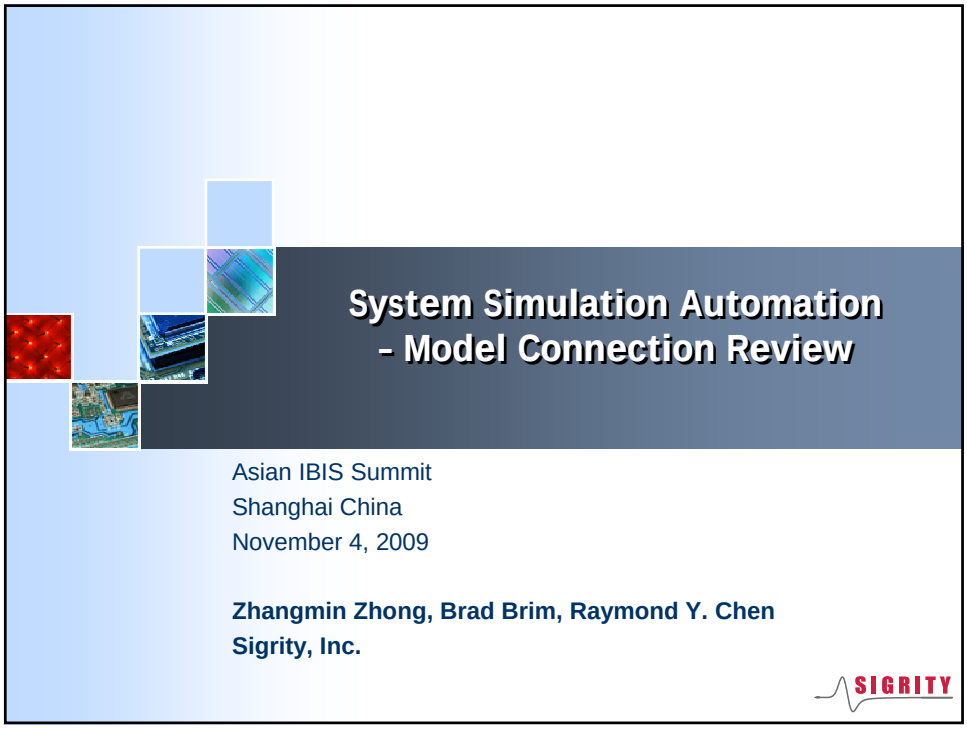
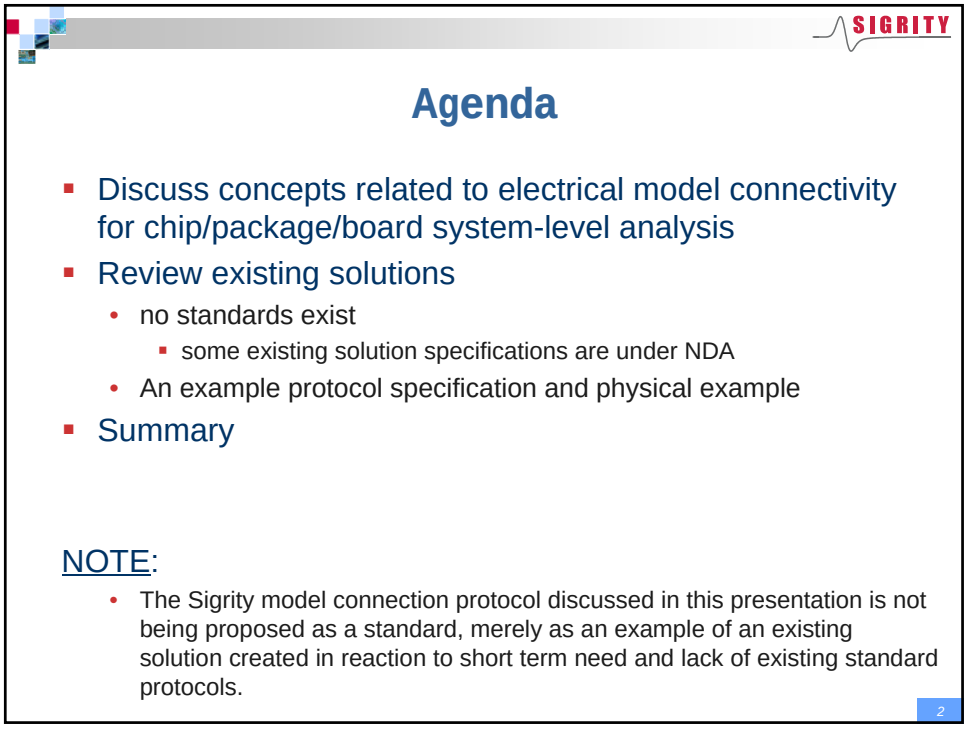
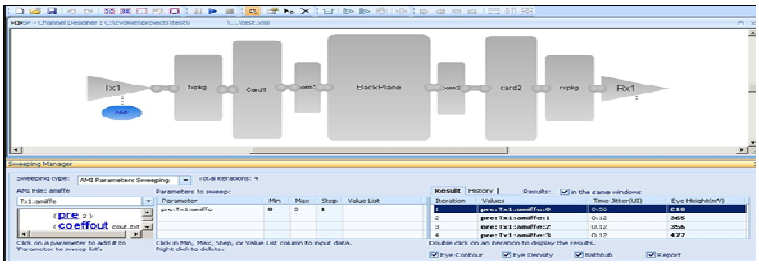

System Simulation Automation
– Model Connection Review
Asian IBIS Summit
Shanghai China
November 4, 2009
Zhangmin Zhong, Brad Brim, Raymond Y. Chen
Sigrity, Inc.
SIGRITY


SIGRITY
Agenda
Discuss concepts related to electrical model connectivity for chip/package/board system-level analysis
Review existing solutions
no standards exist
some existing solution specifications are under NDA
An example protocol specification and physical example
Summary
NOTE:
The Sigrity model connection protocol discussed in this presentation is not being proposed as a standard, merely as an example of an existing solution created in reaction to short term need and lack of existing standard protocols.
2

SIGRITY

Challenge for Chip/Package/Board, Signals and Power/Ground Simulation

- Assume I have …
  - a chip/package/board system with hundreds or thousands of physical connections (pins)
  - individual electrical models for each chip, package and board
- How do I …
  1. know which pins of one model to connect to the pins of another model?
  2. reliably and in reasonable time connect these models in a netlist or a schematic?



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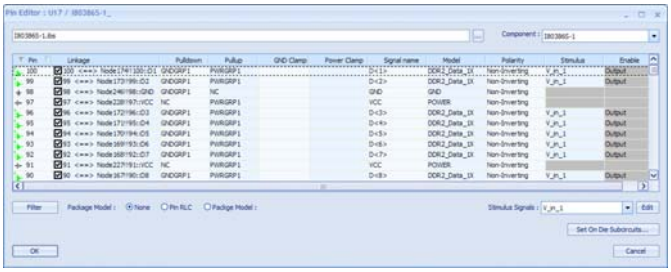
Observations

- Pin section and pin mapping sections in IBIS model are used to connect packages to PCBs, and IBIS EBD pins are used to connect DIMM modules to PCB…these enable all EDA tools to do system level simulation in the past decade



- IBIS does not provide die (chip) side connectivity and die side model
- IBIS provides physical pin information, but not physical pin to circuit node mapping for model abstraction
- IBIS provides connectivity for I/O, but not much information on the signal return paths – the power/ground network

4

SIGRITY

Requirements

- Chip/package/board systems have many physical connections (pins)
  - chip-package boundary ≈ 100 – 5000
  - package-board boundary ≈ 100 – 2000
- Not all electrical models can have pin-level resolution
  - models may be too large to compute, store, etc.
  - difficult to connect in EDA tools
- Adequate modeling may not be possible with net-level resolution
  - especially, if this low resolution is applied throughout the entire system
  - NOTE: “net-level resolution” groups all pins for each net at a domain boundary
- Support is required for
  - arbitrarily pin-grouped models
  - automated connection amongst models in EDA tools

5

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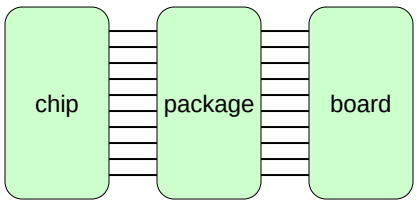
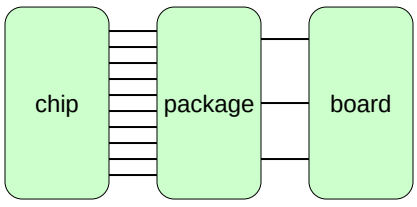
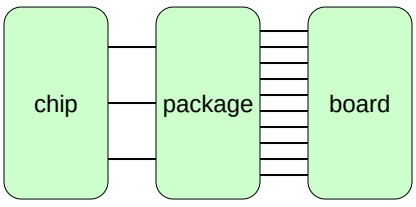
System Analysis



Physical connectivity



Chip-centric model abstraction

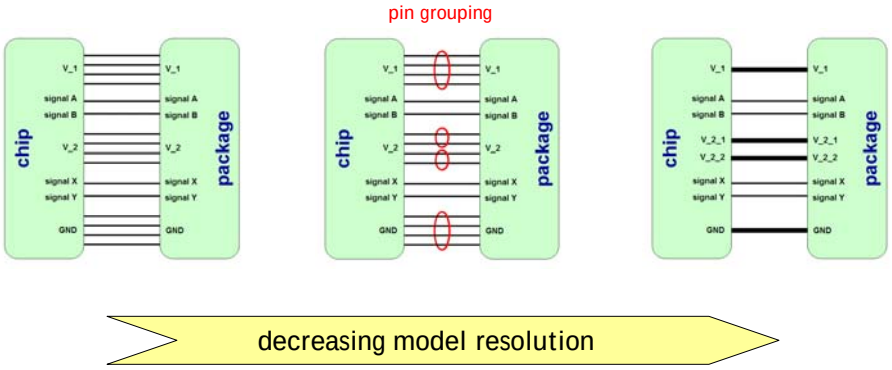


Board-centric model abstraction

6

System Analysis

- A bit more detailed view of electrical model resolution through pin grouping, for one domain boundary



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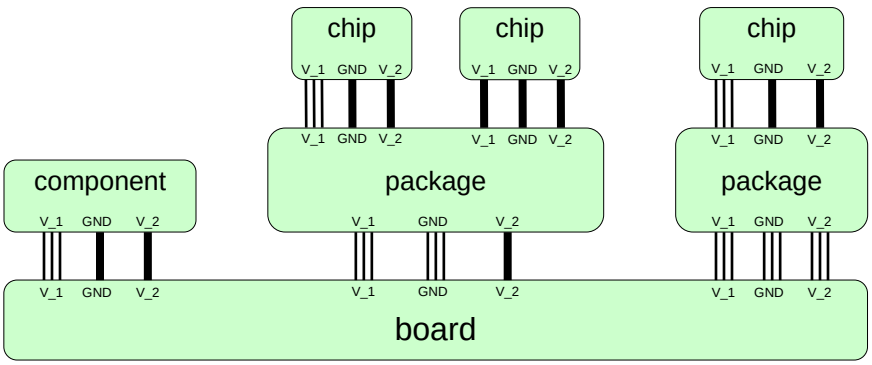
System Analysis

modern system designs requires various levels of model resolution throughout the system, with pin-level, net-level and arbitrarily grouped pins applied to the same component



8

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Existing Model Connection Protocols for Chip/Package/Board Analysis

- Sigrity MCP (**M**odel **C**onnection **P**rotocol)
  - defined by Sigrity
    - publicly available definition
  - objective to support chip/package/board system analysis
- Apache CPP
  - defined by Apache
    - definition covered under NDA
- Implemented as “headers”
- Contained within model-native comment lines
  - model could be either subcircuit or data file

9

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A Typical Model Connection Protocol (Sigrity MCP)

```
* [MCP Begin]
* [MCP Ver] 1.1
* [Structure Type] {DIE|PKG|PCB}
* [MCP Source] source text
* [Coordinate Unit] unit
* [Connection] connectionName  partName  numberPhysicalPins
*   [Connection Type] {DIE|PKG|PCB}
*     [Power Nets]
*       pinName  modelNodeName  netName  x  y
*       …
*       pinName  modelNodeName  netName  x  y
*    [Ground Nets]
*       pinName  modelNodeName  netName  x  y
*       …
*       pinName  modelNodeName  netName  x  y
*     [Signal Nets]
*       pinName  modelNodeName  netName  x  y
*       …
*       pinName  modelNodeName  netName  x  y
* [MCP End]
```

10

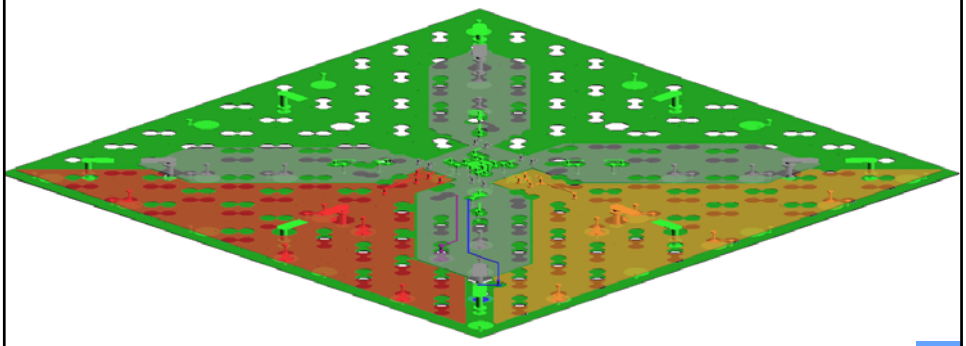
A Typical Model Connection Protocol

- Only one instance of [Structure Type]
- Multiple instances of [Connection] are possible
  - for a single-die package there will be one die-type connection and one pcb-type connection
  - for a pcb there may be many package type connections
  - for a multi-die SiP package there may be multiple die-type connections
- Only one instance of [Connection Type] per [Connection]
- For power integrity applications there may be no signal nets in the model
- Not all physical pins must be documented, only those included in the electrical model
  - For power integrity applications there may be no signal nets
  - For Touchstone data files there may only be signal nets
    - the reference terminal is implicit for the data file
  - For SPICE subcircuits there are likely grounds net but maybe no power nets
    - the reference terminal must be explicit

11

A Physical Example

- a few nets in a small 4-layer flipchip BGA package
  (so the MCP sections fin on a single page)
  - 3 power nets
  - 1 ground net
  - 2 signal nets



12

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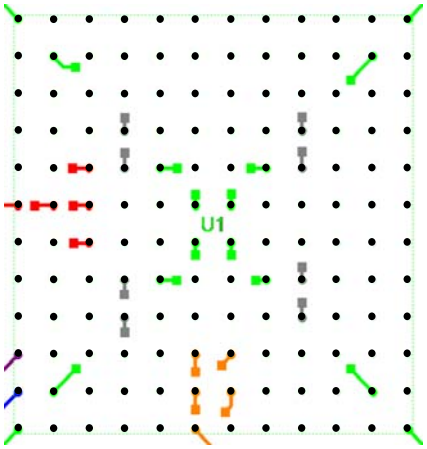
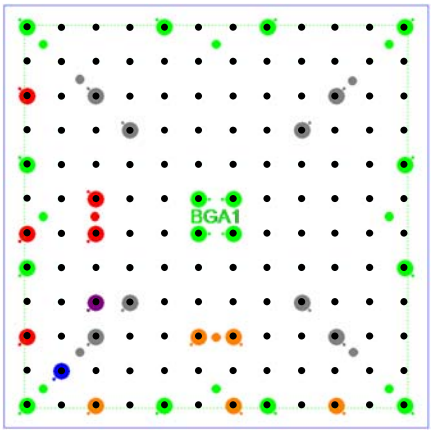
12-by-12 bump and ball arrays
(*for active nets*)

die-side solder bumps



board-side solder balls



13

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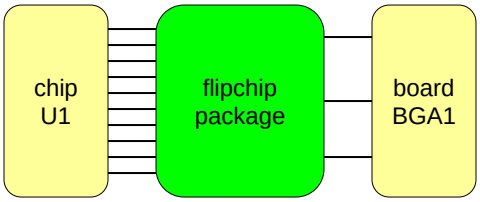
Model Resolution

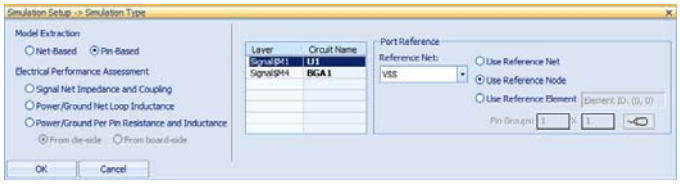
- pin-level at the chip-package boundary
  - 36 physical pins - 36 electrical nodes
    - 18 power nodes - 5 VDD_1, 5 VDD_4, 8 VDDcore
    - 16 ground nodes - 16 VSS
    - 2 signal nodes - Net_1, Net_2
- net-level at the package-board boundary
  - 36 physical pins - 6 electrical nodes
    - 3 power nodes - 1 VDD_1, 1 VDD_4, 1 VDDcore
    - 1 ground nodes - 1 VSS
    - 2 signal nodes - Net_1, Net_2



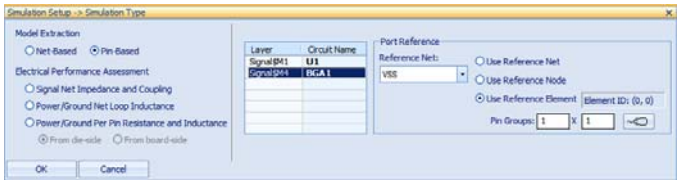
14

Model Extraction Setup

- die-side setup for pin-level model extraction



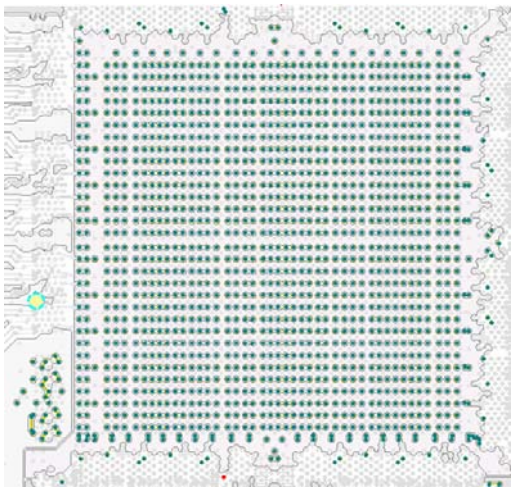
- board-side setup for net-based model extraction
  - equivalent to pin-level model extraction with 1-by-1 grid-based pin grouping

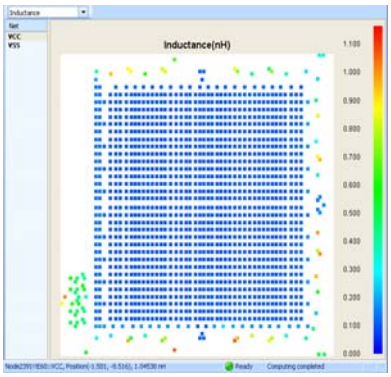


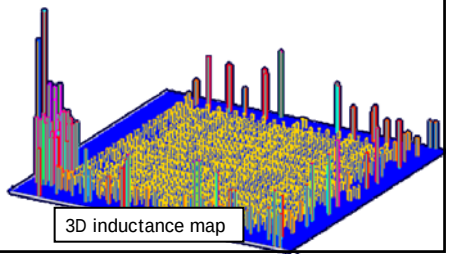
15

A Typical Package

(*one power net*)







3D inductance map

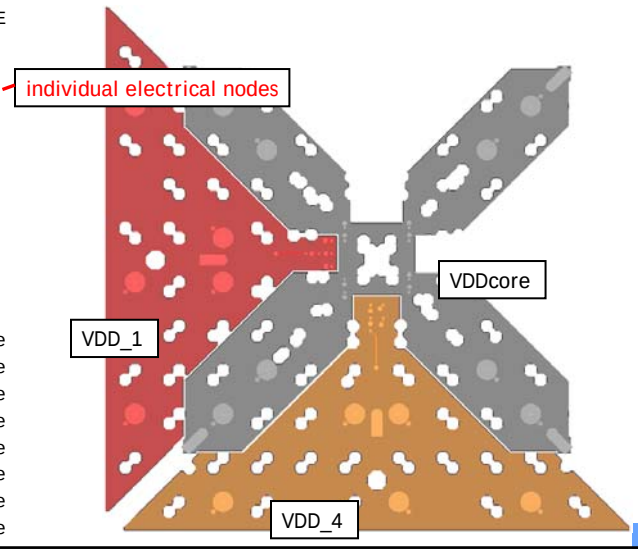
A SPICE circuit with MCP header
(a mixed pin-level/net-level model)

```
.SUBCKT FlipChip_pkg_SPICE
+  U1_E3  U1_F1   U1_F2   U1_F3   U1_G3
+  U1_K6  U1_K7   U1_L6   U1_L7   U1_M6
+  U1_D4  U1_D9   U1_E4   U1_E9   U1_H4  U1_H9  U1_J4   U1_J9
+  U1_A1  U1_A12  U1_B11  U1_B2   U1_E5  U1_E8  U1_F7   U1_G6
+  U1_G7  U1_H5   U1_H8   U1_L11  U1_L2  U1_M1  U1_M12  U1_F6
+  U1_L1  U1_K1
+  BGA1_C1  BGA1_K6  BGA1_C10  BGA1_A1  BGA1_L2  BGA1_J3
*
* The following is the Sigrity MCP Section
*****************************************
*[MCP Begin]
*[MCP Ver] 1.0
*[Structure Type] PKG
*[MCP Source] Sigrity XtractIM 3.0.2.07061 7/18/2009
```

17

A SPICE circuit with MCP header
(a pin-level die-side connection)

```
*[Connection] U1 die_12x12 144
*[Connection Type] DIE
*[Power Nets]
* E3   U1_E3   VDD_1
* F1   U1_F1   VDD_1
* F2   U1_F2   VDD_1
* F3   U1_F3   VDD_1
* G3   U1_G3   VDD_1
* K6   U1_K6   VDD_4
* K7   U1_K7   VDD_4
* L6   U1_L6   VDD_4
* L7   U1_L7   VDD_4
* M6   U1_M6   VDD_4
* D4   U1_D4   VDDcore
* D9   U1_D9   VDDcore
* E4   U1_E4   VDDcore
* E9   U1_E9   VDDcore
* H4   U1_H4   VDDcore
* H9   U1_H9   VDDcore
* J4   U1_J4   VDDcore
* J9   U1_J9   VDDcore
```

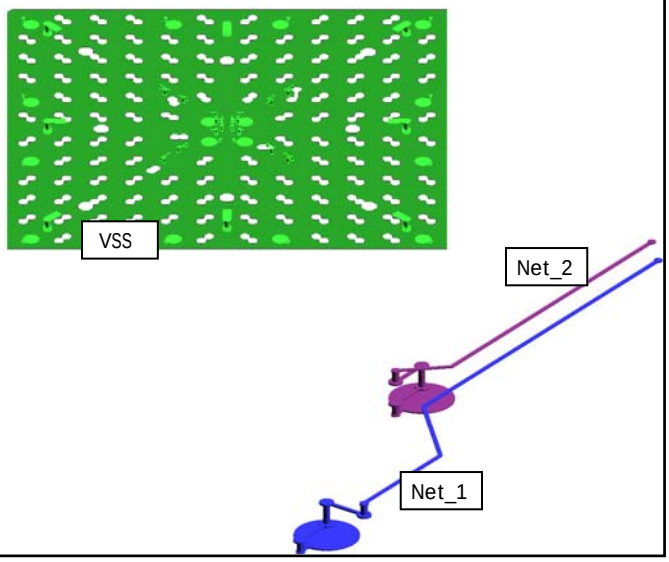


18

A SPICE circuit with MCP header

(a pin-level die-side connection)

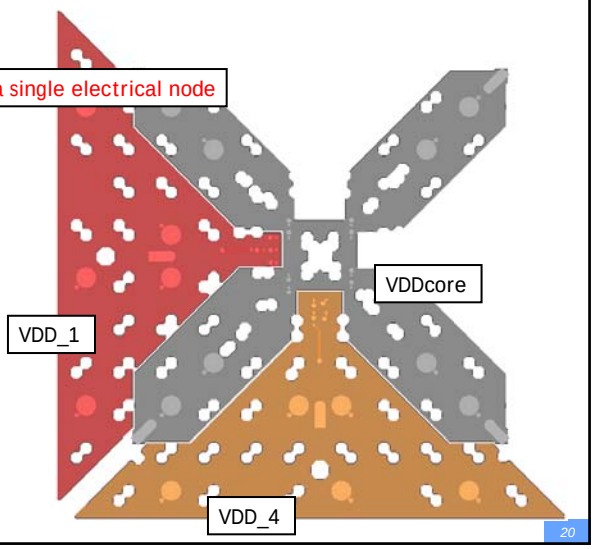
```
*[Ground Nets]
* A1    U1_A1    VSS
* A12   U1_A12   VSS
* B11   U1_B11   VSS
* B2    U1_B2    VSS
* E5    U1_E5    VSS
* E8    U1_E8    VSS
* F7    U1_F7    VSS
* G6    U1_G6    VSS
* G7    U1_G7    VSS
* H5    U1_H5    VSS
* H8    U1_H8    VSS
* L11   U1_L11   VSS
* L2    U1_L2    VSS
* M1    U1_M1    VSS
* M12   U1_M12   VSS
* F6    U1_F6    VSS
*[Signal Nets]
* L1    U1_L1    Net_1
* K1    U1_K1    Net_2
```



A SPICE circuit with MCP header

(a net-base pcb-side connection)

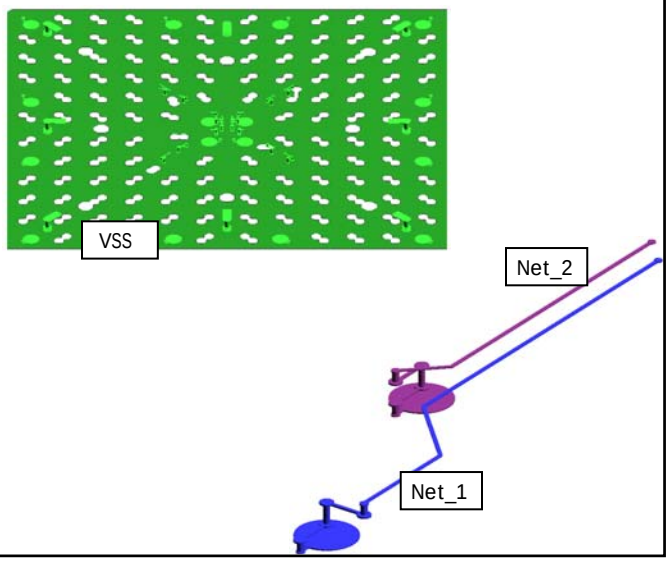
```
*[Connection] BGA1 board_12x12 144
*[Connection Type] PCB
*[Power Nets]
* C1    BGA1_C1    VDD_1
* F3    BGA1_C1    VDD_1
* G1    BGA1_C1    VDD_1
* G3    BGA1_C1    VDD_1
* K1    BGA1_C1    VDD_1
* K6    BGA1_K6    VDD_4
* K7    BGA1_K6    VDD_4
* M10   BGA1_K6    VDD_4
* M3    BGA1_K6    VDD_4
* M7    BGA1_K6    VDD_4
* C10   BGA1_C10   VDDcore
* C3    BGA1_C10   VDDcore
* D4    BGA1_C10   VDDcore
* D9    BGA1_C10   VDDcore
* J4    BGA1_C10   VDDcore
* J9    BGA1_C10   VDDcore
* K10   BGA1_C10   VDDcore
* K3    BGA1_C10   VDDcore
```



A SPICE circuit with MCP header

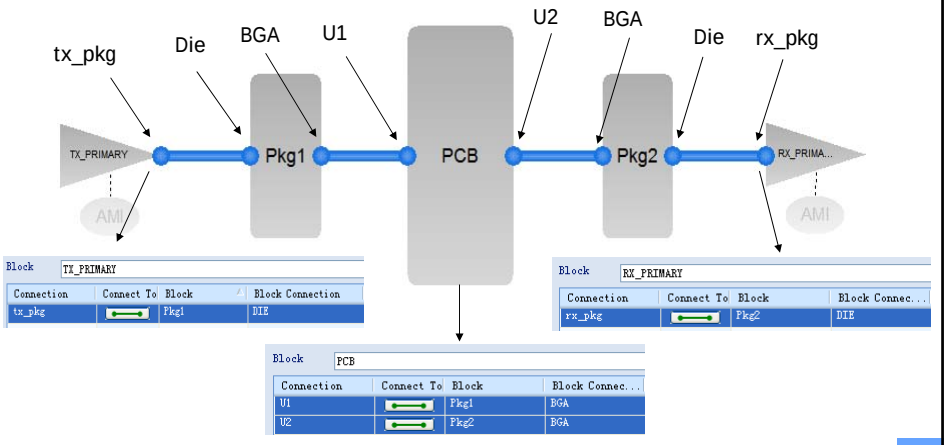
(a net-level pcb-side connection)

```
*[Ground Nets]
* A1    BGA1_A1    VSS
* A12   BGA1_A1    VSS
* A5    BGA1_A1    VSS
* A8    BGA1_A1    VSS
* E1    BGA1_A1    VSS
* E12   BGA1_A1    VSS
* F6    BGA1_A1    VSS
* F7    BGA1_A1    VSS
* G6    BGA1_A1    VSS
* G7    BGA1_A1    VSS
* H1    BGA1_A1    VSS
* H12   BGA1_A1    VSS
* M1    BGA1_A1    VSS
* M12   BGA1_A1    VSS
* M5    BGA1_A1    VSS
* M8    BGA1_A1    VSS
*[Signal Nets]
* L2    BGA1_L2    Net_1
* J3    BGA1_J3    Net_2
*
*[MCP End]
```



A Channel Connection

- The channel is comprised of one transmitter, one receiver, a printed-circuit board or PCB and two packages
- MCP is used to maintain the connections between blocks



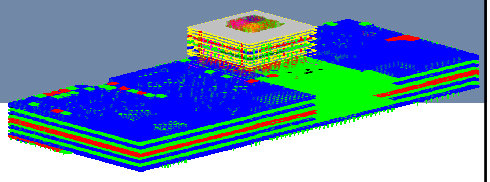
22

Summary

- Chip/package/board designs may have thousands of pins
- Chip/package/board system analysis requires
  - user-definable model resolution
  - automated connection support for EDA tools
- Circuit and data models are commonly applied
  - both should be supported by any connection protocol
- Model connection protocols are much more than simply “port names”
- Proprietary model connection protocols are currently being applied
- An industry standard model connection protocol should be defined
  - user and EDA vendor participation will be required to agree on a standard
  - active participation by more than a few individuals will be required

23

Thank You!



24