Noise Countermeasure Design Technology for Signal and Power Integrity

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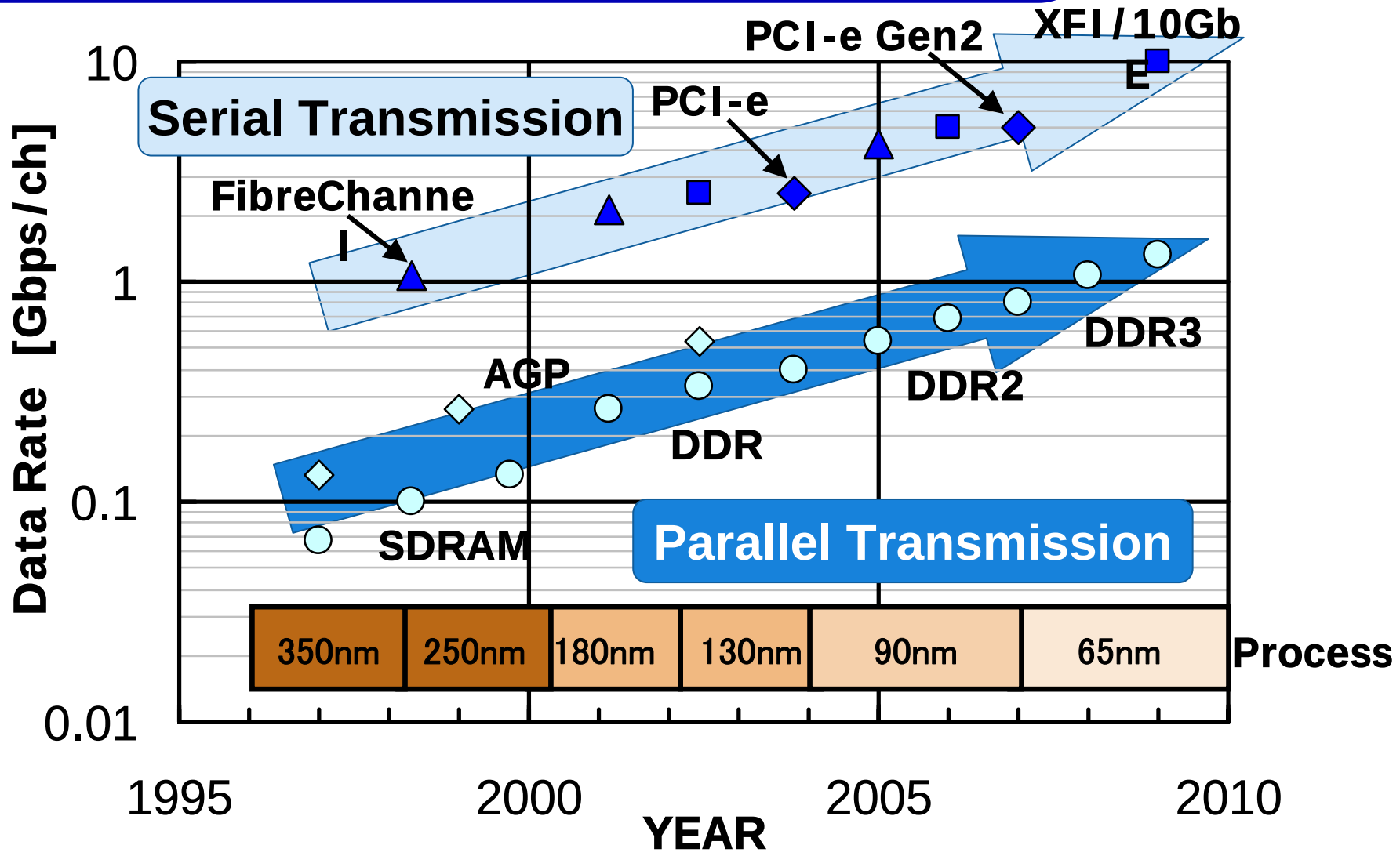
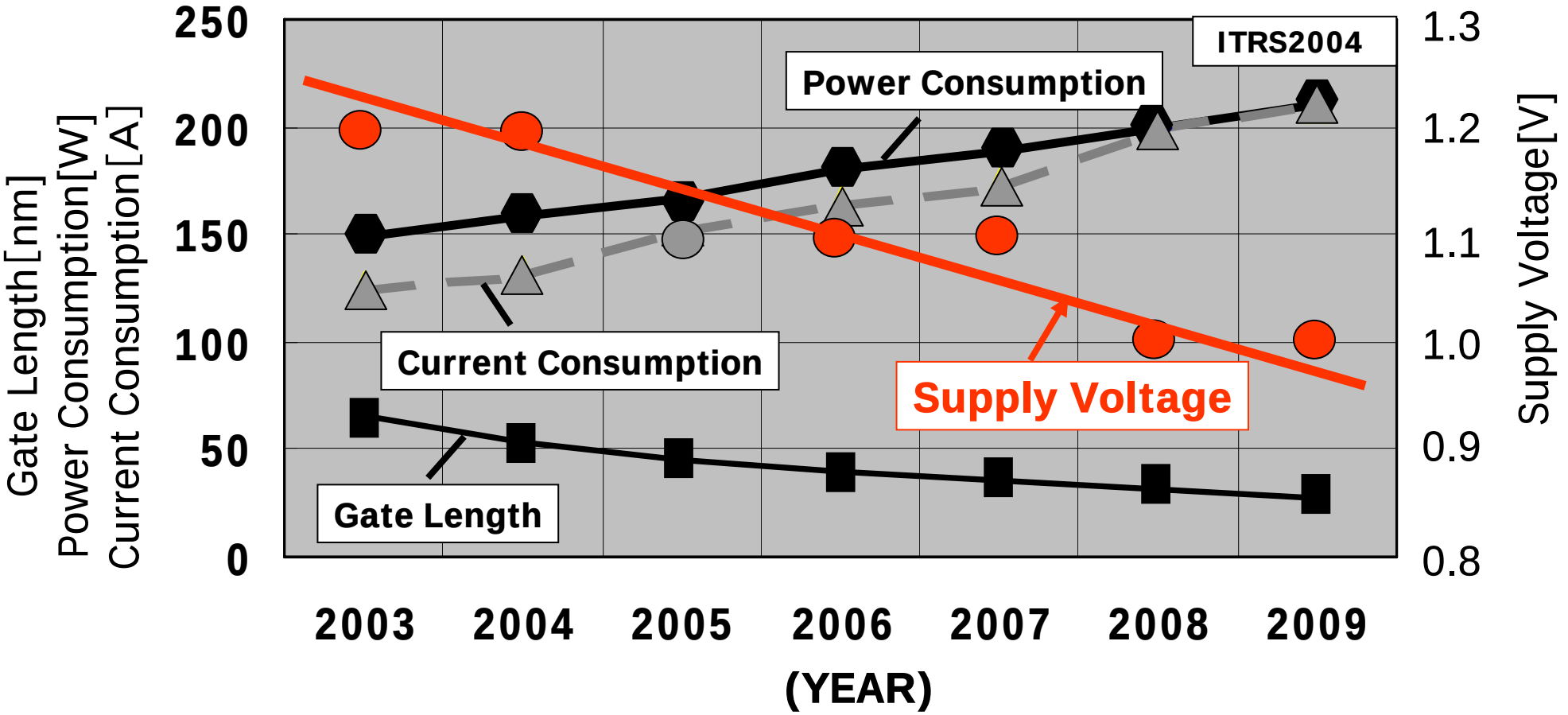
1. Background

Speed Up of Operating Frequency



1. Background

Lowering of Supply Voltage



Supply voltage : Lowering → Allowable power noise : Smaller

2. Tasks

Emerging of Noise Problem

1. Signal Integrity(SI)
   (1) Reflection noise,Crosstalk noise
   (2) Skin effect、Dielectric loss
   (3) ISI：Inter Symbol Interference
2. Power Integrity (PI, power noise)
   (1) Simultaneous switching noise
   (2) Voltage and ground bounce noise
   (3) Noise caused by return current
3. EMC
   (1) EMI
   (2) ESD
4. Composite Noise
   Complex noise problems composed of SI,PI and EMI/ESD etc..
   Ex. Deterioration of cell phone antenna sensitivity

3. Countermeasures

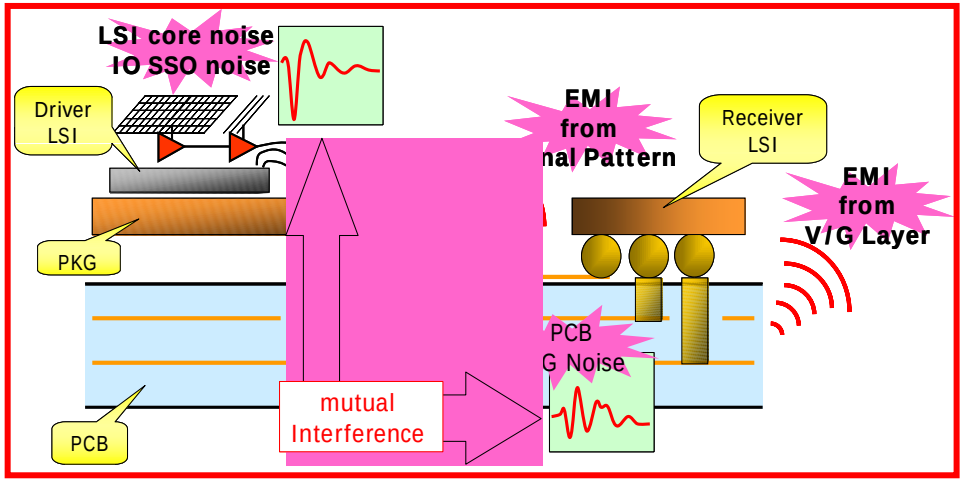
1995 2000 2005 NOW

Simulation based Design

Floor Plan based Analysys

Unified Analysis Enviornmemt

Signal Integrity	**Full automatic verification**	**Advice for design condition**	**Multi-Gbps analysis**
Power Integrity		**Middle scale**	**Large scale**
EMC(EMI,ESD)	**EMI**	**ESD Return Current**	



LSI Power Noise Analysis

LSI,PCB Unified Analysis

Technical Computing

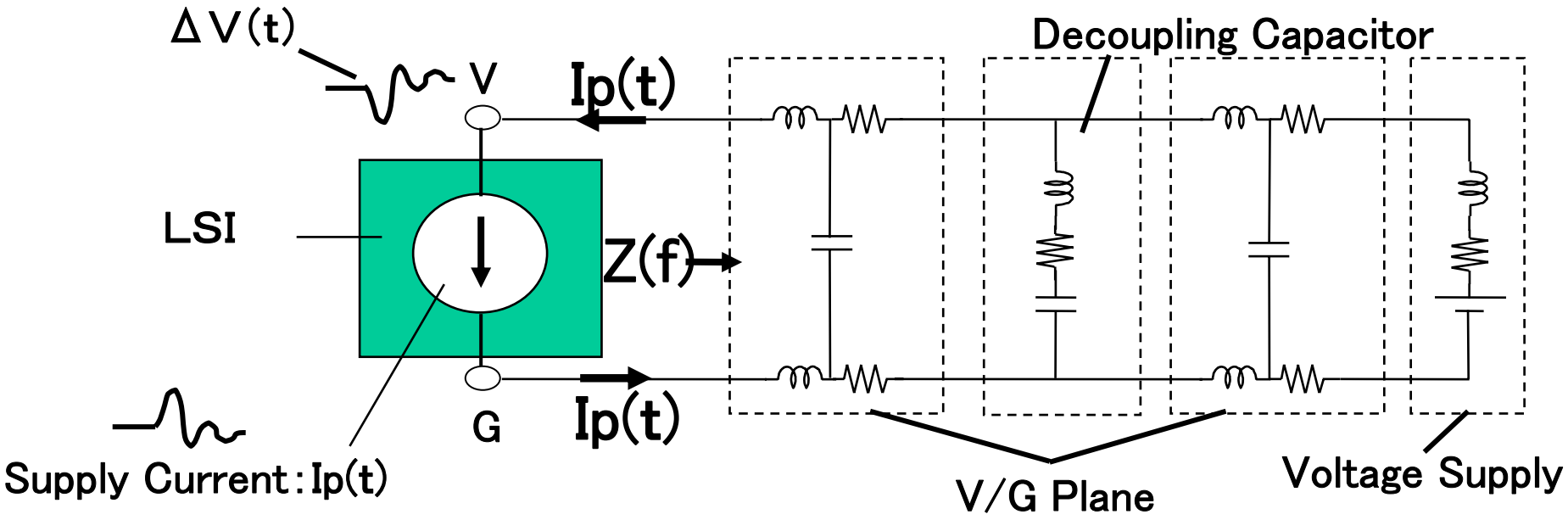
- Large Scale Analysis
- high Speed Analysis

4. LSI,PCB Unified Noise Analysis

Occurring principle of Power noise

- Power noise : $\Delta V = -Z(f) \times \Delta Ip$
- V/G Impedance : $Z(f) \leqq \Delta Vmax / \Delta Ip$ = Allowable Impedance

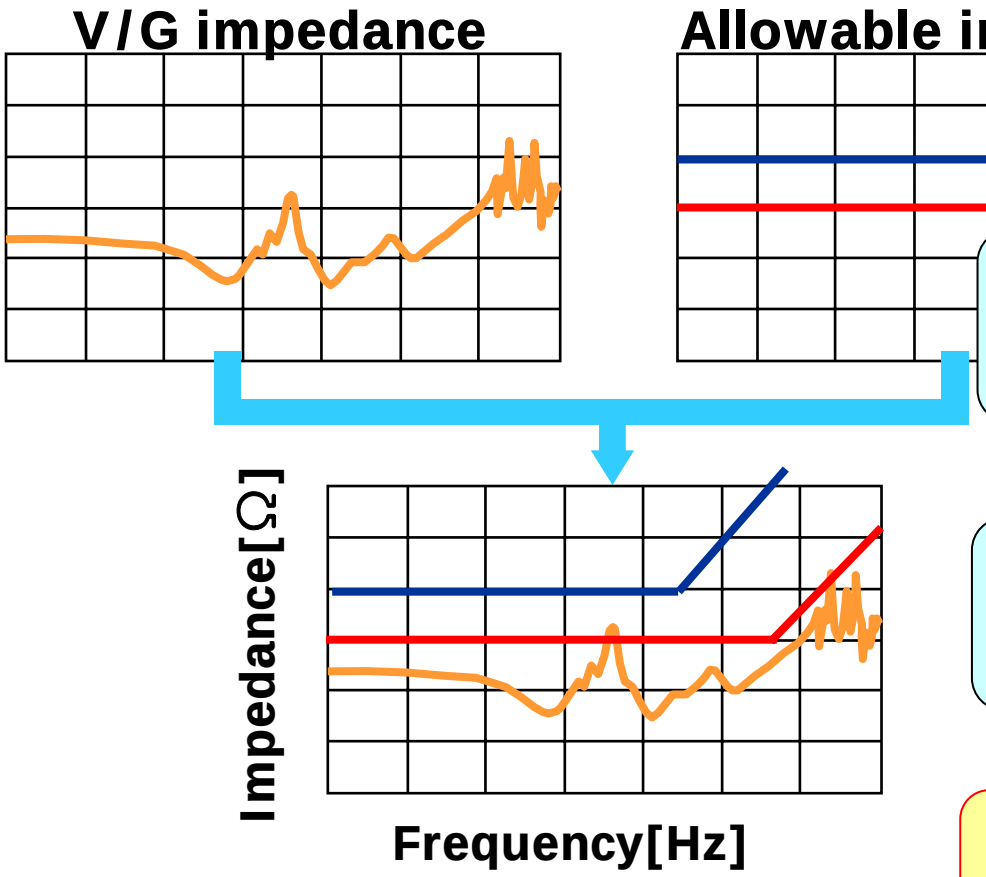
Equivalent Circuit of LSI,PCB and voltage supply



4. LSI,PCB Unified Noise Analysis

Tasks

- **High accuracy power noise analysis**



Allowable impedance decreasing caused by frequency increasing and supply voltage decreasing

Suppressing V/G impedance under the allowable impedance become more difficult

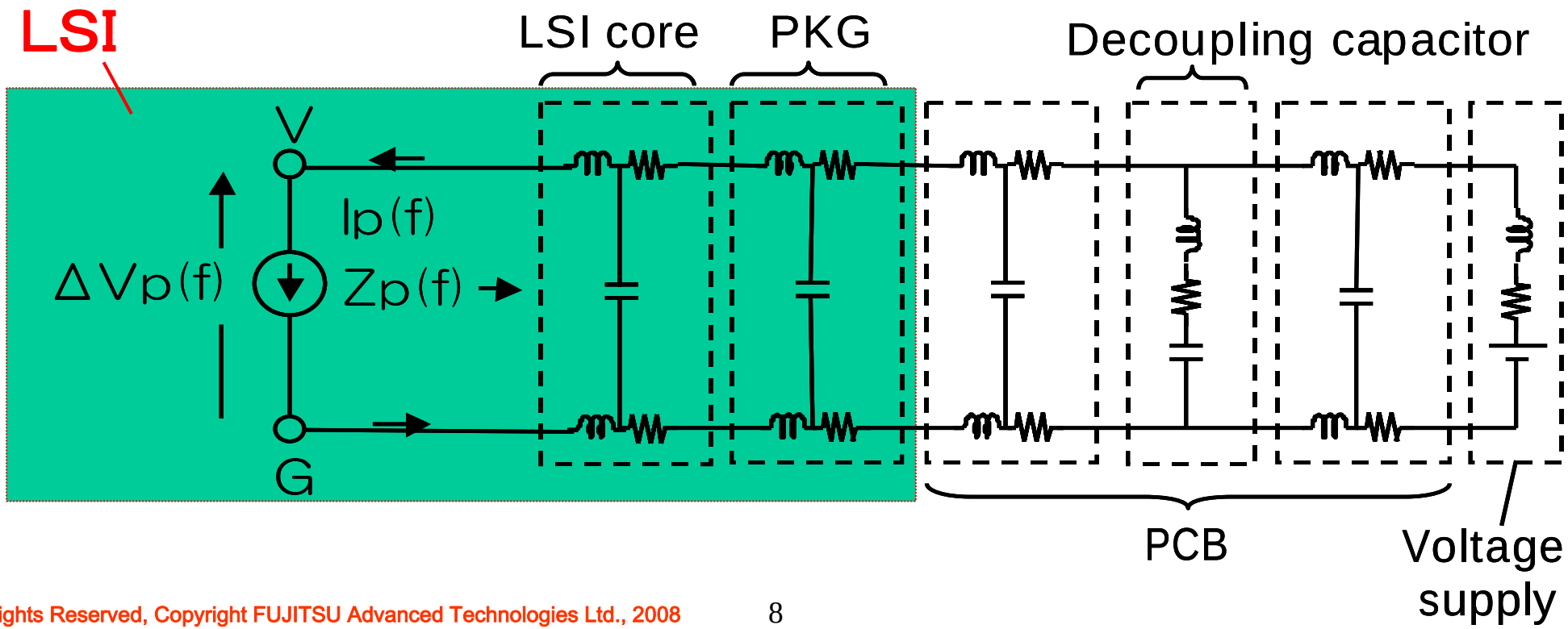
High accuracy power noise analysis method is required

4. LSI,PCB Unified Noise Analysis

Tasks

LSI,PCB Unified Noise Analysis

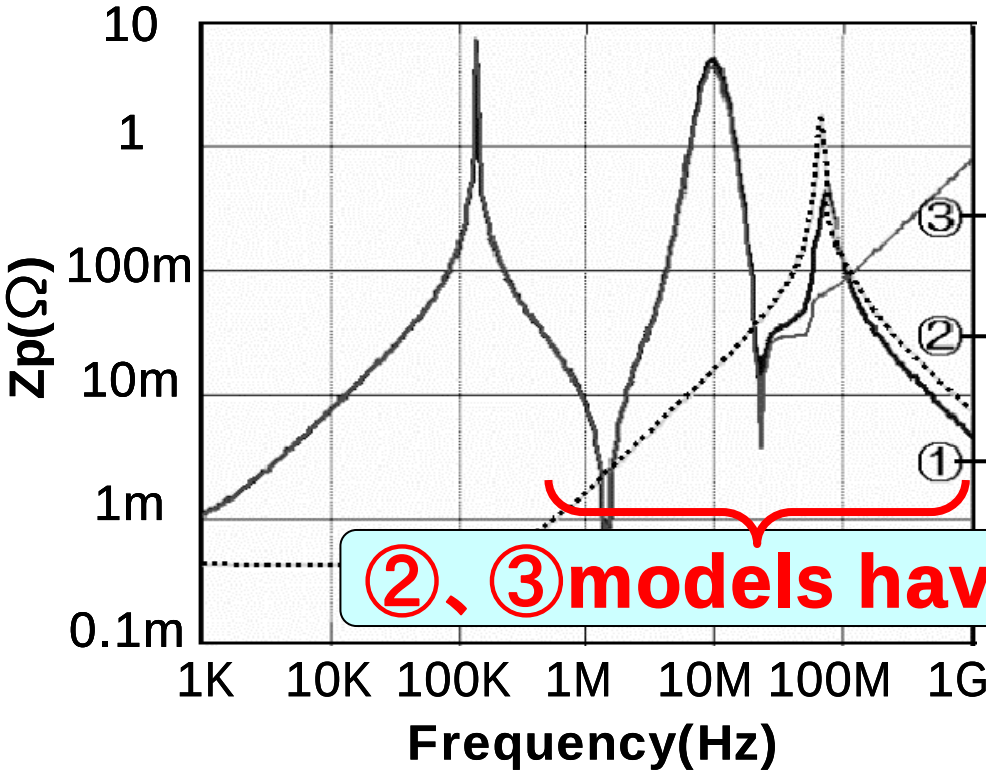
More Detailed Equivalent Circuit of LSI,PCB and voltage supply



4. LSI,PCB Unified Noise Analysis

Tasks

LSI,PCB Unified Noise Analysis



Using PCB model

Using LSI model

Using LSI and PCB model

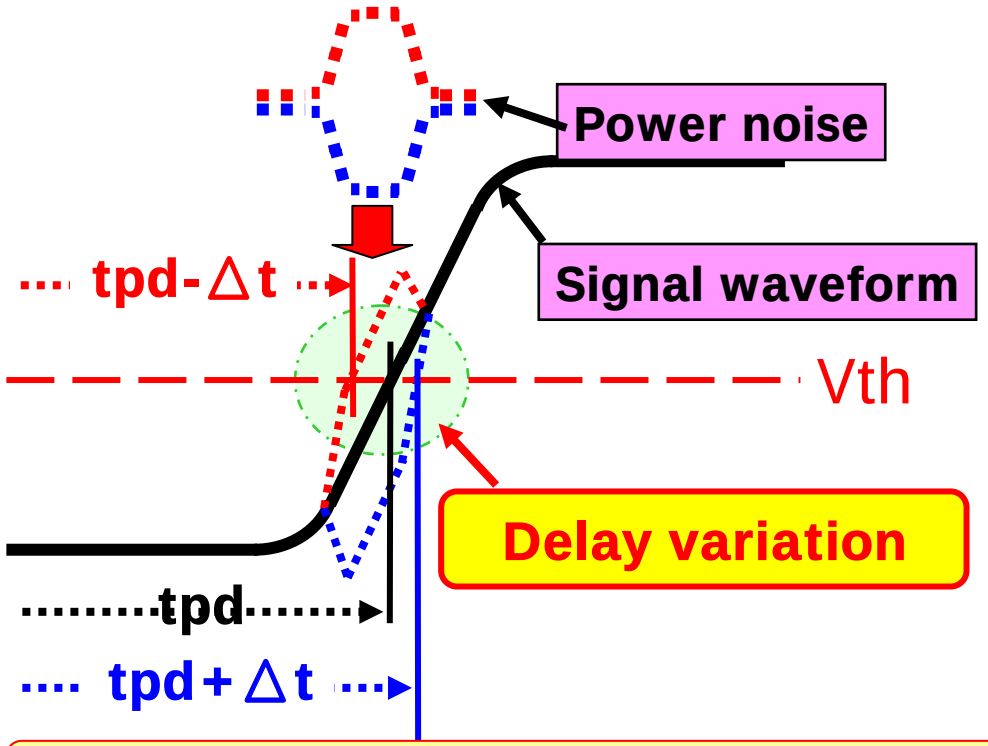
②、③models have large calculation error

LSI,PCB unified model is essential for high accuracy

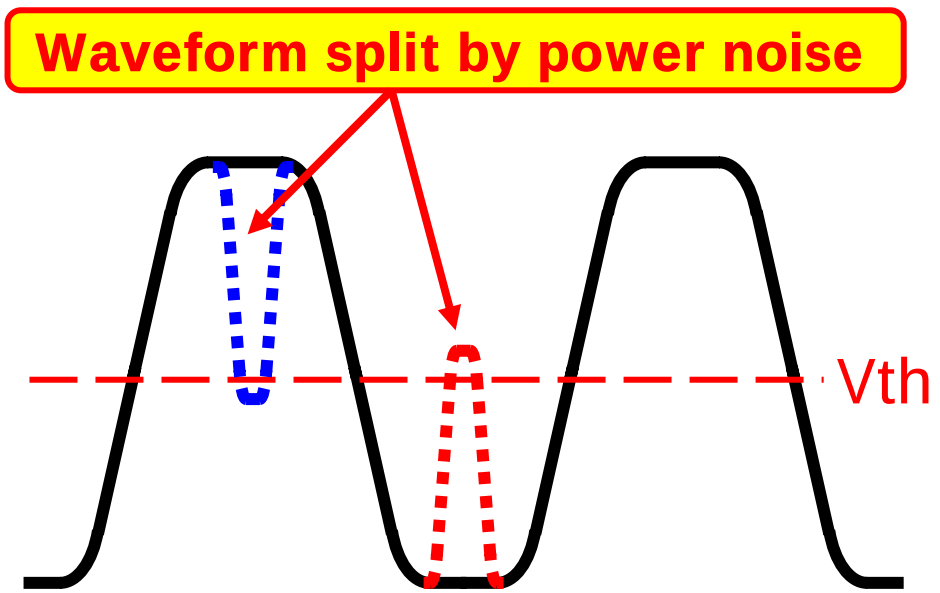
Tasks

LSI,PCB Unified Noise Analysis

Delay variation of signal and clock



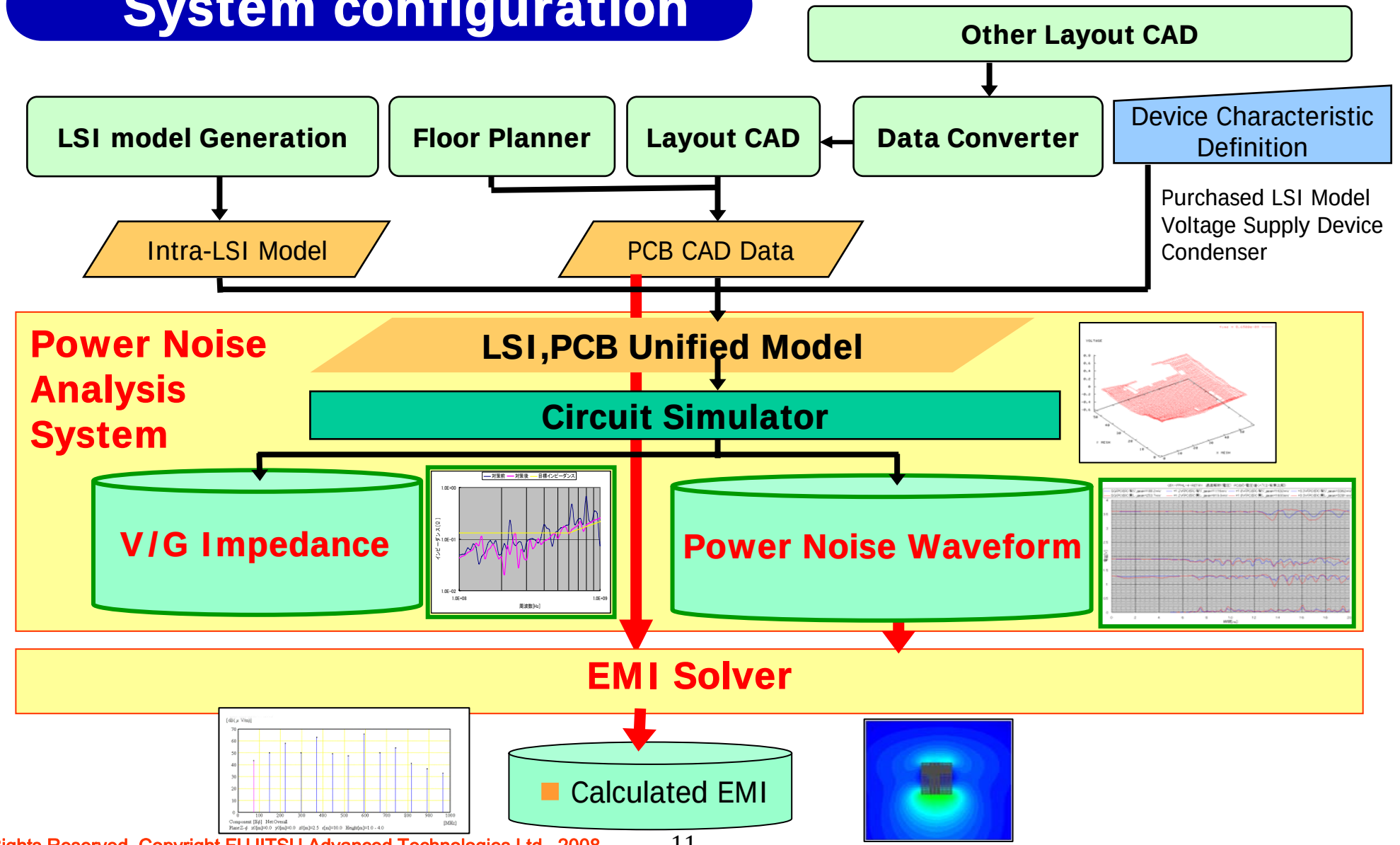
Split clock waveform



SI and PI Problem should be solved simultaneously

4. LSI,PCB Unified Noise Analysis

System configuration



4. LSI,PCB Unified Noise Analysis

LSI,PCB Unified model

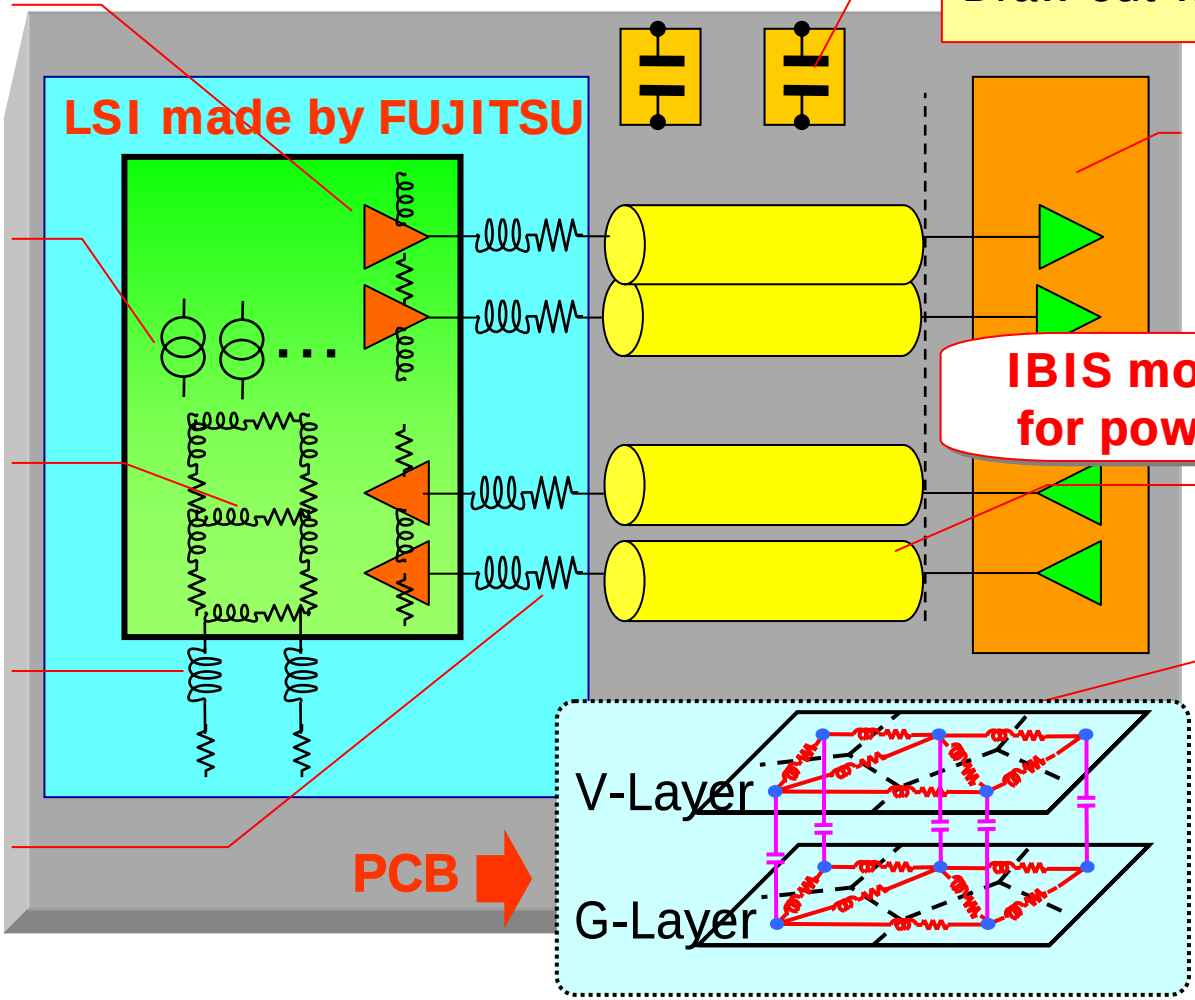
IO cell:
SPICE model
Behavior model

LSI core:
Distributed
current Source

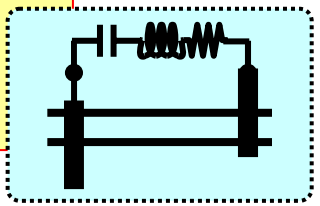
Intra-LSI V/G:
Lattice of LCR
SPICE model

V/G Pin:
LCR model

Package:
LCR model



Bypass condenser
(C, ESL, ESR)
Draw out wiring



Purchased LSI：
IBIS model
(IO Model,PKG)

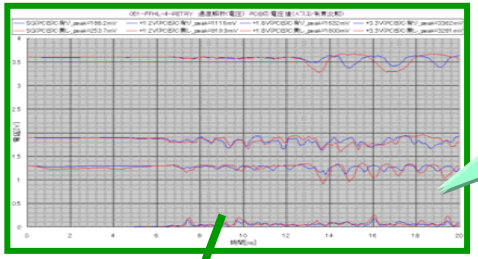
IBIS models not suitable for power noise analysis

Wiring/via:
LCR ladder model

Board V/G:
LCR Mesh model

4. LSI,PCB Unified Noise Analysis

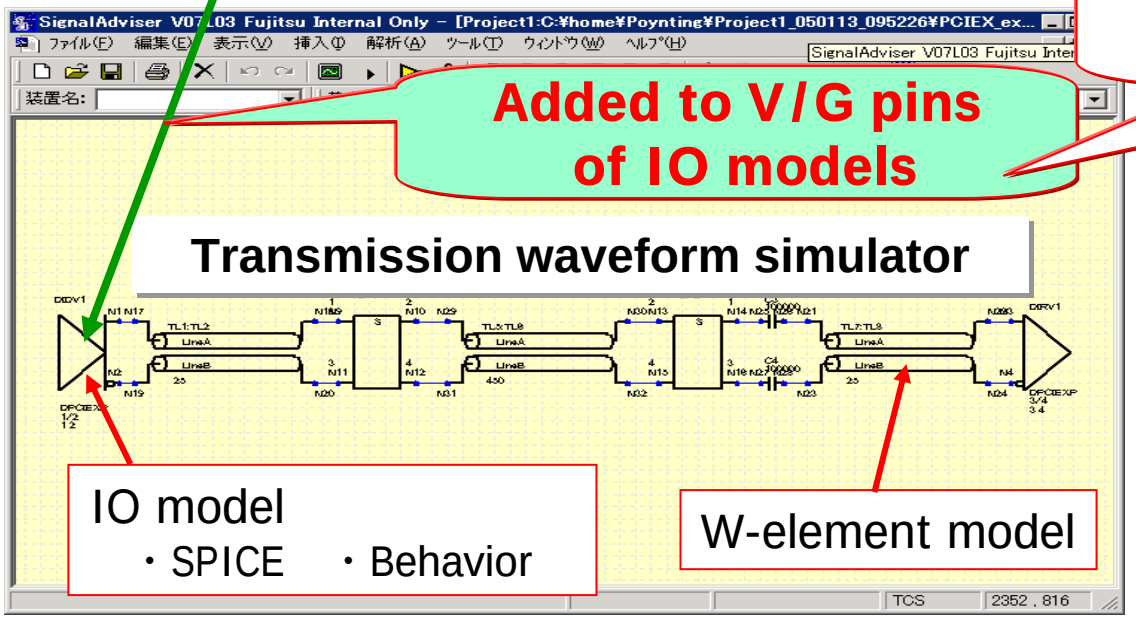
High Speed Transmission Waveform Simulation with Power noise



Power Noise Waveforms
calculated by LSI,PCB Unified Analysis

IBIS models not suitable for such a method

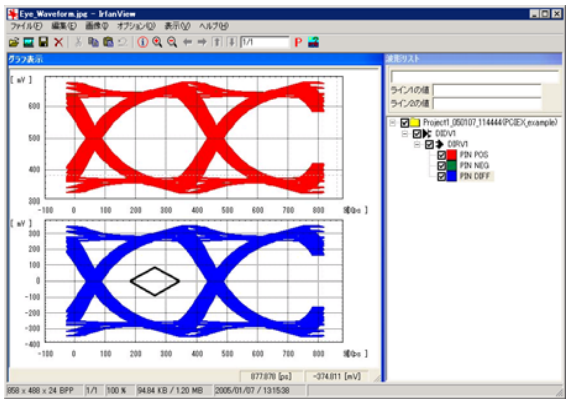
Added to V/G pins of IO models



IO model
・SPICE ・Behavior

W-element model

Eye pattern diagram



This method significantly shortens the calculation time comparing to the full LSI,PCB Unified Analysis with the comparable accuracy.

4. LSI,PCB Unified Noise Analysis

Two typical operating flows

LSI design stage (Pre-simulation flow)

- Optimizing noise countermeasure design of LSI and PCB
  - LSI IO selection,Pin Layout,decoupling capacitor,PKG selection
  - PCB design conditions (layer configuration,topology,decoupling Capacitor)

LSI ,PCB design verification stage(Post-simulation flow)

- Noise verification of LSI and PCB taking account of mutual interference

- Avoiding LSI remake、 Reducing PCB trial production
- Reducing number of parts
- Shortening design and evaluation term

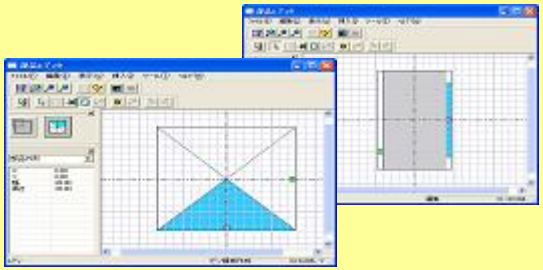
4. LSI,PCB Unified Noise Analysis

Pre-Simulation flow

LSI specification
PCB design constraints

Rough parts difinition
(Minimizing input information)

FloorPlanner

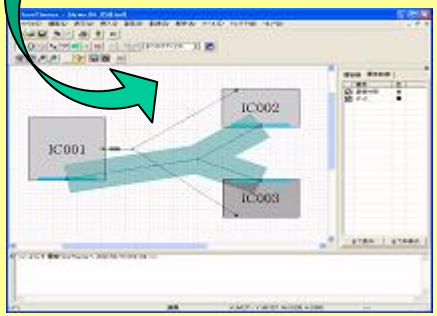


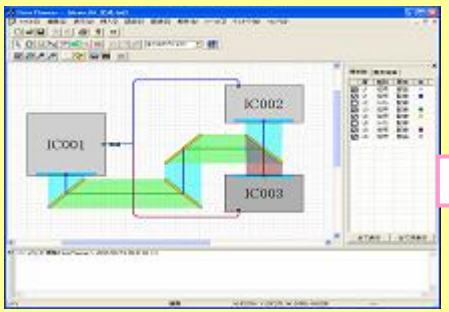
Board Spec.

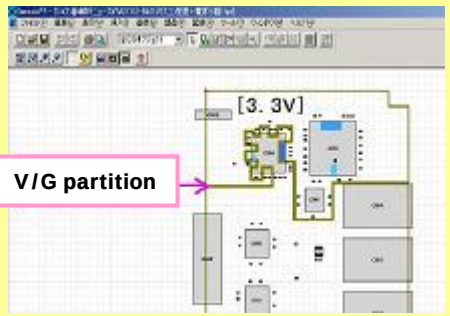
Device Char.

LSI Spec.

LSI Model

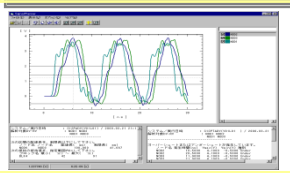




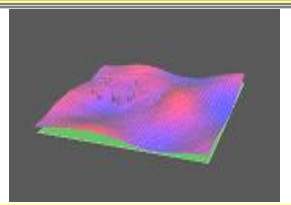


Parts layout study **Wiring strategy study** **V/G design study**

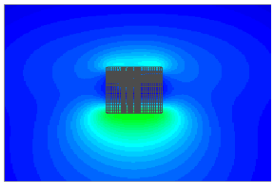
Transmission line analysis → **Signal Integrity**



Power noise analysis → **Power Integrity**



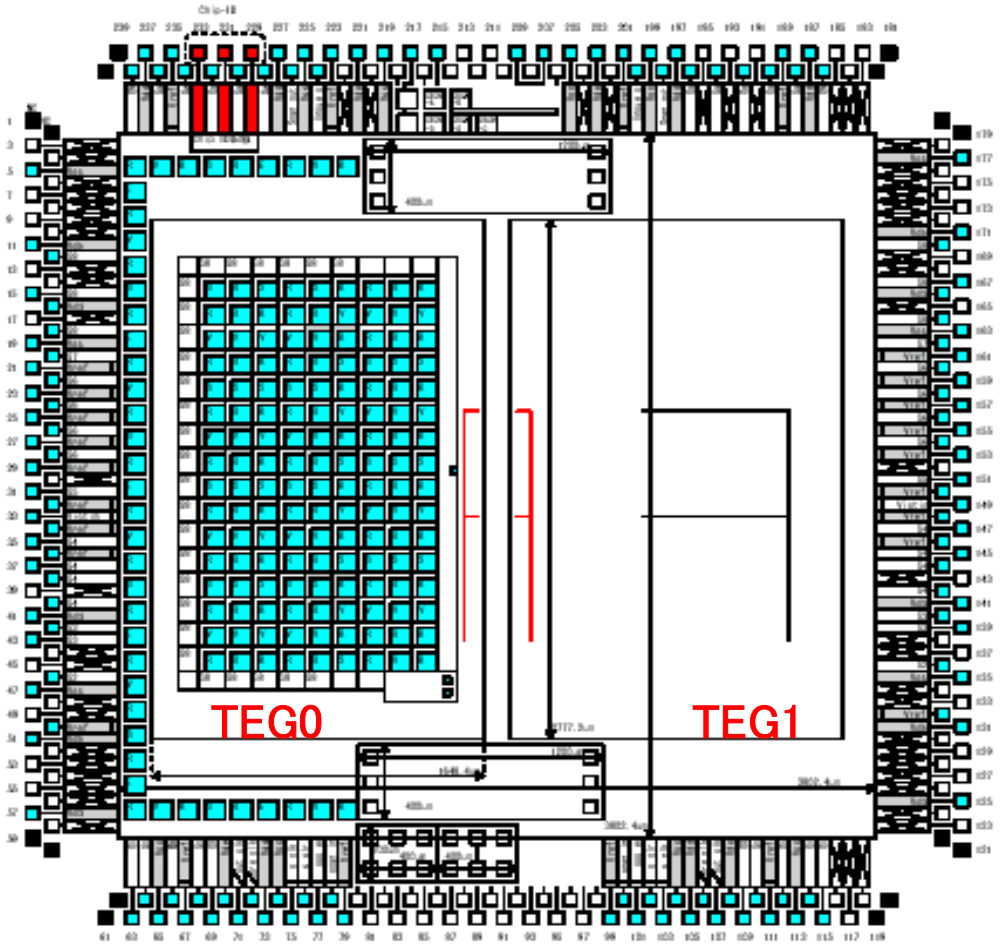
EMI analysis → **EMC**

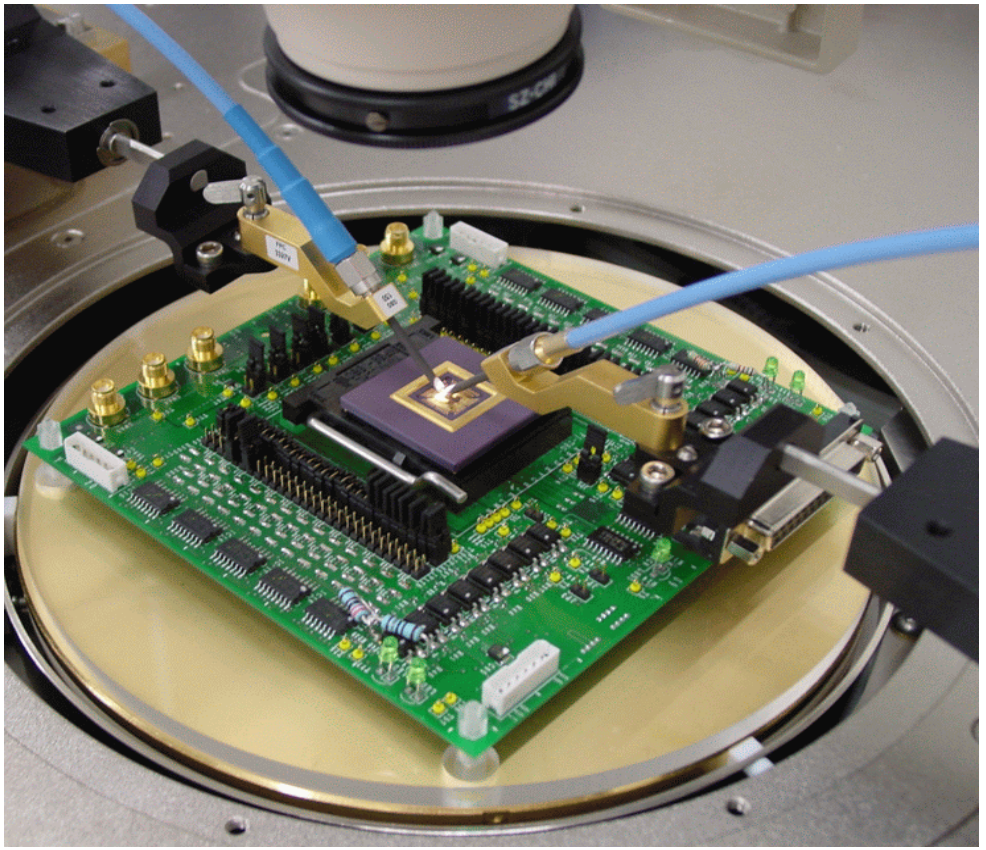


4. LSI,PCB Unified Noise Analysis

Evaluation results of analysis accuracy

Accuracy of V/G noise analysis by evaluation LSI and PCB





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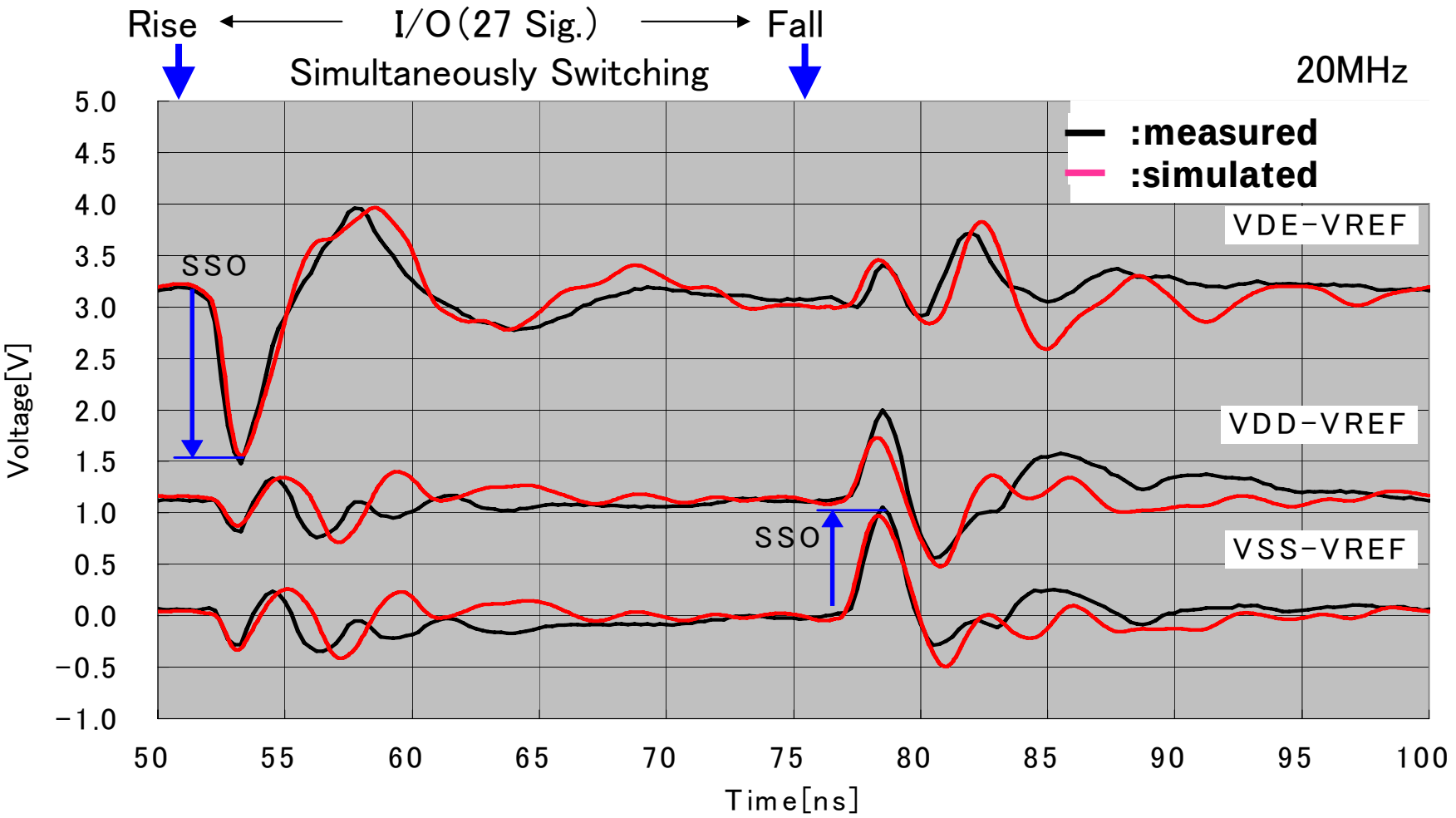
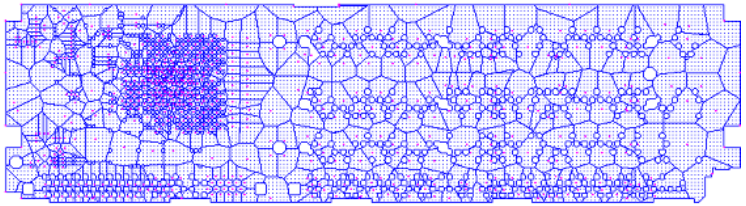


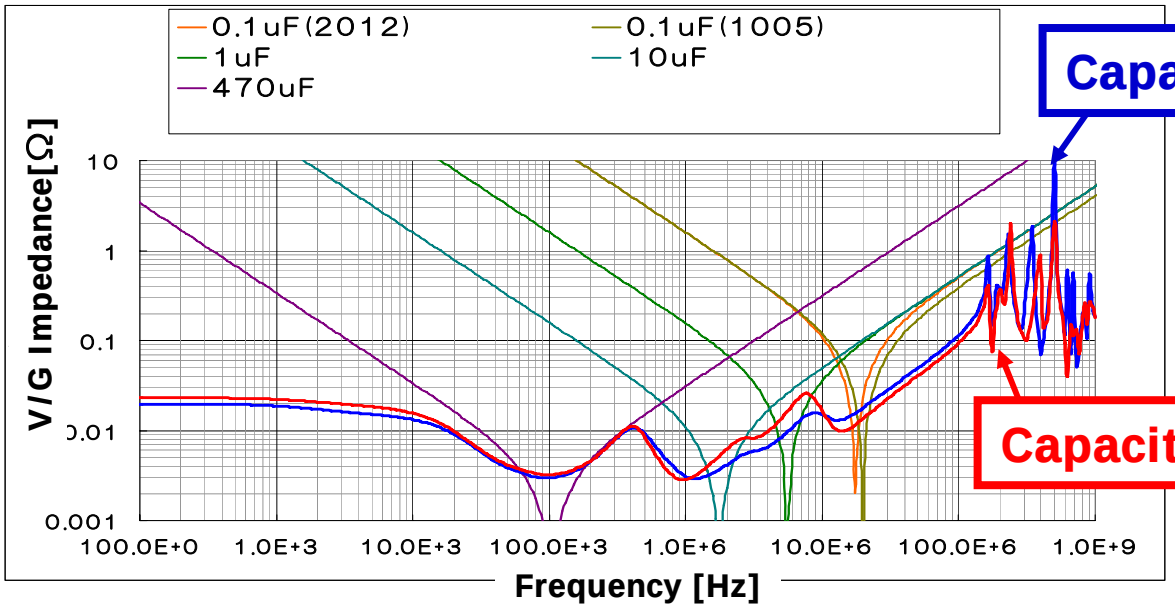
5. Application Results

Example of V/G Impedance Analysis

V/G mesh model



Results of V/G Impedance Analysis



Capacitors around LSI

Capacitors on backside of LSI

5. Application Results

V/G Impedance Calculation Results of Various PCBs

No.	PCB size (cm^2)	Number of PCB layer	Calculation time (HH:MM:SS)
1	106	6	0:01:24
2	43	6	0:26:19
3	1036	12	0:20:03
4	1398	12	3:08:13
5	1061	22	7:57:53
6	2184	22	25:07:02

5. Application Results

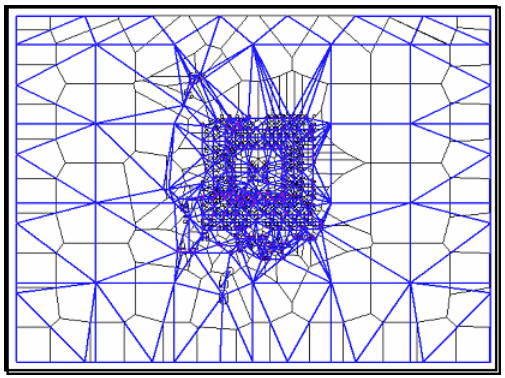
V/G Impedance Analysis Using Floor Planner

Analysis Model

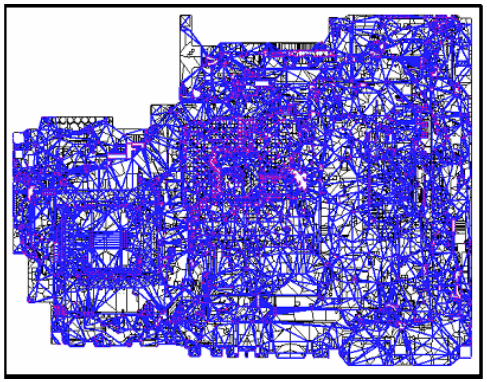
【Specification of Analyzed PCB】

PCB size (cm^2)	Number of PCB layer
180	10

【Using Floor Planner CAD Data 】



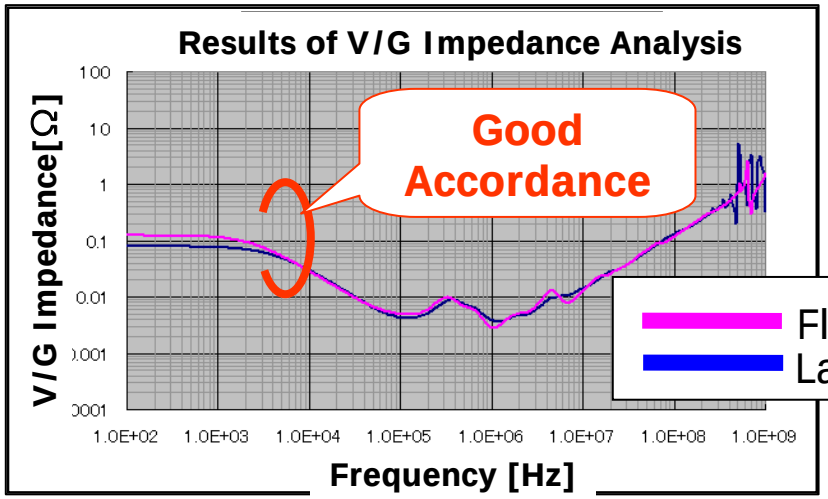
【Using Layout CAD Data】



5. Application Results

V/G Impedance Analysis Using Floor Planner

Analysis Result



Calculation Time

(HH:MM:SS)

CAD Data	Model Size	Calculation Time
Floor Planner	2MB	0:01:37
Layout CAD	50MB	4:52:00

x180 faster

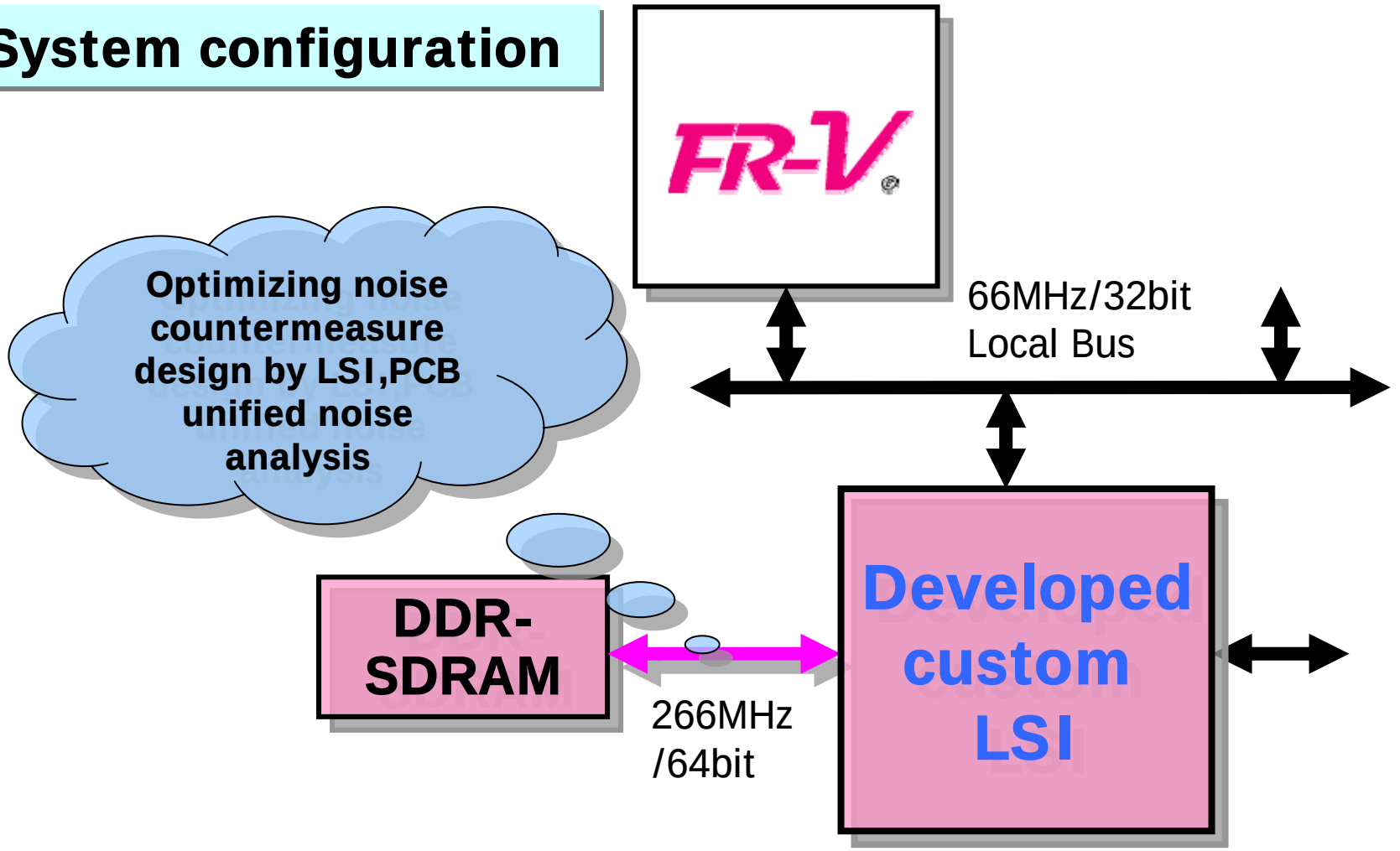
Power noise countermeasure from floor planning stage enables us to easily determine Power design constraint.

(Decoupling capacitors,V/G layer construction,V/G layer partition)

5. Application Results

Example of LSI,PCB Unified Noise Analysis

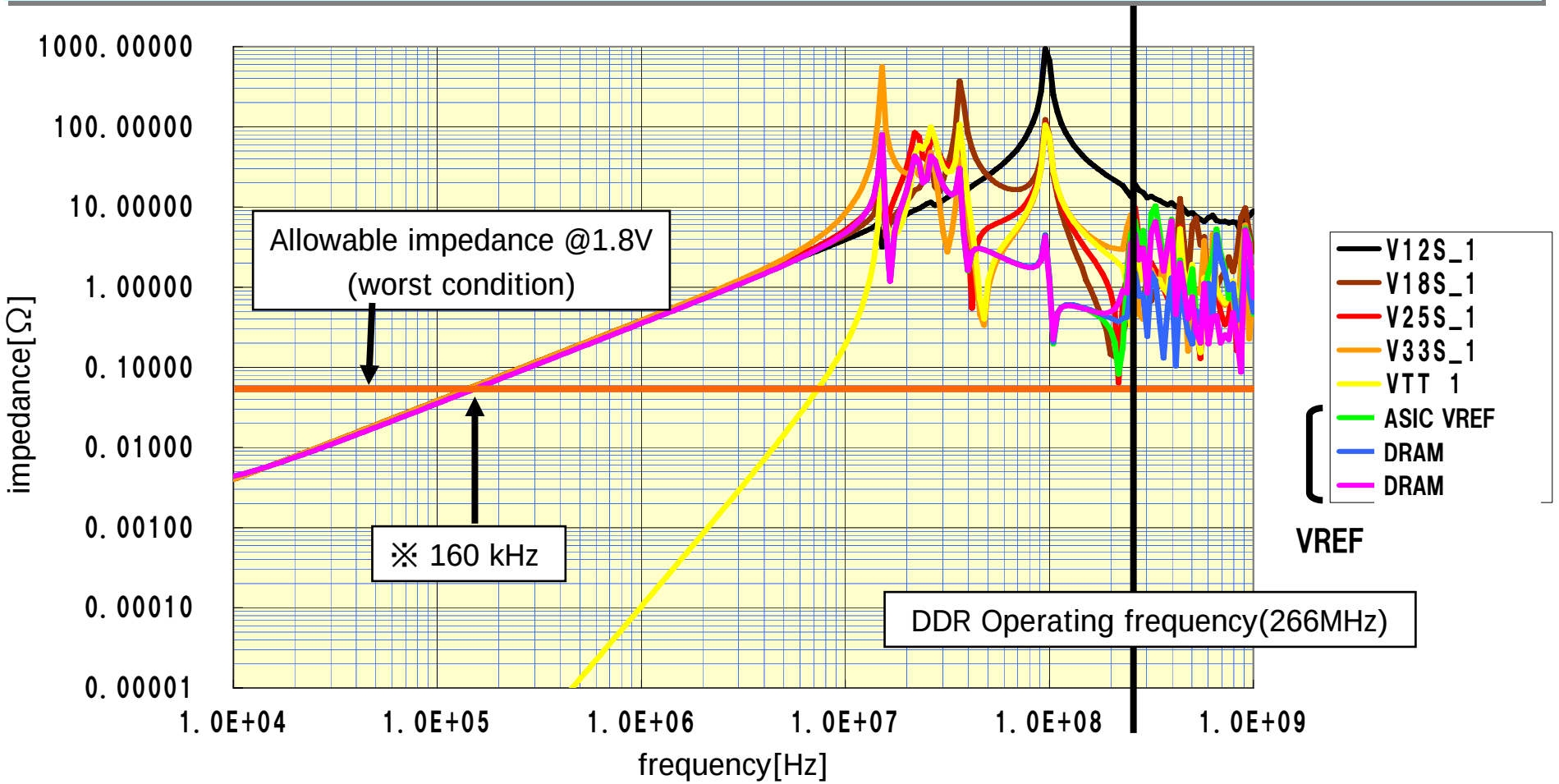
System configuration



5. Application Results

Example of LSI,PCB Unified Noise Analysis

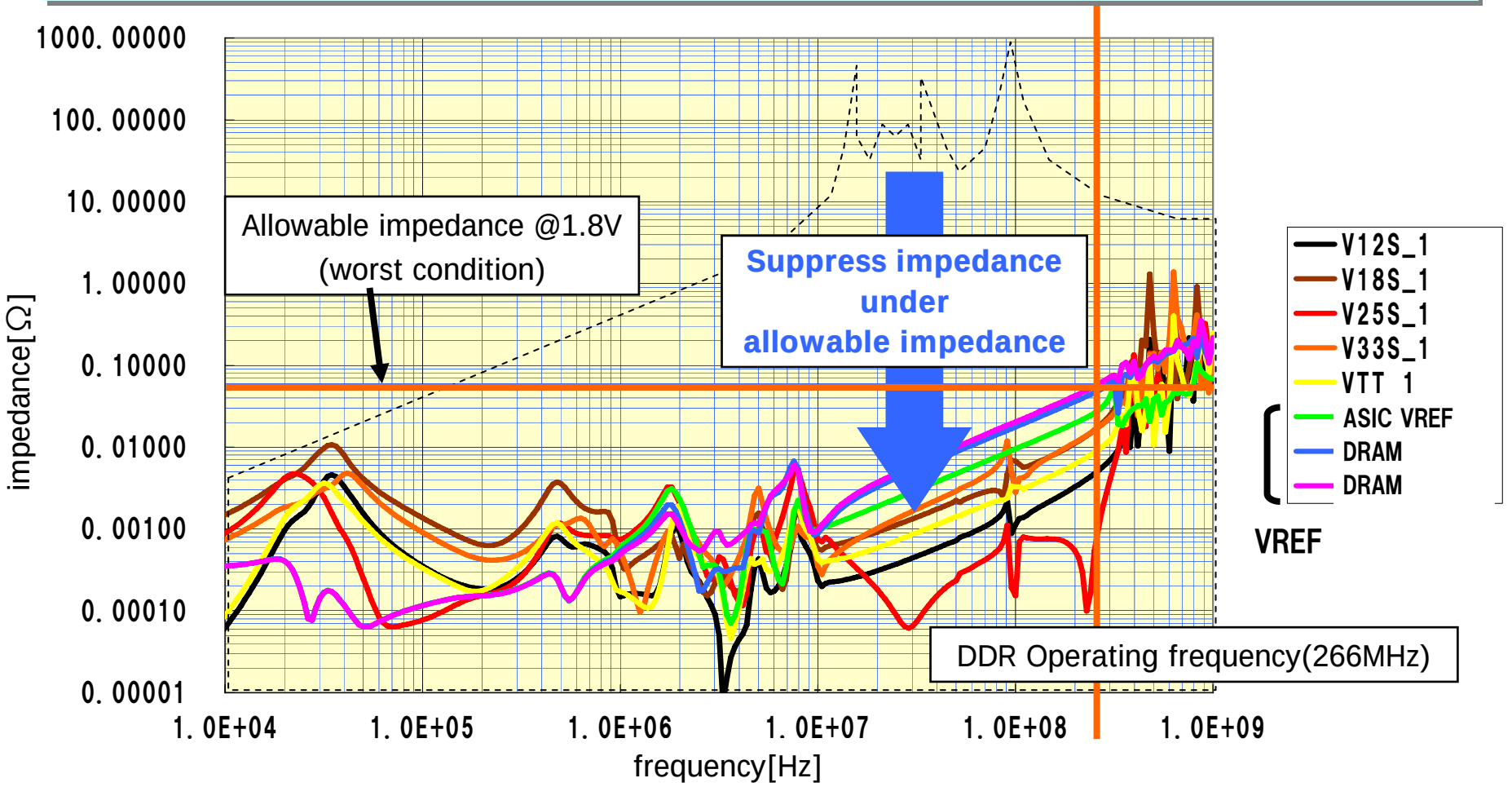
V/G impedance analysis (without decoupling capacitors)



5. Application Results

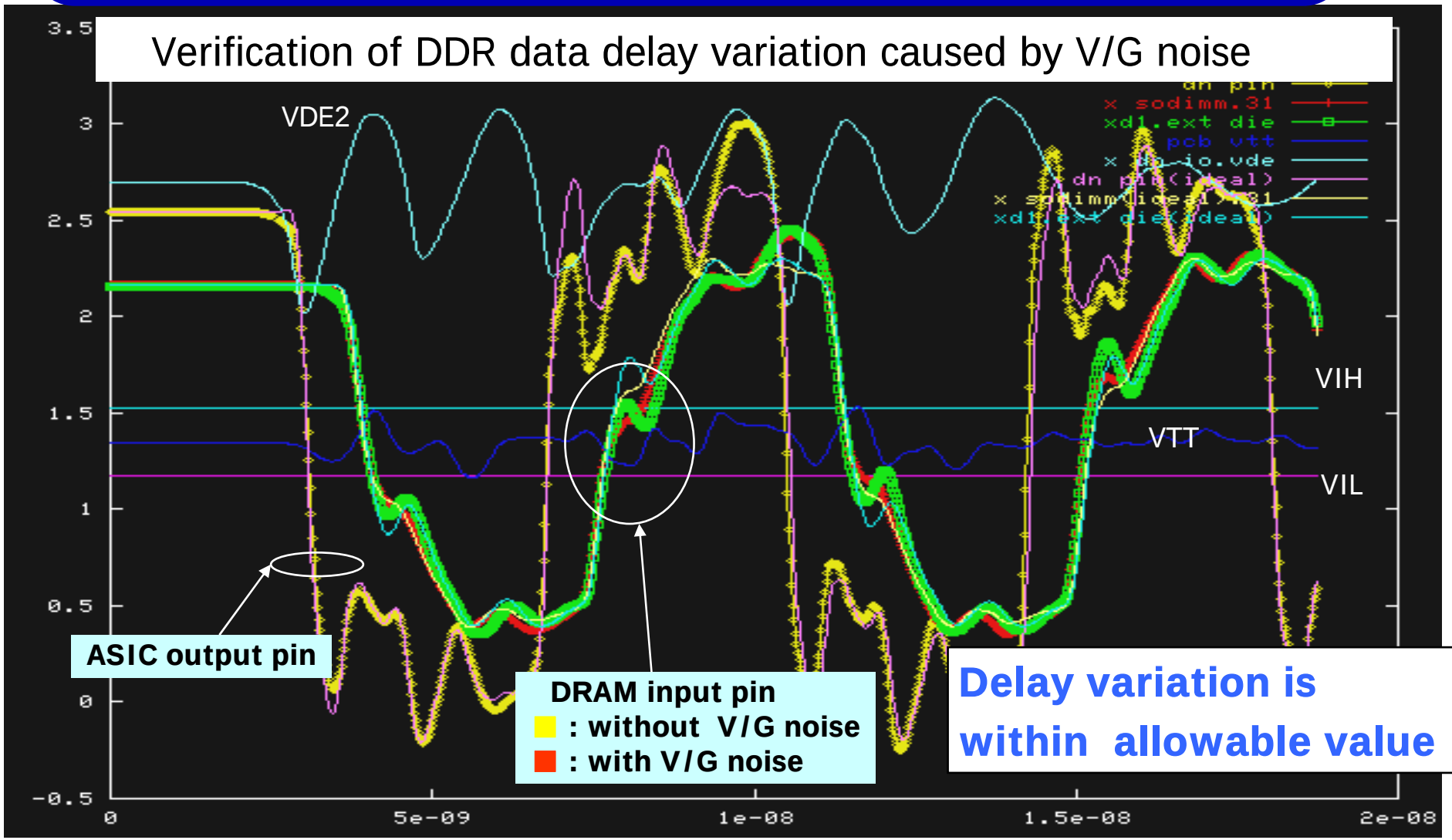
Example of LSI,PCB Unified Noise Analysis

V/G impedance analysis (with decoupling capacitors)



5. Application Results

Example of LSI,PCB Unified Noise Analysis



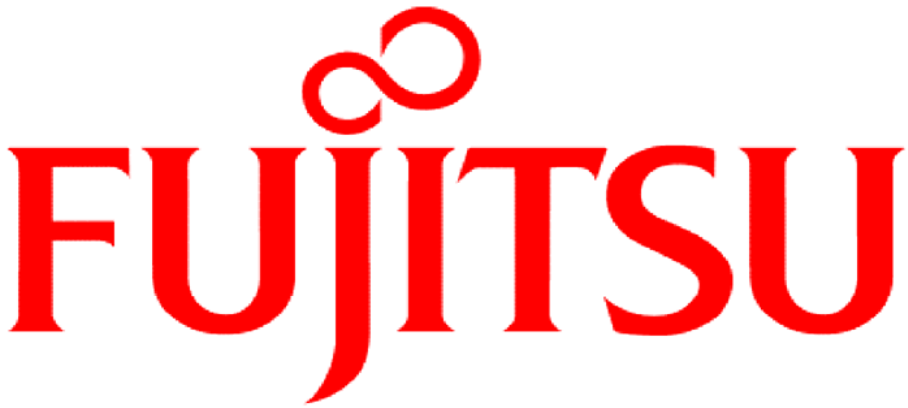
6. Conclusion

- Fujitsu's LSI,PCB Unified Noise Analysis System were introduced and the effectiveness of the system were explained.

- Further developments of the noise countermeasure design system to overcome the rapid advances of technology are scheduled.

7. Future Tasks

- The LSI,PCB Unified Noise Analysis Technology has been established as explained today. But,it is difficult to obtain the various LSI models available for power noise analysis (DDR,FPGA,ASIC,ASSP ・・・).
- Sufficient supply of LSI power noise models are required.
- It is one of the most desirable solutions for this problem that the standard IBIS models available for power noise analysis are widely supplied by LSI vendors.
- We hope IBIS Forum and JEITA will promote to establish the standard IBIS model for power noise analysis and spread it widely as a future task.



THE POSSIBILITIES ARE INFINITE