

Easy IBIS model handling with Simulation Kit

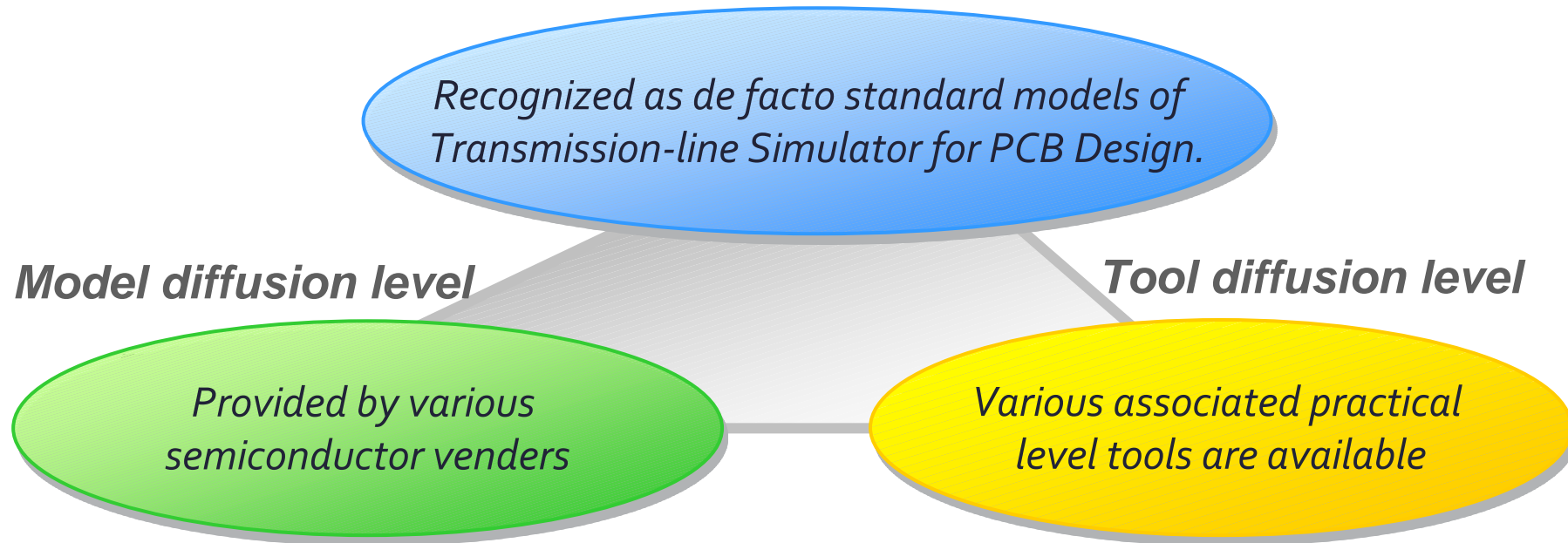
ZUKEN Inc.

High-speed Solution Center

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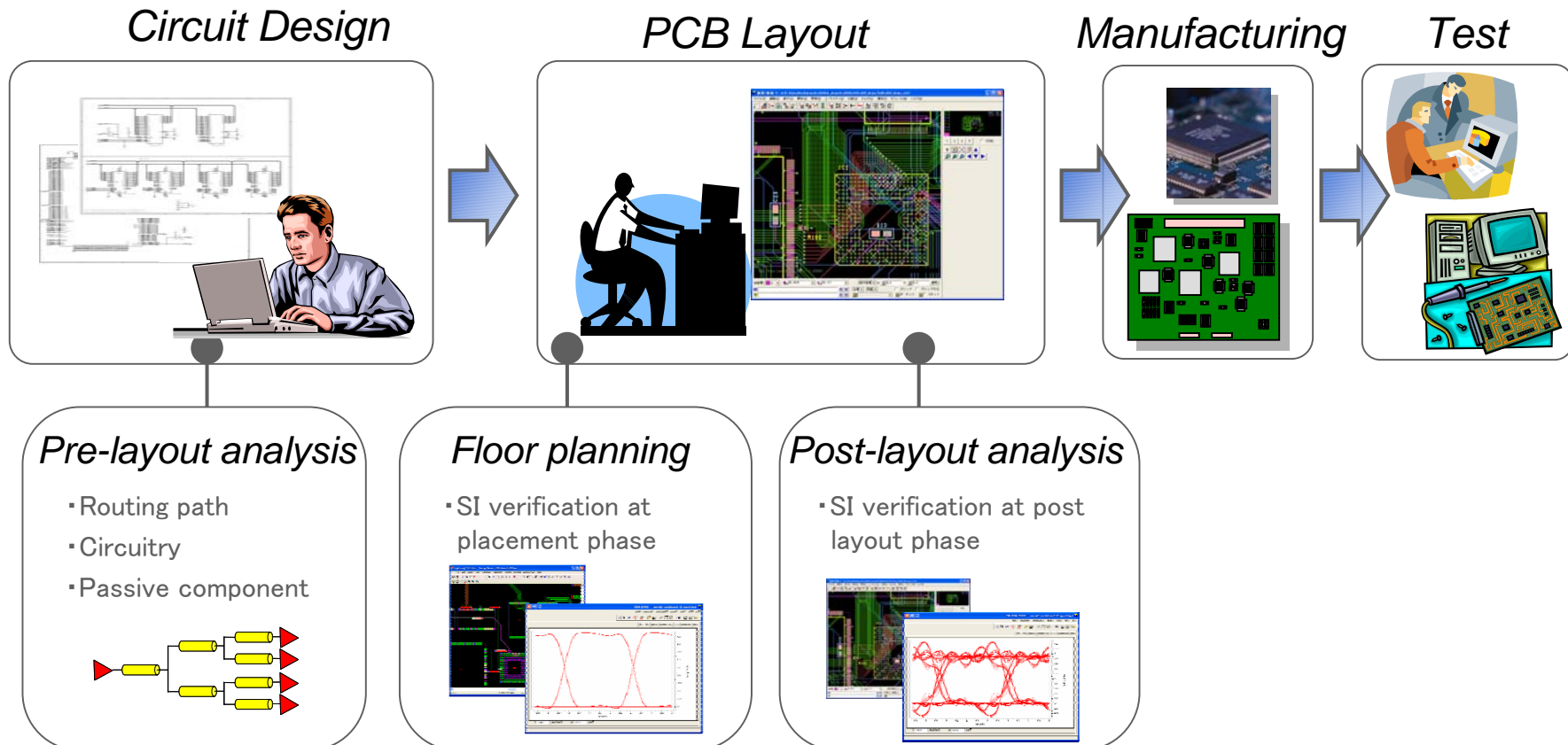
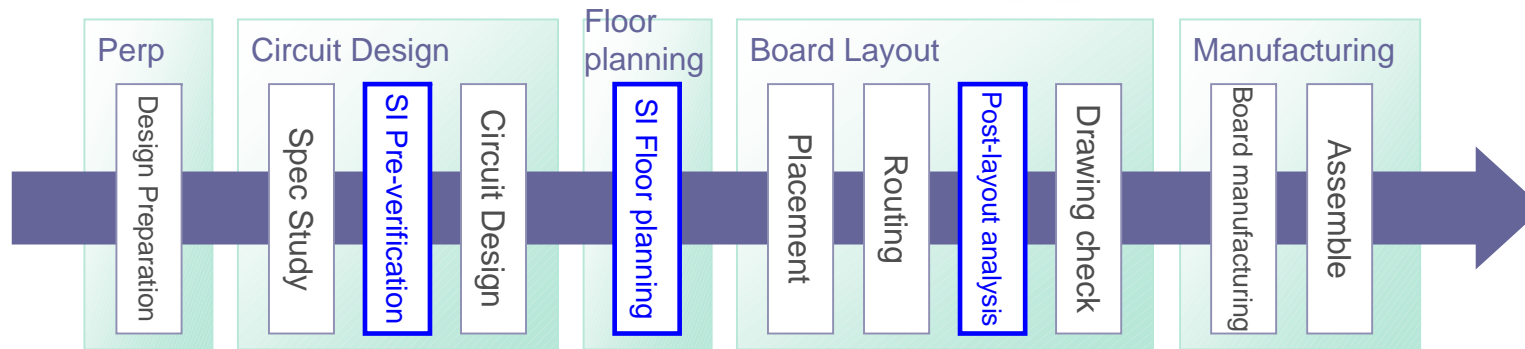


The visibility of IBIS



Looking overall, IBIS environment is thoroughly satisfied.

IBIS Simulation Flow



- *Division-of-roles type usage i.e. Operation by **Full-time Analysis Engineer** is very common.*
- *Operation by **Normal Designer** is much less common (different from each customer).*



Why?

Investigate the cause by listening to the designer's voice...



Let's use Simulator!

Obtain Models

Import Models

Simulation Setup

⋮

Execute Simulation

I cannot use the simulator at once due to a complex preparation work!

I have no idea if I can ignore the various messages which appear during IBIS import.



Are the models set correctly by this operation?



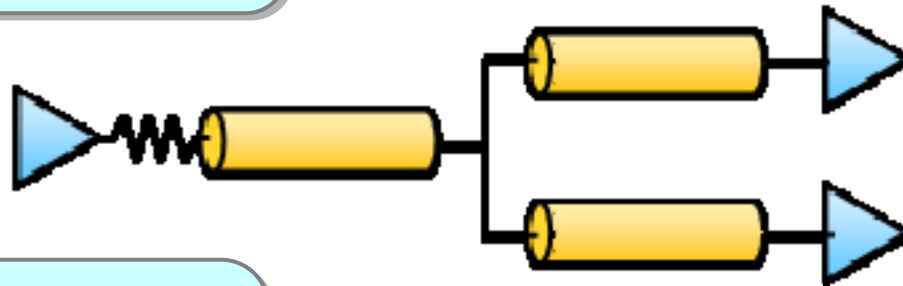
I don't understand well how to setup the Simulator.

Required preparation task for analysis



*Stimulus setting
(Input pulse pattern)
66, 133, 200MHz, etc.*

*Circuit data creation
LVDS, LVTTTL, SSTL, etc.*



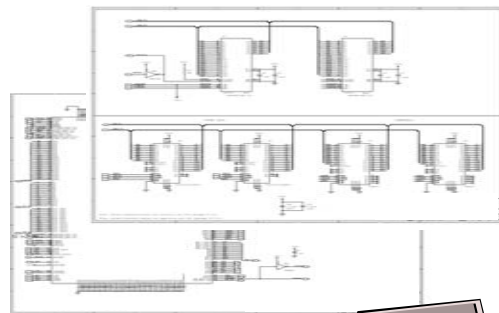
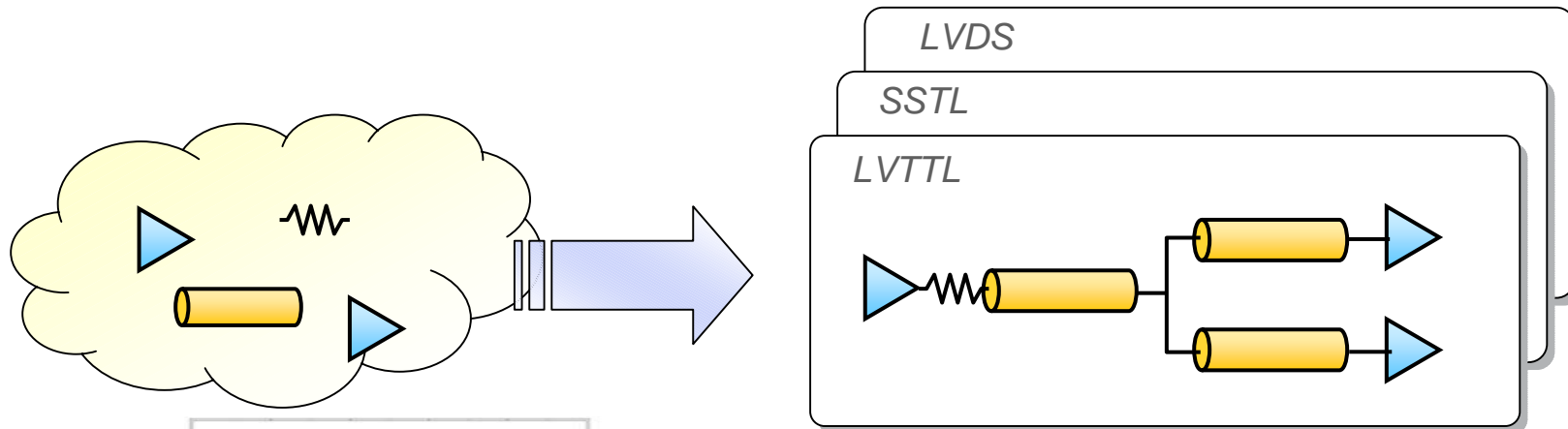
IBIS model preparation
- Import
- Check
- Assignment

*TL model preparation
Strip, Micro Strip,
Differential pair*

*Complicated preparation task can be reduced by
providing these initial templates.*

What Simulation Kit solves

Create the circuit data for analysis purpose



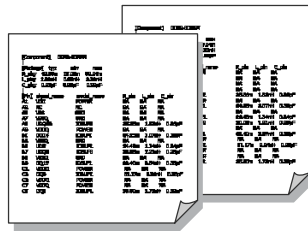
I don't remember the operation well, hence it is tough to create it from scratch.

Provide the circuit data for analysis corresponding to various I/O buffers.

What Simulation Kit solves

Preparation of IBIS models

Model Import



Check

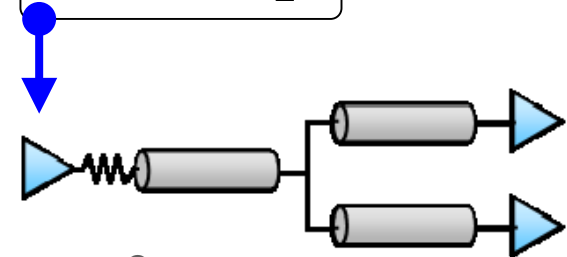
IBIS Checking
Warning
Warning
Warning

*What's meaning of this warning message?
Are there any problem with Models?*

It is painful to set up the models one by one.

Assignment

Driver: SSTL18_I



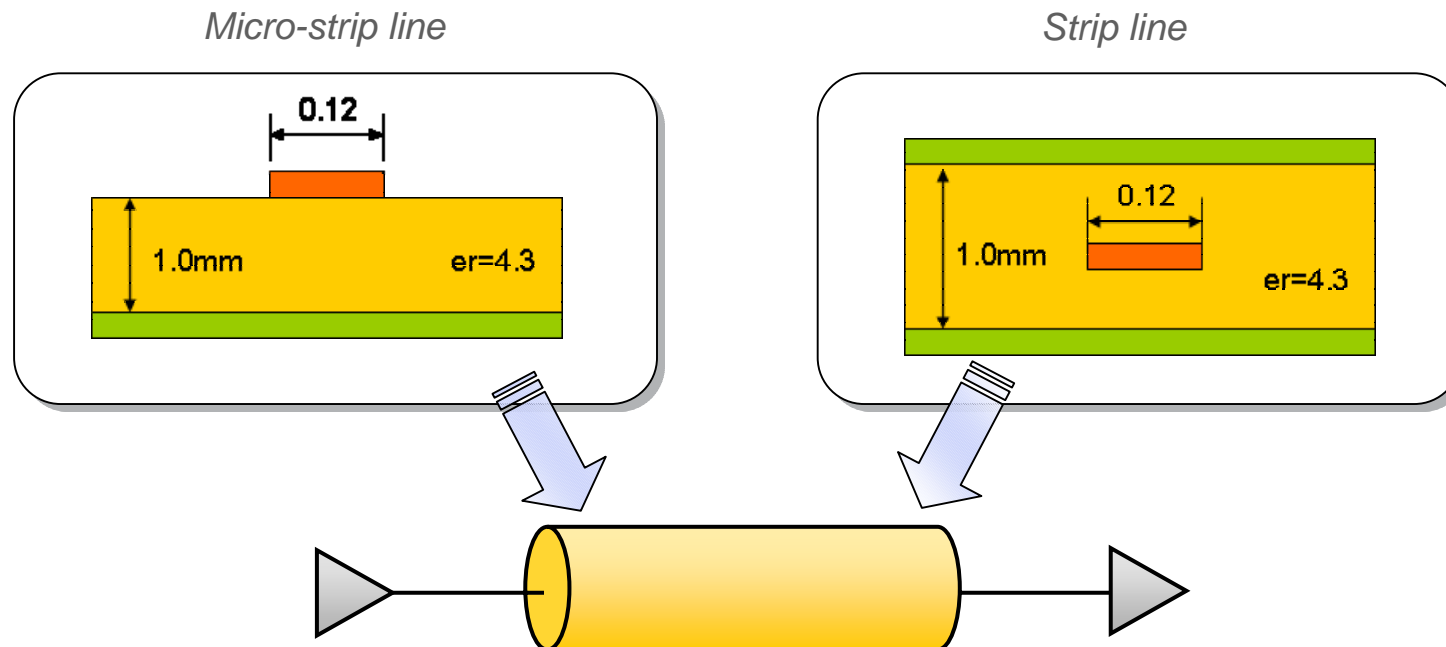
Receiver: SSTL18_I

All processes from the model import to the model assignment are implemented in advance.

What Simulation Kit solves

Preparation of Transmission Line Model

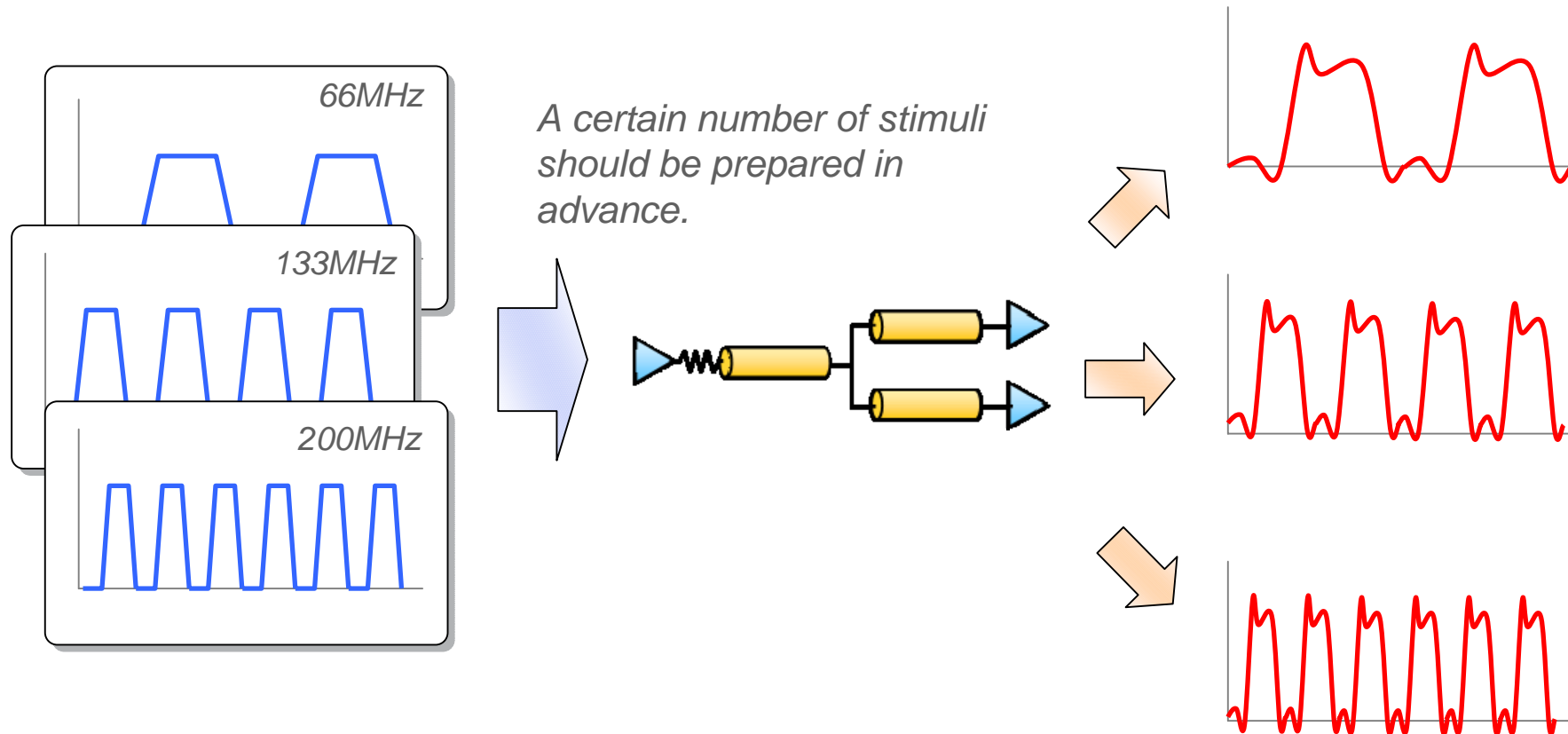
*TL model preparation also takes time.
Provide the template or something is required.*



Template of the cross-section models of the transmission line is pre-defined.

What Simulation Kit solves

Setup of stimulus (input pulse pattern) for Simulation



Several Templates of stimulus for simulation are predefined.

Contents of Simulation Kit



Circuit data for analysis

Stimulus template

TL model template

Simulation model

Include all information required for Simulation.

| Line | No. | Type | Offset (mm) | Width (mm) | Weight (mm) | Thickness (mm) | Material | Resistance (Ohm/m) | Inductance (nH/m) | Velocity (mm/ns) |
|-------|-----|-----------|-------------|------------|-------------|----------------|-----------|--------------------|-------------------|------------------|
| DL324 | 1 | Rectangle | 0.1524 | 0.127 | - | 0.0762 | Al Copper | 0.0175 | 0.157 | 0.18 |
| DL324 | 2 | Rectangle | 0.1778 | 0.127 | - | 0.0762 | Al Copper | 0.0175 | 0.157 | 0.18 |

| Name | Kind | Type | Information |
|-----------------------|--------|-------|--|
| 3S_LVTL18_4mA typ.in | Buffer | IOIn | Vcc=3.3 V, Ri=7.26e+005 Ohm, Ci=6.38e-012 F, Tec= |
| 3S_LVTL18_4mA typ.out | Buffer | IOOut | Vcc=3.3 V, Tec=UK, Derived from [File name] sparta |
| 3S_LVTL18_6mA typ.in | Buffer | IOIn | Vcc=3.3 V, Ri=7.26e+005 Ohm, Ci=6.38e-012 F, Tec= |

Simulation Kit Release History



- 17-Oct-2006 Release the Kit for Altera Stratix II FPGA*
- 13-Sep-2007 Release the Kit for Altera Arria GX FPGA*
- 17-Oct-2007 Release the Kit for Xilinx Virtex-5 FPGA*
- 20-May-2008 Release the Kit for Altera Cyclone III FPGA*
- 10-Oct-2008 Release the Kit for Xilinx Spartan-3 FPGA*

We are continually expanding the simulation kit to promote the utilization of the simulator by the designer.