EIA IBIS Open Forum Minutes

Meeting Date: **November 14, 2008**

GEIA STANDARDS BALLOT VOTING STATUS
See last page of the minutes for the voting status of all member companies.

VOTING MEMBERS AND 2008 PARTICIPANTS

Actel	(Prabhu Mohan)
Agilent Technologies	Sanjeev Gupta, Radek Biernacki, Amolak Badesha Fangyi Rao, [Ian Dodd], Yutao Hu, Vuk Borich Nobutaka Arai, Ludwig Eichingner, Cheng-ming Ren, Xuliang Yuan, Jianping Zhu
AMD	Nam Nguyen, Tadashi Arai*
Ansoft Corporation	Steve Pytel, Ricardo Teliuteuesh, Dan Dvorscak, Steele Deng, Donny Hou, Baolong Li, Davis Yan, Long Yang, Song Zheng, Kazuhiro Kadota*, Mitsuyo Kawata*, Toru Watanabe*
Apple Computer	(Bill Cornelius)
Applied Simulation Technology	(Fred Balistreri)
ARM	(Nirav Patel)
Cadence Design Systems	Terry Jernberg, Hemant Shah, Ambrish Varma [C. Kumar], Brad Griffin, Zhen Mu, Lanbing Chen, Wenliang Dai, Feng Li, Shirley Li, Jinbai Liu, Ping Liu, Yabao Meng, Jian (John) Peng, Jain Shan, Hui Wang, Yitong Wen, Yitong Wu, Dingru Xiao, Ke (Coco) Xu, Feng Yu, Rong Zhang, Wenjiang Zhang, Alex Zhao, George Zhou, Yukio Masuko*, Morihiro Nakazato*, Norikazu Takada*
Cisco Systems	Syed Huq, Mike LaBonte, AbdulRahman (Abbey) Rafiq Huyen Pham, Emily Yao, Susmita Mutsuddy John Fisher, Paul Ruddy, Jun Li, Jianmin Zhang Luis Boluna, Kelvin Qiu, Jane Lim, Ilyoung Park Rick Brooks, Chris Padilla, Ehsan Kabir, Jin (Leo) Hu, Weifeng Shu, Xinghai (Sean) Tang, Huihui (Iris) Zhao
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Freescale	Jon Burnett
Green Streak Programs	Lynne Green
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	Wen Yu, Cheng Zhang, Gezhi Zhang, Yuehui Zhu
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Infineon Technologies AG	Christian Sporrer
Intel Corporation	Michael Mirmak*, Rich Mellitz, Wei-hsing Huang Vishram Pandit, Lili Deng, Haifeng Gong, Fanghui Li, Wenjie Mao, Yang Qu, Yiunglei Ren, Wayne Tsuchimoto, Yang Wu, Maoxin Yin, Xinjun Zhang, James Zhou, Nanditha Rao*
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Mentor Graphics	Arpad Muranyi, John Angulo, Minggang Hou, Jane Liao, Xuefeng Liu
Micron Technology	Randy Wolff*
Nokia Siemens Networks GmbH	Eckhard Lenski, Klaus Huebner, Katja Koller, Xianyun Wang
Samtec	Jim Nadolny, Justin McCalister
Signal Integrity Software	Mike Steinberger, Walter Katz, Todd Westerhoff Doug Burns, Mike Mayer, Barry Katz
Sigrity	Sam Chitwood, Brad Brim, Ben Franklin Kristopher Stytte, Raymond Chen, Jiangsong Hu, Xianfeng Li, Tao (Helen) Xu
Synopsys	Ted Mido, Xuefeng Chen, Wenyun Gu, Jinghua Huang, Deng Shi
Teraspeed Consulting Group	Bob Ross*, Tom Dagostino, Al Neves
Texas Instruments	Richard Ward, Pavani Jella
Toshiba (I.S. Corporation)	Yasumasa Kondo, Noriyasu Yoshikawa*, Yoshihiro Hamaji*, Atsushi Osaki*
Xilinx	David Banas*, Ajay Shah, Suzanne Yiu Mustansir Fanaswalla
Zuken	Michael Schaeder, Ralf Bruening, Shigeru Hayashi*, Hirohiko Matsuwawa*
ZTE	Huifeng Chen, Xiaolin Chen, Jinku Guan, Hui Jiang, Nan Jiang, Shiju Sui, Zhiwei Yang, Shunlin Zhu

OTHER PARTICIPANTS IN 2008

3M	Kylin Chen, Shiang Yao
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AET	Mikio Kiyono*
Aica Kogyo	Akihiro Tanaka
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Alcatel-Shell	Weiping Chen, Feng Ji
Altera	Ravindra Gali, Jing Wu, John Oh, Hui Fu
ATE Service Corporation	Hideaki Endo*, Yutaka Honda*, Kevin Iida*, Hiroyuik Itabashi*, Kenji Kagawa*
Avago Technologies	Minh Quach, Sari Tocco

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EFM	Ekkehard Miersch
Elma Bustronic	Michael Munroe
Exar	Helen Nguyen
Feng Hao Shanghai Information	Zhengchang Gu
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Flextronics	Hasnain Syed
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Hisense Electronic	Haishi Hu
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Nuova Systems	Zhiping Yang
Nvidia Corporation	Baal Yang, Tibet Zhao
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TDK	Yoshikazu Fujishiro*
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TietoEnator GmbH	Heinz-Hartmut Ibowski
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Tyco Electronics	Chad Morgan
Universal Scientific Industrial	Lurker Li, Spenser Tang
VeriSilicon Microelectronics	Qiang Chen, Steven Gou, Zhiying Yuan
Vertical Circuits	Mark Egbers
Victor Corporation of Japan (JVC)	Manabu Matsumoto*
Winwin Corporation	Haiphe Lau, Linfa Liu
Xsigo Systems	Robert Bada
Zuken Support and Service	Seikou Go*, Yoshiaki Nishi*, Tomotaka Unose*, Yin Yi*
Independent	Guy de Burgh, Ardy Forouhar, Dave Galloi Kazuhiko Kusunoki

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS summits teleconferences are as follows:

Date	Telephone Number	Meeting ID
November 21, 2008	1-866-432-9903	121522040

All meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, provide the bridge number and passcode at the automated prompts. If asked by an operator, please request to join the IBIS Open Forum hosted by Michael Mirmak. For international dial-in numbers, please contact Michael Mirmak.

NOTE: "AR" = Action Required.

GENERAL ANNOUNCEMENT

Kazuyoshi Shoji made an announcement showing a list of the meeting sponsors and introducing the event schedule. Yutaka Honda of the JEITA TCS working group welcomed the

IBIS members and thanked them for attending.

WELCOME AND KEYNOTE COMMENTS

The IBIS Open Forum Summit was held in Tokyo, Japan at the JEITA offices. About 61 people representing 28 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda.org/pub/ibis/summits/nov08b/

Takashi Watanabe of NEC Electronics began the meeting shortly after 9:30 AM and made brief comments to welcome the participants.

Michael Mirmak made brief remarks and opened the meeting. He thanked JEITA for hosting the event as well as all the co-sponsors including Agilent Technologies, Ansoft, ATE (Sigrity), Cadence Design Systems, Cybernet Systems, Fujitsu and Zuken.

JAPAN IBIS ACTIVITIES UPDATE

Kazuyoshi Shoji, Hitachi ULSI Systems

Kazuyoshi began with a brief introduction to IBIS models. He showed the relationship of the IBIS Committee within the ITAA/GEIA structure. He then introduced the IBIS board members. He detailed the JEITA EC center objectives, operations, members and focus. He showed the history of the Japan IBIS summit and mentioned suspension of work on an IBIS guidebook. An IBIS quality presentation has been made at two conferences this year. Interconnect modeling is being studied.

MICRON'S IBIS MODEL QUALITY PROCESS

Randy Wolff, Micron Technology

Randy highlighted that building a quality IBIS model involves building quality checks into each step of the model creation process. A quality IBIS model begins with a quality SPICE model. Including multiple pre-driver stages ensures that the model input stimulus does not affect the output slew rate and timing. Critical timing paths should not be modified. Micron has two choices of netlists for inclusion of layout parasitics. An RC netlist provides the best match to silicon but is a much larger netlist than a C-only netlist. A good compromise is to use a C-only netlist but add RC models on critical nets to match timing delays of long metal lines. The resulting netlist shows good correlation to the RC netlist when looking at rising and falling waveform crossing voltage, Vox. C_comp minimum and maximum corners should be adjusted to match the range seen from silicon measurements including the package. When correlating I-V curves to measurements, voltage and temperature are easy to adjust, but it is more difficult to know how to adjust the transistor process model to match the silicon. Randy detailed a method for adjusting the process model to match the silicon. Detailed checklists should be used during both the SPICE and IBIS model creation processes. Example checklists were shown. Randy mentioned the importance of the IBIS Quality task group's work. Micron releases a detailed report with each IBIS model comparing the model to specification data and measurement data and comparing the IBIS model to the SPICE model. Randy showed an example of Micron's

quality report. He concluded that model users should demand quality models from vendors and show them examples of quality models.

A question was asked about whether the comparisons to measurements were of a transistor device or the actual buffer. Randy responded that the measurements were of the actual buffer. Another question was if he measured devices across voltage and temperature as well as process? Randy responded that typically he gets measurements at two voltage-temperature corners, but rarely measurements showing much process variation. Another question was how you know what process corner you have in measurement and how to get all the process corners. Randy said that he is able to determine the process corner based on measurements of other devices on the same wafer, and it is difficult to get measurements of all process corners. The final question was how do you guarantee your model covers the worst case corners, and is it important to test the device with test fixtures showing large board variation? Randy answered that the transistor models are created by a group within Micron that measures a large sampling of wafers, so the full process variation is included within the slow and fast corners of the model. Randy also thought that it would be a good idea to test the device with multiple test fixtures.

IBIS QUALITY ACTIVITIES IN JEITA EDA WG

Yoshihiro Hamaji, Toshiba I.S. Corporation

Yoshihiro noted that IBIS models are essential for transmission line signal simulation. Accurate IBIS models are required. IC vendors supply IBIS models, but they rarely mention the accuracy of the model. Model users sometimes do not know how to use the model with their simulation software. EDA vendors can interpret the IBIS data in their own way. There have been many presentations on IBIS model quality in recent years. All of the issues mentioned make it difficult for the IC vendors to deal with simulation issues their customers have, even after exactly duplicating the simulation environment of the customer. JEITA is focusing on fixing the quality issue through an IBIS model distribution system. The JEITA IBIS Quality SWG is establishing a base for discussion between EDA vendors, model creators, and model users. The group has defined many test circuits used to compare simulation data with IBIS Golden Waveforms. Six companies in the working group take part in this activity using seven different simulators. Results were shown of this activity. Yoshihiro described the process JEITA is working on for distribution of quality models. An open website is used in the process. JEITA is in the process of checking the validity of the established framework and hopes that many simulator vendors will take part in the activity. Verification and validation are going to be very important for ISO9001 in the near future.

LOOK INTO IBIS BUFFER CURVES

Lance Wang, IO Methodology

Lance reviewed the circuit elements of a basic I/O buffer. He then related these elements to their corresponding I-V curves in IBIS. He noted that all I-V curves are related to specific voltage references and showed examples of I-V curves for high, low and open buffer states. He overlaid load lines on the I-V curves. The voltage point where the load line intersected to the [Pullup] or [Pulldown] I-V curve corresponded to the endpoint voltage found in the V-t curves of the same load. He discussed the importance of maintaining timing relationships between the V-t curves. [Submodel] I-V curves were shown to demonstrate how to model on-die termination characteristics.

A question was asked about how to handle LVDS models. Lance responded that the I-V curves look different, so different test loads must be analyzed to look at the differential currents.

EASY IBIS MODEL HANDLING WITH SIMULATION KIT

Hirohiko Matsuzawa, Zuken

Hirohiko noted that the IBIS environment is well developed with many tools and models available and good visibility. The IBIS simulation flow starts with circuit design and SI pre-verification, continues with SI floor planning and ends with post-layout analysis. Use of models by full-time analysis engineers is very common, but operation by normal designers is much less common. Designers cannot use simulators easily due to complex preparation work and limited understanding of IBIS models. Complicated preparation tasks can be reduced by providing initial setup templates in simulation kits. The simulation kits provide circuit data for analysis of various I/O buffers. All processes from the model import to the model assignment are implemented in advance. Templates for cross-section models of the transmission lines are pre-defined as well as various input stimuli waveforms. Kits should include all information required for simulation. Zuken has released several kits for FPGAs to promote utilization of the simulator by the design engineer.

NEW TABLE-BASED MODELS IN IBIS 5.0, A COOKBOOK-STYLE GUIDE

Michael Mirmak, Intel Corporation

Michael began with a summary of IBIS development. He noted two new table-based keywords in IBIS 5.0. BIRD98 introduced [ISSO_PD] and [ISSO_PU] and BIRD95 introduced [Composite Current]. A cookbook style method was demonstrated for extracting the [ISSO_PD] and [ISSO_PU] data from a buffer. He stressed the importance of excluding diode clamp current from ISSO tables (including on-die termination effects). He noted that the ISSO keywords do not describe the pre-driver stage and describe static current modulation. The [Composite Current] data should include tables using the same load as the V-t tables and be time correlated to the V-t tables. The power delivery structure must be complete including buffer rail inductances and resistances, pre-driver structures, and on-die decoupling structures. He summarized that model makers should start collecting this data now and encourage the EDA tool providers to support these keywords.

The first question noted that IBIS models are correlated well to measurements already, so to include ISSO keywords, how does one de-embed the data from measurement data. Michael responded that ISSO is easy to extract from simulation data. To get from measurement data, one must remove resistive effects from the package. Also, collect the measurement data very slowly to remove the parasitic effects in the path and also take into account how many buffers are in parallel. A second question asked if the parasitics of the rail voltages are only on-die parasitics or inclusive of the package. Michael noted that this is only on-die parasitics. A follow-up question asked if the sweep voltage for [Composite Current] is from –VCC to VCC or to 2*VCC? Michael responded that the range of most interest is –VCC to VCC, as the clamp region is not of interest. Bob Ross commented that the rail parasitics included would be the same as included for V-t waveform extraction.

TOUCHSTONE VERSION 2.0 MIXED-MODEL SYNTAX - UPDATED

Bob Ross, Teraspeed Consulting Group

Bob noted that terms used in Touchstone include SE for single-ended, MM for mixed-mode and GMM for generalized mixed-mode. The original Touchstone was issued in 1984. Touchstone version 2.0 is extended to remove some format limitations and to add some resistance per port flexibility for PDS applications. Touchstone 2.0 adds eight IBIS-like keywords. Details of the keywords are found in the IBIS summit meeting at DesignCon 2008. Only four of the keywords are required. He showed the differences in block arrangement between Touchstone version 1.0 and 2.0. He highlighted that the new [Mixed-Mode Order] keyword applies to S, Y and Z n-port matrices. Mathematical details are found in the Touchstone 2.0 specification. Examples were shown of converting single-ended data to generalized mixed-mode and mixed-mode data formats. Several EDA tools are already implementing portions of the mixed-mode syntax. He noted that the specification is not yet completed, so minor changes are still being considered.

IBIS EBD MODELING, USAGE AND ENHANCEMENT, AN EXAMPLE OF MEMORY CHANNEL MULTI-BOARD SIMULATION

Tao Xu, Sigrity

Yutaka Honda of ATE Service Corporation (Sigrity) presented for Tao Xu. Yutaka began by showing the typical system memory bus structure for a two DIMM system. Several challenges in memory channel simulation exist including multi-drop topologies, high speed signaling with transmission loss, tighter timing among different signal groups, significant crosstalk and SSO, and model accuracy. He introduced EBDs and noted that they are good for transmission effect assessment and timing analysis for first order considerations. Sections of EBD syntax were shown for a DIMM module address path and for a differential data strobe path. An EBD simulation problem was presented. Yutaka noted that PDS noise was simulated on the motherboard, but the EBD assumes ideal powers and grounds, so much information is lost by using an EBD for the DIMM. Also, crosstalk analysis is incomplete. He recommended enhancing EBD for improvements to crosstalk and power and ground effects analysis. He demonstrated the ability to simulate both power integrity and signal integrity effects for proper SSN analysis and concluded that enhancements are required for EBD.

DE-EMPHASIS BUFFER MODELING ISSUES WITH IBIS

Nanditha Rao, Intel

Nanditha showed the schematic for a PCI Express differential buffer. De-emphasis is added through a second buffer connected in a wired-OR fashion. During de-emphasized operation, opposite legs of the buffer are switched on. The implementation in IBIS is through two differential buffers where the boost is driven by a stimulus derived from the main pattern and C_comp is split between the main and boost models. An example was shown of implementing the boost stimulus in SPICE. Two approaches were shown using various combinations of B-elements, but each approach had problems correlating to the SPICE model for either the single-ended or differential signals. An equation based Verilog-A model was created that showed good correlation. Different de-emphasis implementations will require unique boost stimulus logic. Some alternatives to investigate are use of [Driver Schedule] and an AMS approach.

A question was asked if it is possible to use [Driver Schedule] to control the boost buffer. Nanditha responded that this has been shown before to work. Lance Wang commented that using split C_comp with the B-element may solve some problems and thought that the SPICE macro-model approach could yield a model as good as the Verilog-A model. The next question was if there are any drawbacks with use of the AMS model. Nanditha was not aware of any.

The last question was if she was simulating with Verilog-A or Verilog-AMS. Michael Mirmak commented that most simulation tools implement either a superset of Verilog-A or a subset of Verilog-AMS.

EYE DIAGRAMS IN IBIS

YuBao Meng, Cadence Design Systems

Yukio Masuko of Cadence presented for YuBao Meng. Yukio noted that eye diagrams are very important for SI analysis, but IBIS does not support inclusion of eye mask data in the specification. Including eye mask data in IBIS models would improve design flows by encouraging earlier eye mask checking. Eye mask data added to the specification could represent either standards such as PCI Express or device specific eye limits. Eye masks included for SerDes channel analysis would allow easy checking of interface compliance. For source synchronous channels, the eye mask might relate to setup and hold time limits and be aligned to the clock/strobe. Examples were shown for HDMI, HDMI TP2, source synchronous and common clock eye masks. By including eye masks in the IBIS model, this will promote earlier use of eye masks in the design process and IC vendors might also be allowed to advertise their device-specific, less stringent eye mask requirements.

A question was asked if some specifications may change based on BER targets, would this be included in the proposal. Yukio responded that this should be considered. The next question noted that some eye masks are noted in specifications to be measured at specific locations. Some buffers may need to look at the eye mask after receiver equalization and clock recovery circuits are considered. How would this be handled? Yukio answered that right now this would only support eye masks that would be defined by specification, but one should include eye masks in the IBIS model that are specific to the company's technology. The next question noted that eye masks should be defined based on the CDR circuit unique to the receiver including information on the unit interval sampling, etc. How would this be included? Yukio responded that perhaps one would need to consider specifying a location for the mask, but this is not included in current simulator technology. There was an additional comment to consider inclusion of additional, arbitrary x and y coordinates to define complicated eye masks.

SYSTEM-LEVEL SERIAL LINK ANALYSIS USING IBIS-AMI MODELS

Todd Westerhoff, SiSoft

Lance Wang of IO Methodology presented for Todd Westerhoff. Lance began by detailing requirements for analyzing serial links. Multi-million bit simulations are needed as well as modeling of equalization and clock recovery circuits. IP must also be protected. There are challenges with using traditional SerDes analysis. SerDes vendor tools don't work together and open-source tools lack IP vendor models. IBIS-AMI is a new serial link analysis method and is now part of IBIS 5.0. It divides SerDes simulation into two parts – network characterization and communications analysis. IBIS-AMI models include an analog model and an algorithmic model. Designing a serial link involves a lot of analysis and design decisions. Statistical analysis directly computes eye distributions and is extremely fast. Tap settings are easily optimized for a transmitter to minimize bit error rate. Time domain analysis can be used to model non-linear effects and time-varying behavior including adaptive optimization. The RX DFE model can include adaptive equalization to optimize tap coefficients based on an input data stream. IBIS-AMI models provide significant performance enhancement over SPICE simulation and equivalent performance to proprietary SerDes simulation tools. Comparisons were shown

between an IBIS-AMI model and both SPICE and IBM HSSCDR. The results correlated very well.

NOISE COUNTERMEASURE DESIGN TECHNOLOGY FOR SIGNAL AND POWER INTEGRITY

Toshiro Sato, Fujitsu Advanced Technology

Toshiro noted the increasing data rate of new serial and parallel bus technologies. He also showed the trends of increasing current and power consumption and decreasing supply voltage and gate length. There is an emerging noise problem. Fujitsu has developed a unified analysis environment for signal integrity, large scale power integrity and EMC. For power integrity, it is important to analyze the die, package, PCB, and power supply at the same time. The allowable power/ground impedance is decreasing due to increasing frequency and decreasing supply voltage. A highly accurate power noise analysis methodology is needed. Models of the power distribution system (PDS) of the core and package must be added to previous models that only included models of the PCB and power supply. SI and PI problems are related and should be solved simultaneously. Toshiro detailed the simulation configuration and the model types used for each piece of the PDS. Two operational flows were shown for pre-layout and post-layout simulation. An example of the capacitor placement effect on power plane impedance was shown. It was shown that using a floor planner model of the power/ground structure showed similar results to and simulated much faster than the layout CAD database. An analysis of a DDR memory bus was shown. Toshiro hoped that IBIS models will begin to supply PDS data suitable for detailed power noise analysis.

A question was asked about when analyzing the power noise, how are W-element models used when they assume an ideal power supply connection. Toshiro responded that the noise model only includes noise injected into the device.

CONCLUDING ITEMS

Michael Mirmak thanked the presenters, sponsors, co-sponsors and attendees for their support and participation. He hoped to continue this summit in the future. Takashi Watanabe also thanked the presenters and participants. The meeting adjourned at approximately 5:00 PM.

NEXT MEETING

The next IBIS Open Forum teleconference will be held November 21, 2008 from 8:00 AM to 10:00 AM US Pacific Standard Time.

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NOTES

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This meeting was conducted in accordance with the GEIA Legal Guides and GEIA Manual of Organization and Procedure.

The following e-mail addresses are used:

majordomo@eda.org
In the body, for the IBIS Open Forum Reflector:
subscribe ibis <your e-mail address>

In the body, for the IBIS Users' Group Reflector:
subscribe ibis-users <your e-mail address>

Help and other commands:

help

ibis-request@eda.org

To join, change, or drop from either or both:
IBIS Open Forum Reflector (ibis@eda.org)
IBIS Users' Group Reflector (ibis-users@eda.org)
State your request.

ibis-info@eda.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the EIA-IBIS Open Forum as a full Member.

ibis@eda.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/bugs/ibischk/
http://www.eda.org/ibis/bugs/ibischk/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/
http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eigroup.org/ibis/ibis.htm

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/ibis/directory.html

All eda.org documents can be accessed using a mirror:

http://www.ibis-information.org

Note that the "/ibis" text should be removed from directory names when this URL mirror is used.

GEIA STANDARDS BALLOT VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	October 10, 2008	October 31, 2008	November 11, 2008	November 14, 2008
Actel	Producer	Inactive				
Advanced Micro Devices	Producer	Active	√	√		√
Agilent Technologies	User	Inactive			√	
Ansoft	User	Active			√	√
Apple Computer	User	Inactive				
Applied Simulation Technology	User	Inactive				
ARM	Producer	Inactive				
Cadence Design Systems	User	Active			√	√
Cisco Systems	User	Active	√	√	√	
Ericsson	Producer	Active	√	√	√	√
Freescale	Producer	Inactive				
Green Streak Programs	General Interest	Inactive				
Hitachi ULSI Systems	Producer	Inactive				√
Huawei	User	Inactive			√	
IBM	Producer	Inactive	√	√		
Infineon Technologies AG	Producer	Inactive				
Intel Corp.	Producer	Active		√	√	√
LSI	Producer	Inactive				
Marvell Semiconductor	Producer	Inactive			√	
Mentor Graphics	User	Active	√		√	
Micron Technology	Producer	Active	√	√	√	√
Nokia Siemens Networks	Producer	Active	√	√	√	
Samtec	Producer	Inactive				
Signal Integrity Software	User	Active	√		√	
Sigrity	User	Inactive			√	
Synopsys	User	Inactive			√	
Teraspeed Consulting	General Interest	Active	√	√	√	√
Texas Instruments	Producer	Inacive		√		
Toshiba	Producer	Inactive				√
Xilinx	Producer	Active		√	√	√
ZTE	User	Inactive			√	
Zuken	User	Inactive				√

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH GEIA BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
- PRODUCERS - MEMBERS THAT SUPPLY ELECTRONIC EQUIPMENT.
- GENERAL INTEREST - MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.