# Using Behavior-level Model for SSN Analysis

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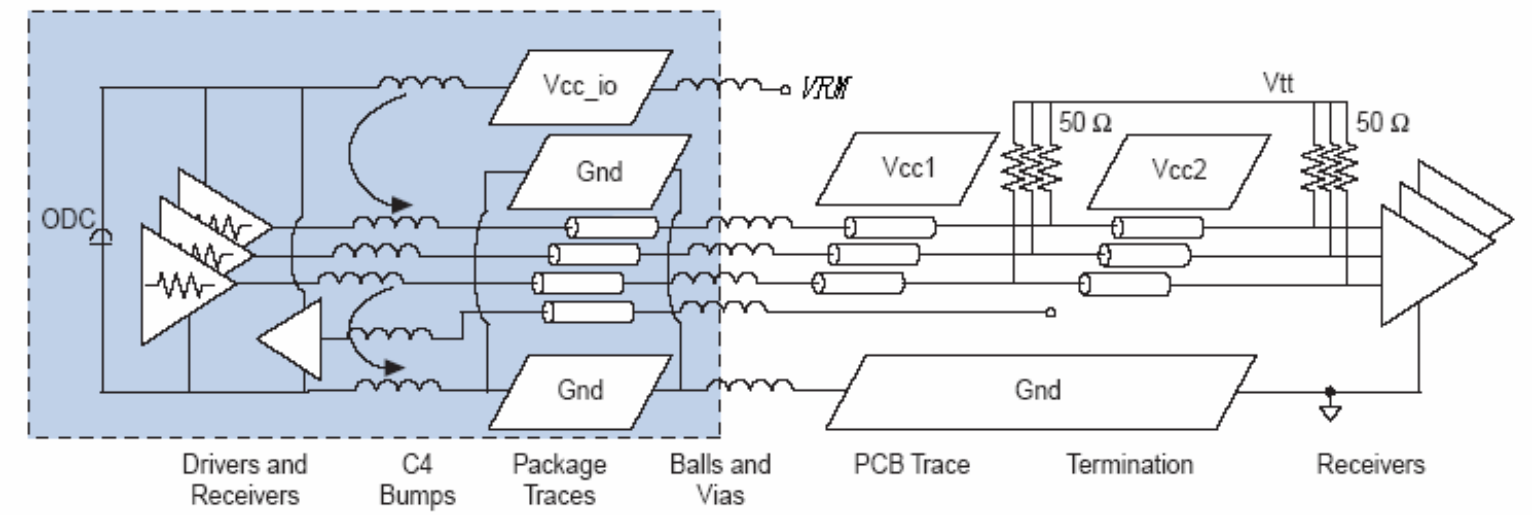
# Agenda

- Overview
- Solution Method of SSN
- Application with IBIS Model
- Improve Accuracy with IBIS Model
- Summary and expectation

# Overview

- Schematic diagram of simultaneous switching circuit




- Delta-I Current and Inductive Coupling result in SSN

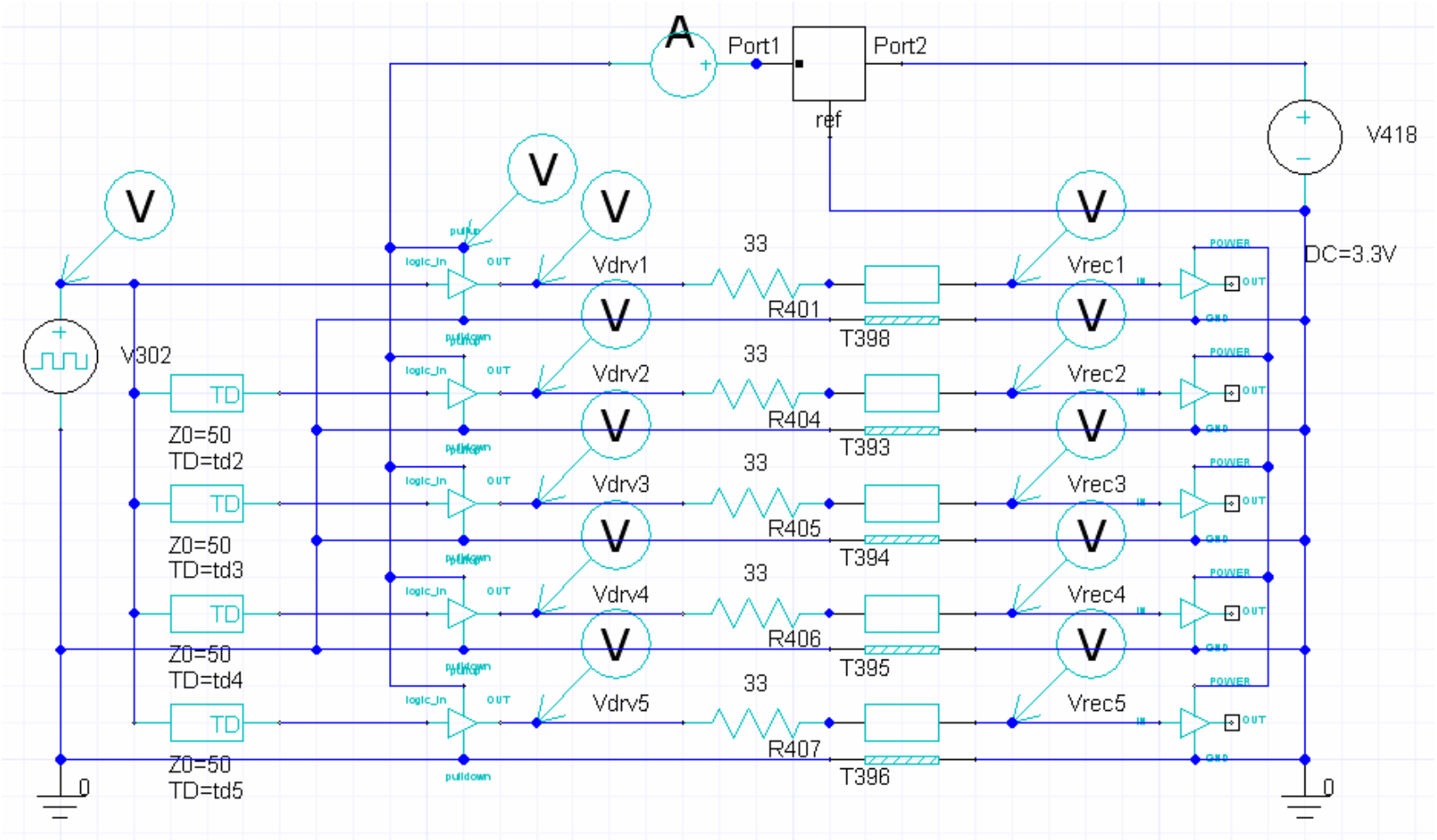
$$V = \sum_{k=1}^{N} L_k \times \frac{di_k}{dt}$$

# Solution Method of SSN

- Use SPICE Model
  - Good accuracy
  - models are derived from transistor-level netlist and layout
  - Relatively long simulation time and sometimes convergence problems
  - Intellectual property protection concerns
- Use IBIS Model
  - Models are derived from measurements and/or full SPICE model simulations
  - Fast simulation run time
  - overestimates power noise, ground noise and quiet line noise on account of no considering voltage feed back
- Use Macro Model based on IBIS model
  - Fast simulation run time
  - Good accuracy
  - Complex process in Modeling

# Application with IBIS Model

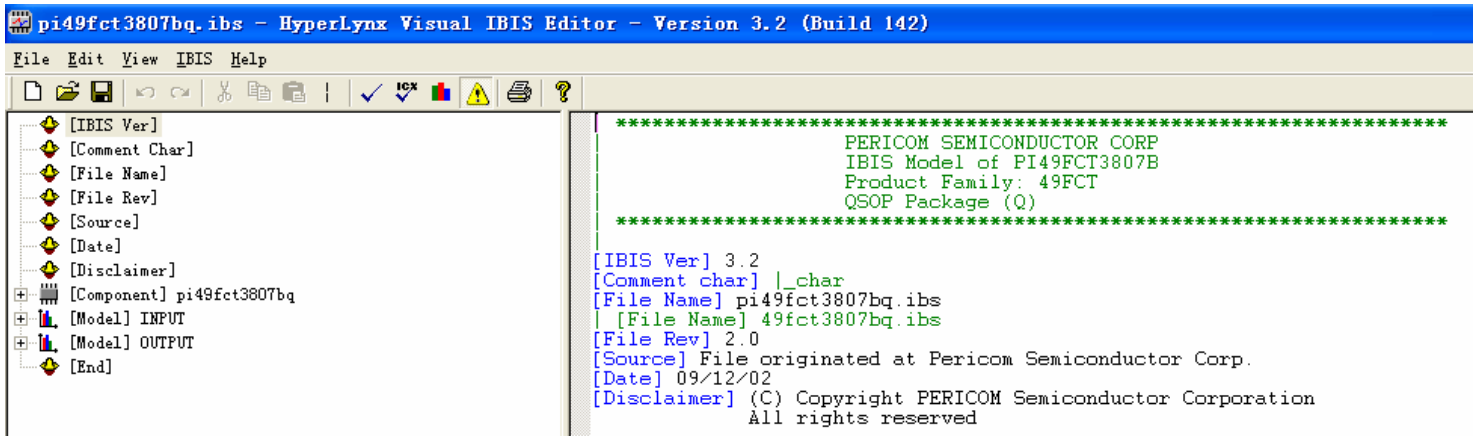
- Schematic diagram of test circuit



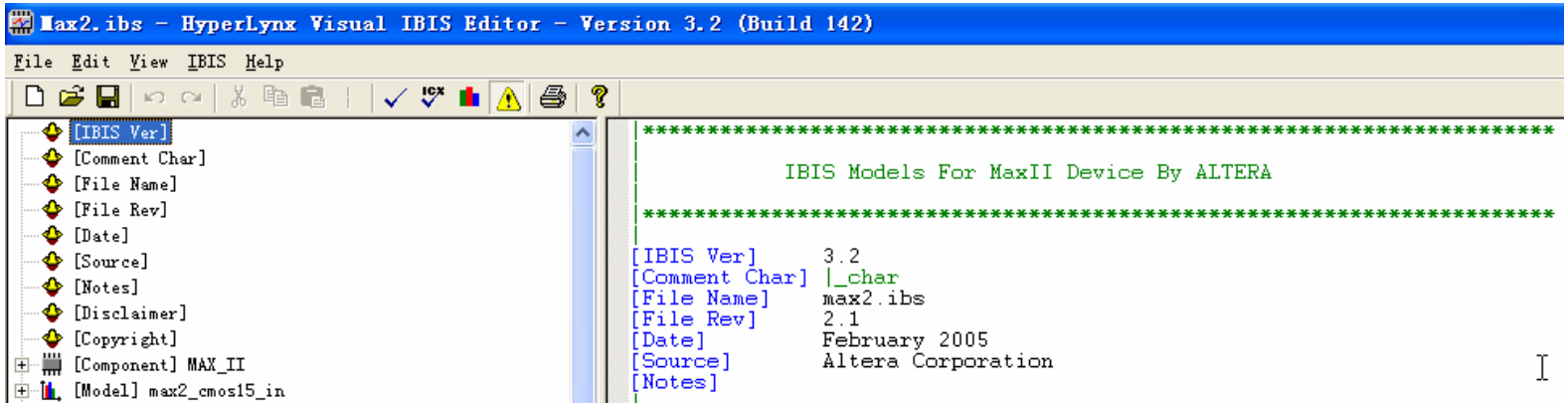
# Application with IBIS Model

## ❖ V3.2 IBIS Model

### ➢ Driver Model

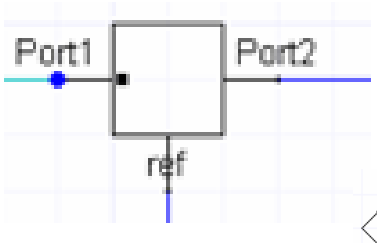


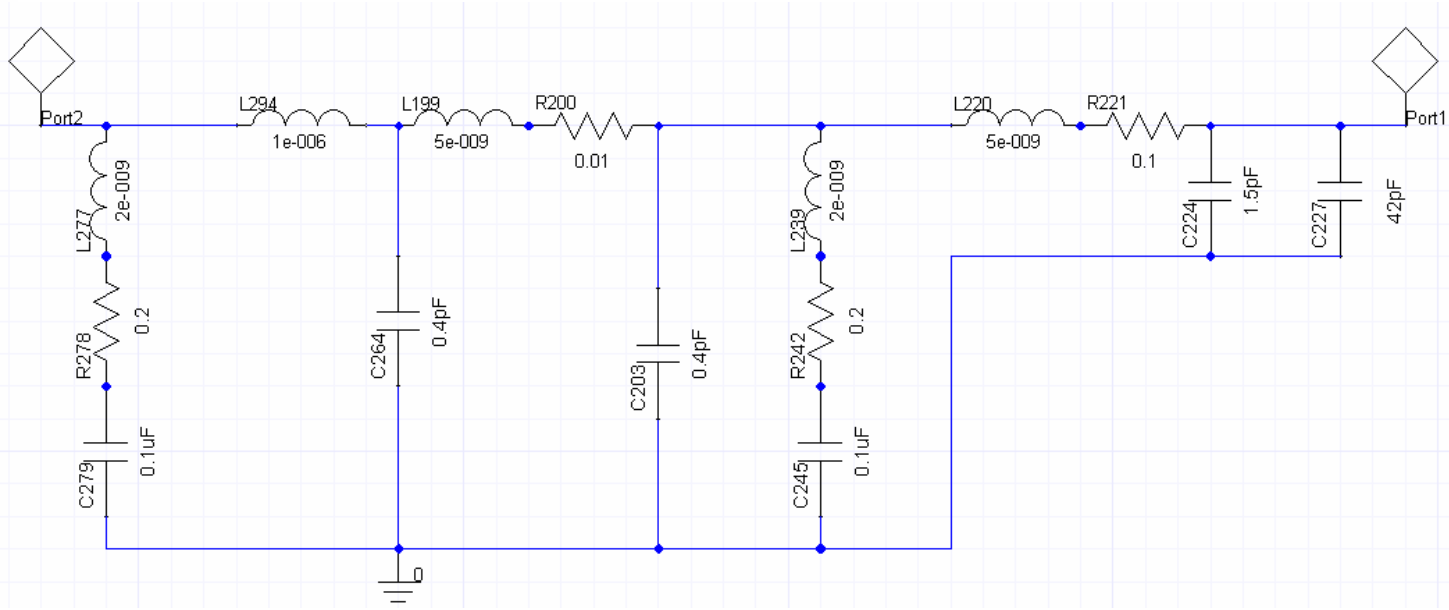

### ➢ Receiver Model



# Application with IBIS Model

- N-port for mimicking PDS

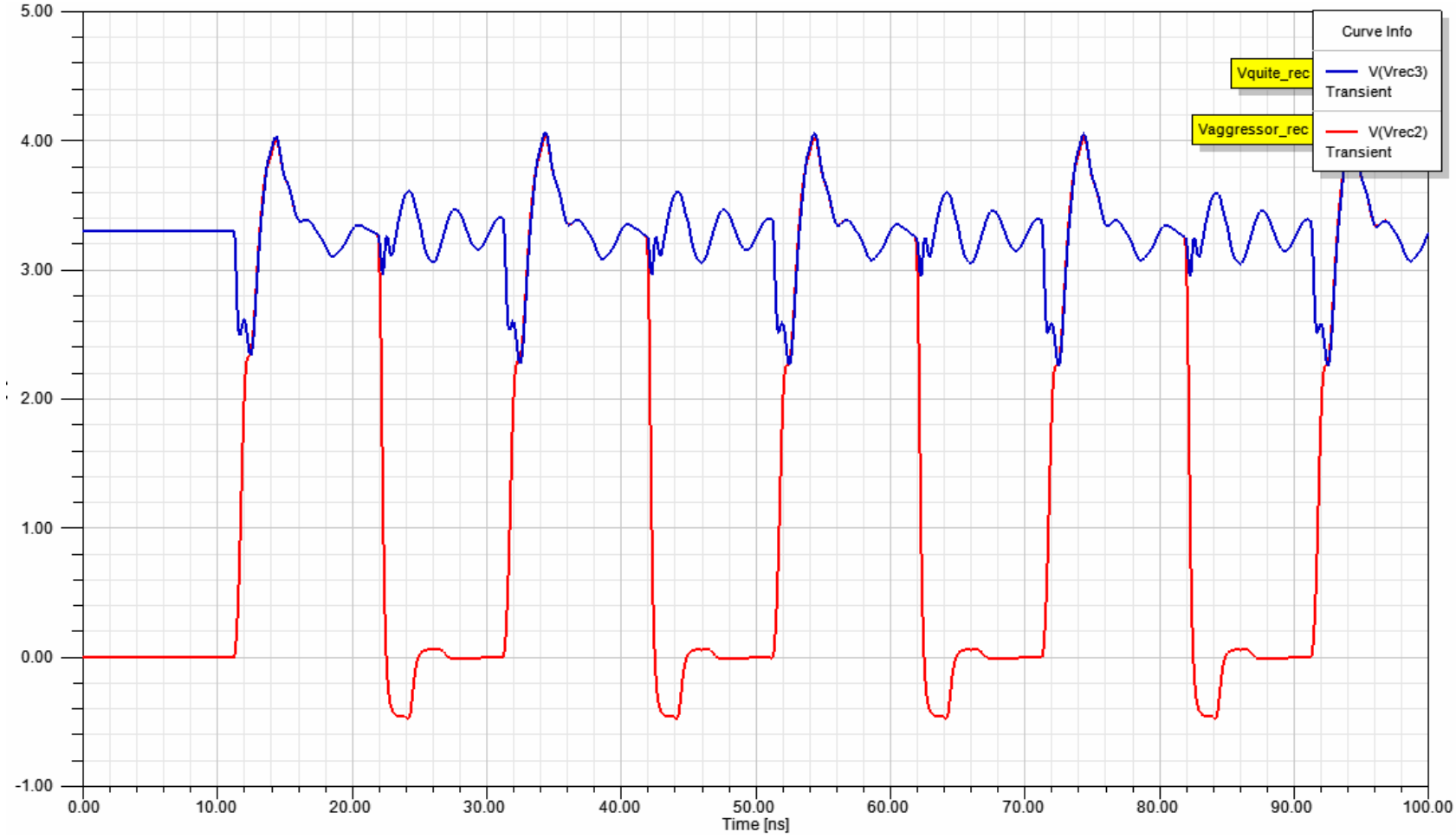



for simplifying, the 2-Port composed of RLGC component is applied

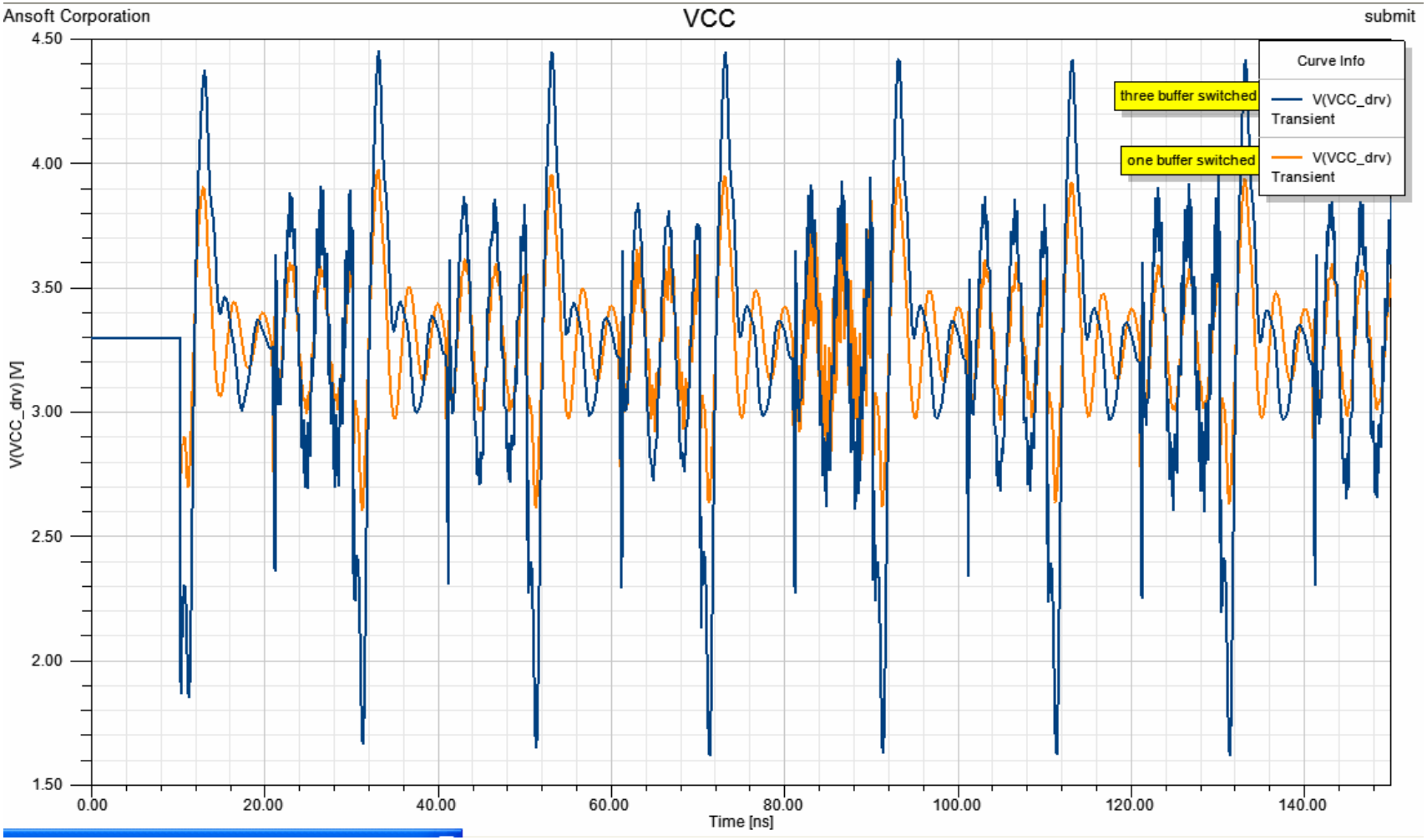
# Application with IBIS Model

- IO voltage for quite and signal line



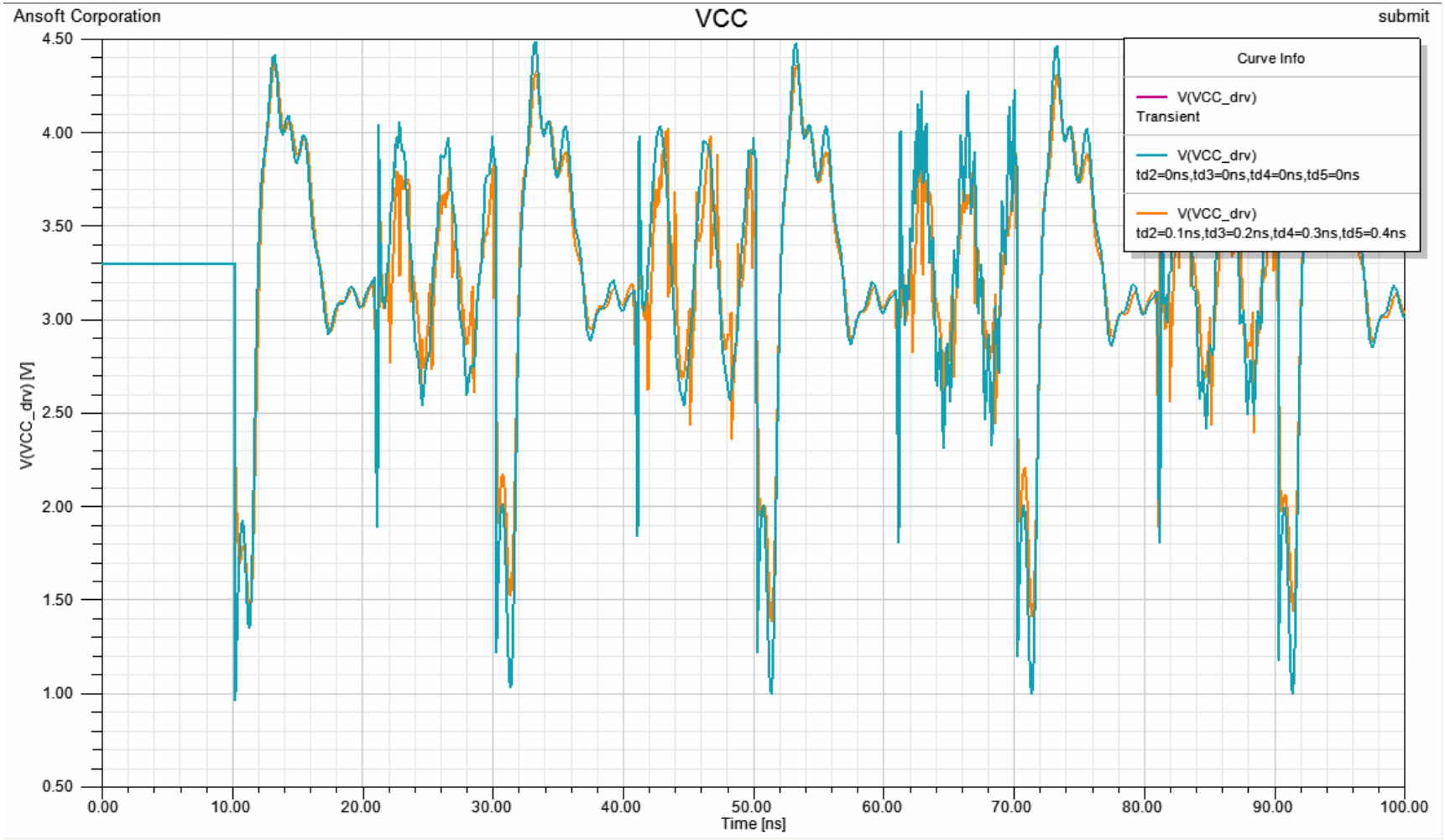
# Application with IBIS Model

- Correlation between buffer's quantity and VDD voltage



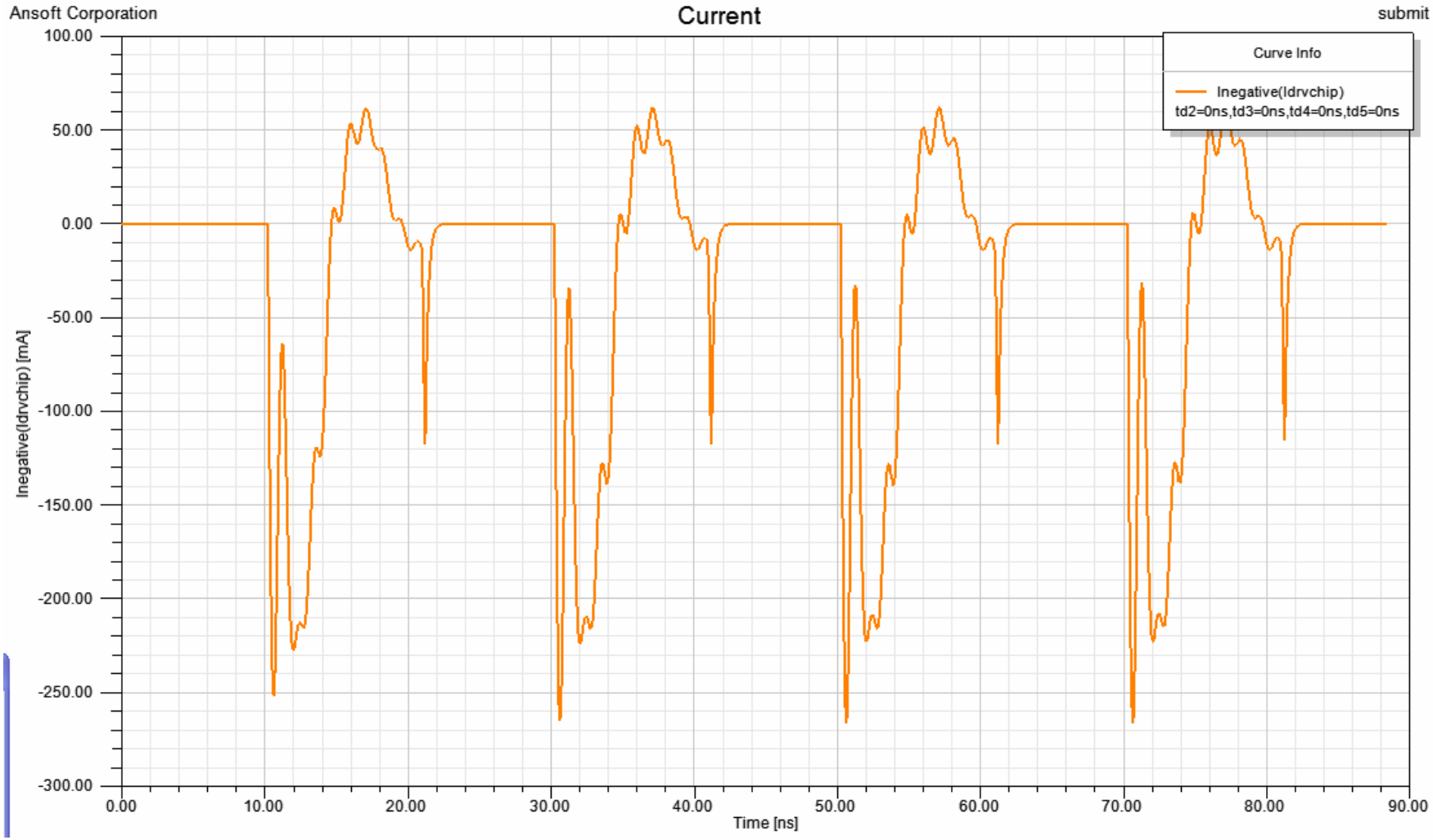
# Application with IBIS Model

- Correlation between switch time and VDD voltage



# Application with IBIS Model

## ❖ VDD current vs Time



# Improve Accuracy with IBIS Model

- Solution with IBIS Model is competent for optimizing PDS and SI/PI design
- As described in many paper, the accuracy isn't enough for evaluating SSN. Exactly, the result with IBIS Model overestimates power noise, ground noise and quiet line noise
- Some Method is proposed for improve accuracy with IBIS Model
  - Improve IBIS model with macro models
  - Improve model with voltage feedback
  - Improve algorithms to the extractions of parasitic current
  - …
  - BIRD95 methodology

# Related Presentation

- Varma, Proc of EPEP'04, SSN issues with IBISmodels

Create IBIS model of the driver using spline functions with finite time difference approximation modeling techniques

- Varma, Proc of EPEP'05, New method to achieve improved accuracy with IBIS models

Create IBIS model using voltage feedback by providing voltage controlled capacitances

- CHEN R Y, DesignCon'04, Adding on-chip capacitance in IBIS format for SSO simulations

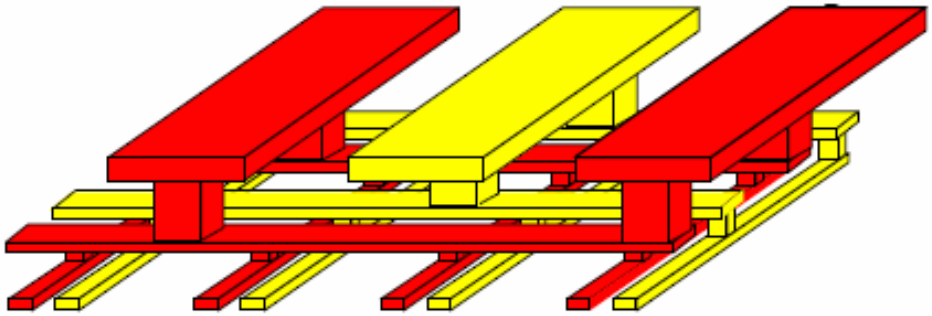
A new compensation capacitor is needed for the power and ground parasitics to maximize SSO correlation with realistic PDS models

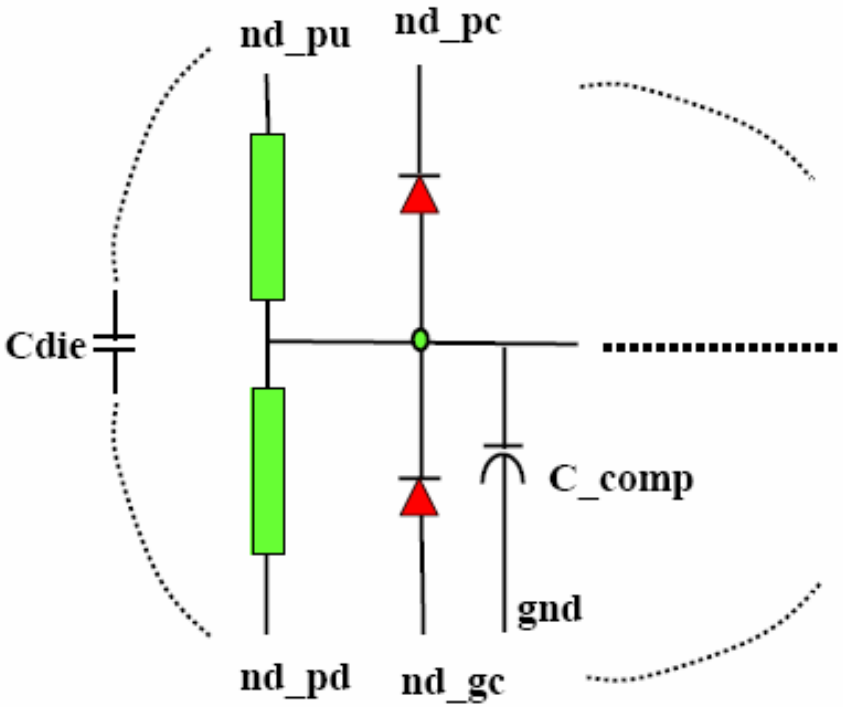
- BIRD95:http://www.vhdl.org/pub/ibis/birds/bird95.6.txt

Solving SSN will be achieved through the use of I-T tables updated BIRD95.6 now

# Use IBIS model with voltage feedback

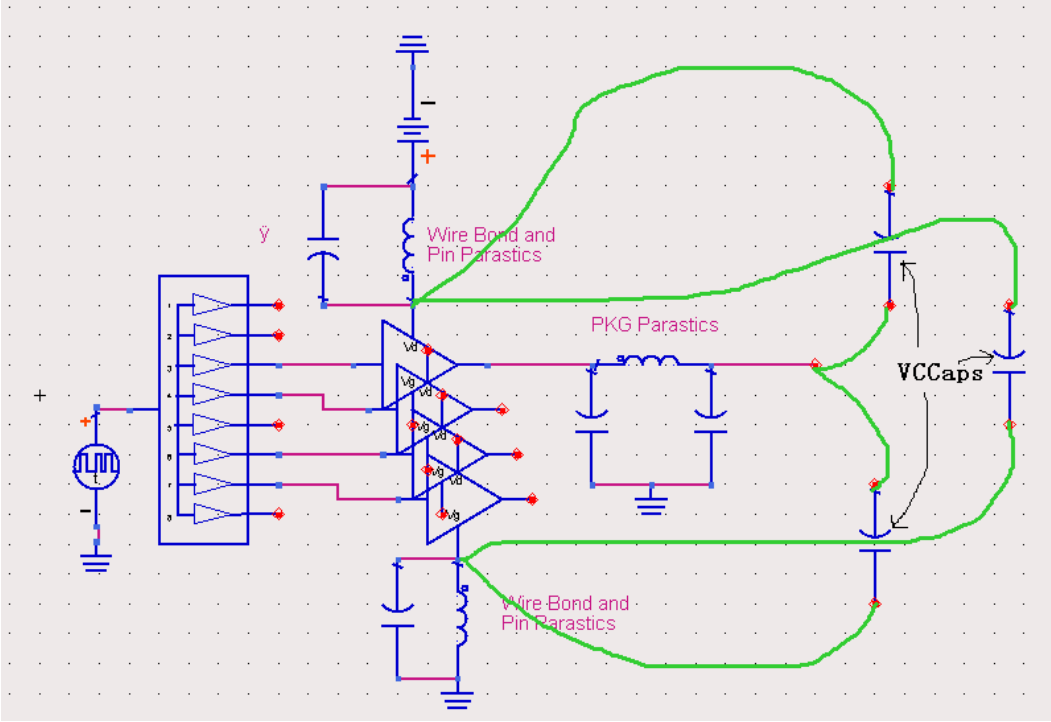
- Parasitic capacitance exists between all MOSFET terminals
- For the I/O pin, this is modeled in IBIS by C_comp
- A new compensation capacitor Cdie is needed





# Use IBIS model with voltage feedback

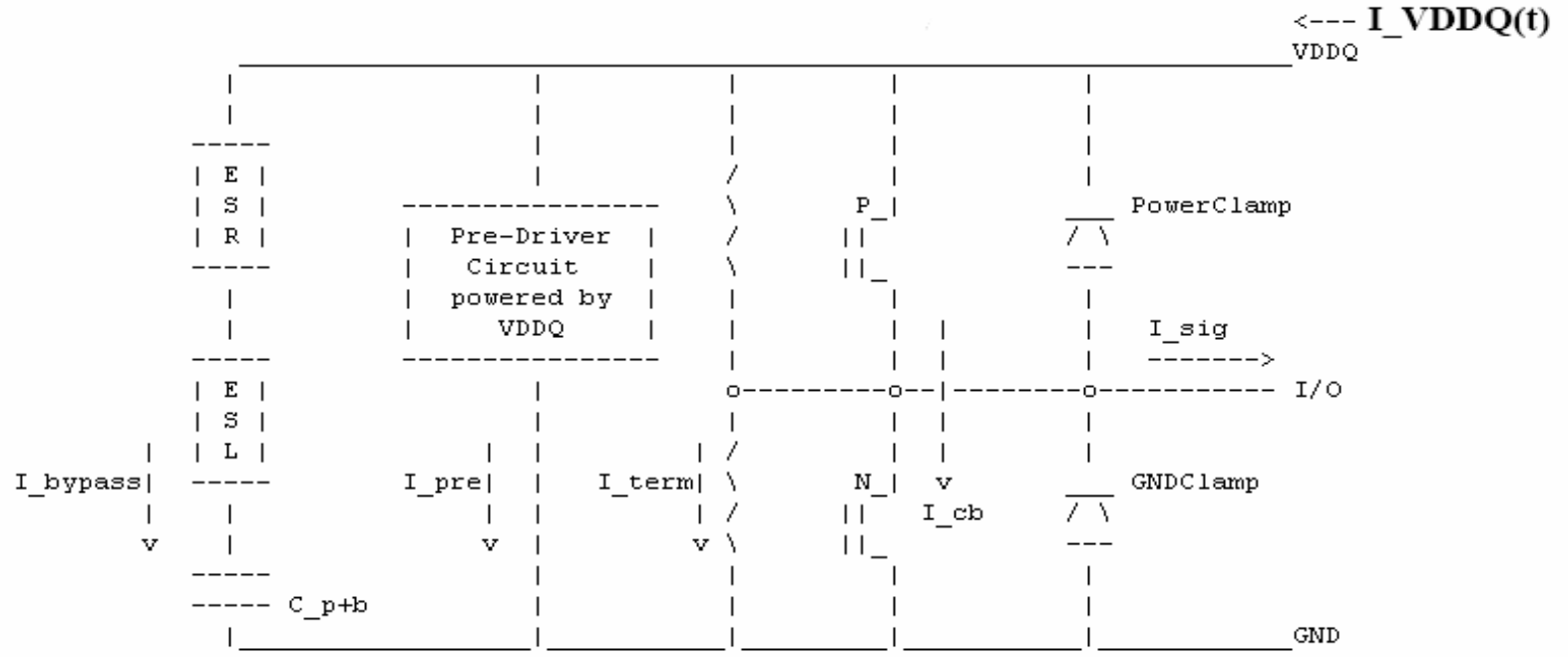
- Complement the IBIS driver as a separate subcircuit that users would add in conjunction to the B element in their circuit




The subcircuit consists of three separate Voltage Controlled Capacitances (VCCAPs) that are placed between the power and ground rails, the output and the power rail and the output and the ground rail

# BIRD95 methodology with IBIS Model

- BIRD95 shows great promise
  - Total VDDQ current will be measured for the transistor level model
  - Current versus time tables will be added to the IBIS file
  - The IBIS simulator will use the I_VDDQ(t) tables to include the parasitic currents from the pre-driver, I/O termination, crowbar, etc.
  - A power / ground impedance model is necessary for optimal correlation



# Summary and expectation

- Solution with IBIS Model of analyzing SSN is available for optimizing PDS design
- Many solutions of improving IBIS Model are proposed for evaluating SSN. BIRD95 Improves IBIS models to obviously facilitate accuracy of the SSN simulation
- Expect chip vendor put more efforts on generating more effective and accurate IBIS Model for circuit-level's designer as with birds95.6 format contained in IBISv5.0. And EDA vendor can develop corresponding tool to support the simulation based on the models
- It is expected by chip vendor and circuit-level's designer  that develop a conversion tool that can generate IBIS model of higher version from SPICE model