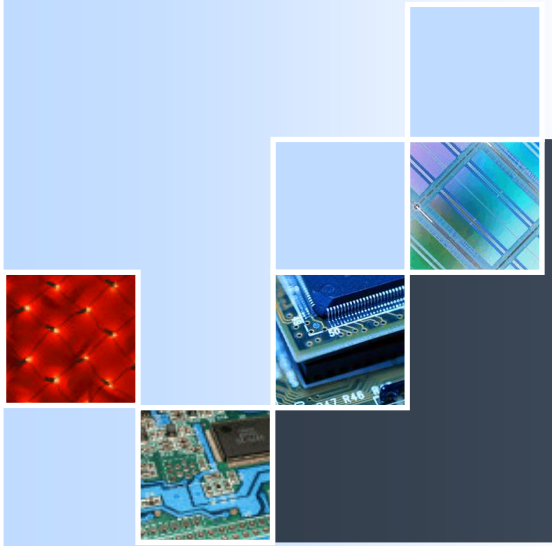

IBIS EBD Modeling, Usage and Enhancement

An Example of Memory Channel Multi-board Simulation

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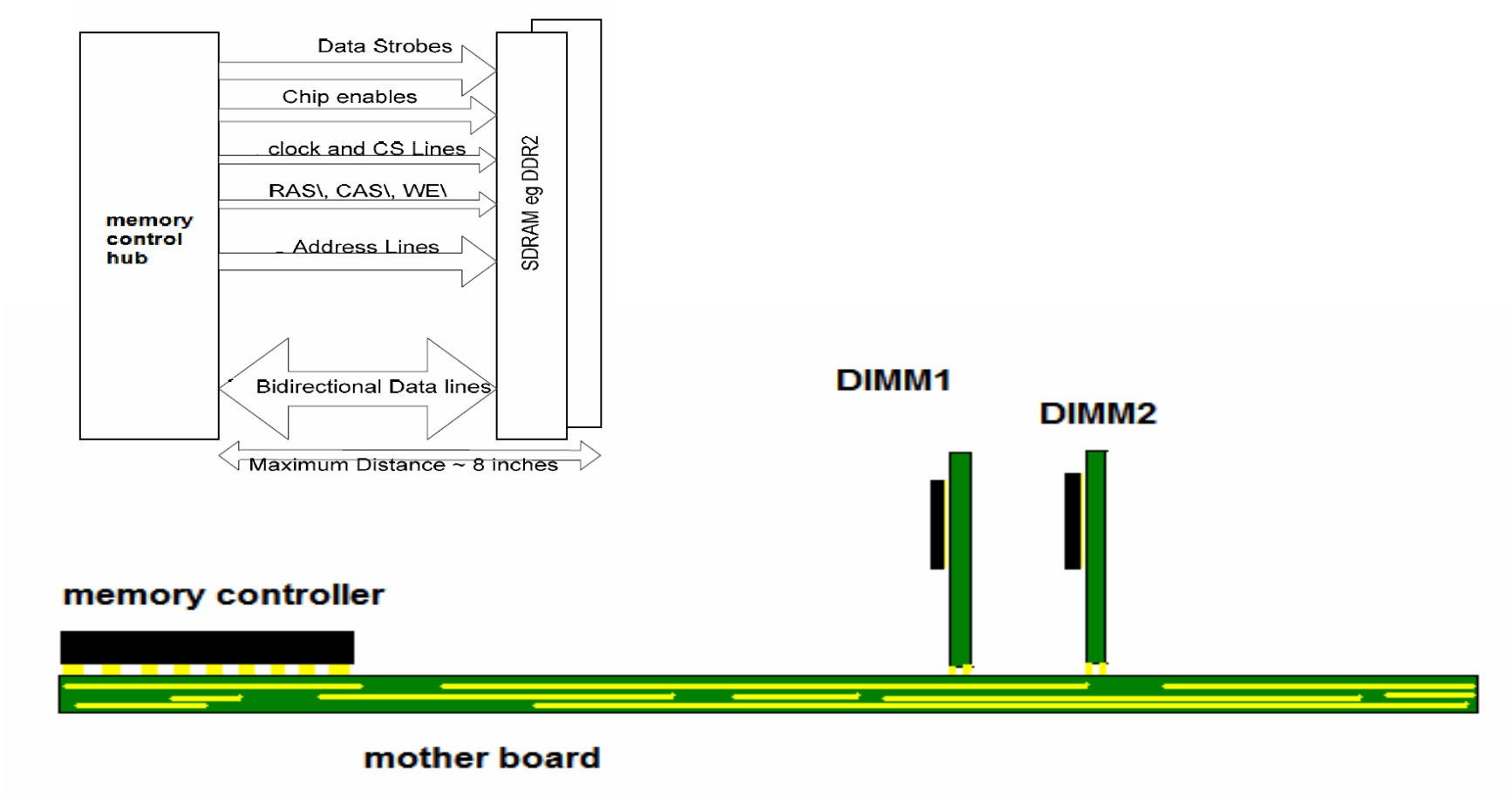
SIGRITY

Agenda

- Memory channel simulation
- EBD description
- EBD model for DIMM module
- EBD's pros and cons
- EBD enhancement requirement

Memory channel simulation



- A typical DIMM structure of memory channel

Challenge in memory channel simulation

- Multi-drop topology for different signal groups, especially for ADD/CMD and clock.
- High Speed signaling with transmission loss through dielectric material
- More tight timing requirement among different signal groups
- Serious crosstalk among signals and SSO
- Model accuracy for I/O buffer and sub-system of board component

EBD introduction

A board level component is the generic term to be used to describe a printed circuit board (PCB) or substrate which can contain components or even other boards, and which can connect to another board through a set of user visible pins. The electrical connectivity of such a board level component is referred to as an Electrical Board Description.

- EBD--Electrical Board Description
- A pure transmission line description without coupling for board component
- All inductance and capacitance parameters listed in the file are derived with respect to well-defined reference plane (s) within the board
- Via in EBD is described as zero length with lump RLC value
- EBD is good for transmission line effect assessment and timing analysis for first order consideration.

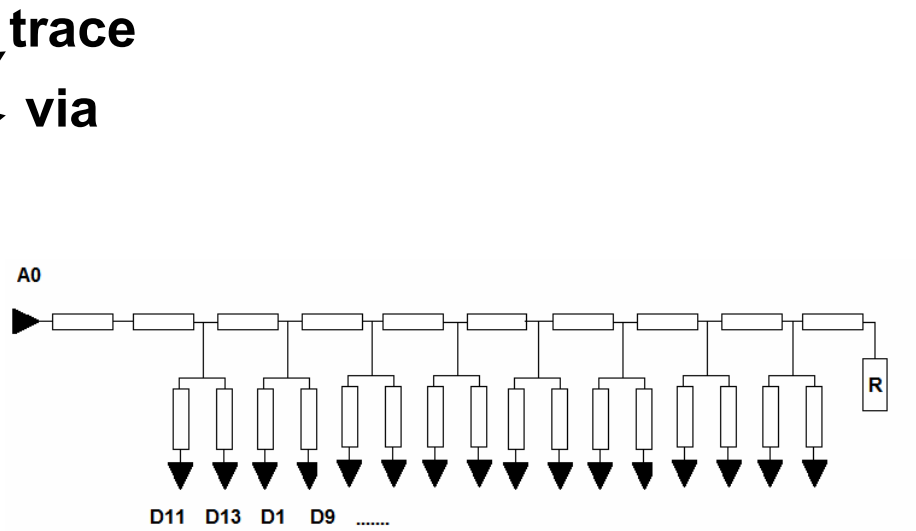
EBD description

- [Ibis Ver]
- [File Name]
- [File Rev]
- [Date]
- [Disclaimer]
- [Copyright]
- [Notes]
- [Begin Board Description]
- [Manufacturer]
- [Number of Pins]
- [Pin List] 240
- [Path Description] A0
- Pin 100
- Len = 0.0037.....
- .....
- Node aa.1
- [Reference Designator Map]
- aa ddr3.ibs ddr3input
- [End Board Description]
- [End]

Main part of EBD

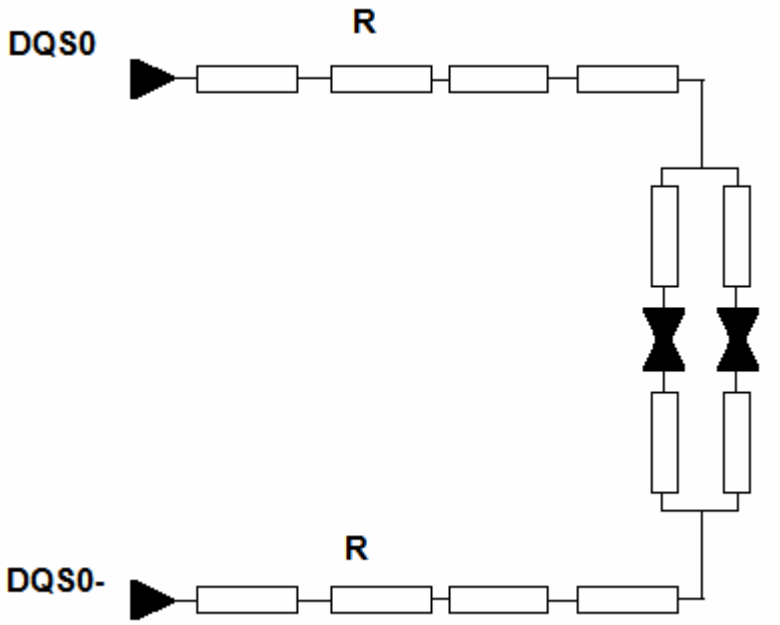
EDB used as DIMM module_ address path

- [Path Description] A0
- Pin 100
- Len = 0.00334997 L = 3.6198e-07 C = 9.34292e-11 R = 6.47878 /
- Len = 0 L = 1.886294e-10 C = 1.0395e-13 /
- Len = 0 L = 1.886294e-10 C = 1.0395e-13 /
- Len = 0.02320685 L = 3.6679e-07 C = 1.2723e-10 R = 13.9845 /
- Len = 0 L = 9.431472e-11 C = 5.1975e-14 /
- Fork
- Len = 0 L = 9.431472e-11 C = 5.1975e-14 /
- Len = 0.00213924 L = 3.6198e-07 C = 9.34292e-11 R = 6.47878 /
- Node D11.K3
- Endfork
- Len = 0 L = 9.431472e-11 C = 5.1975e-14 /
- Len = 0 L = 9.431472e-11 C = 5.1975e-14 /
- Fork
- Len = 0 L = 9.431472e-11 C = 5.1975e-14 /
- Len = 0.00214104 L = 3.6198e-07 C = 9.34292e-11 R = 6.47878 /
- Node D3.K3
- Endfork
- Len = 0 L = 9.431472e-11 C = 5.1975e-14 /
- Len = 0.03001702 L = 3.29692e-07 .....



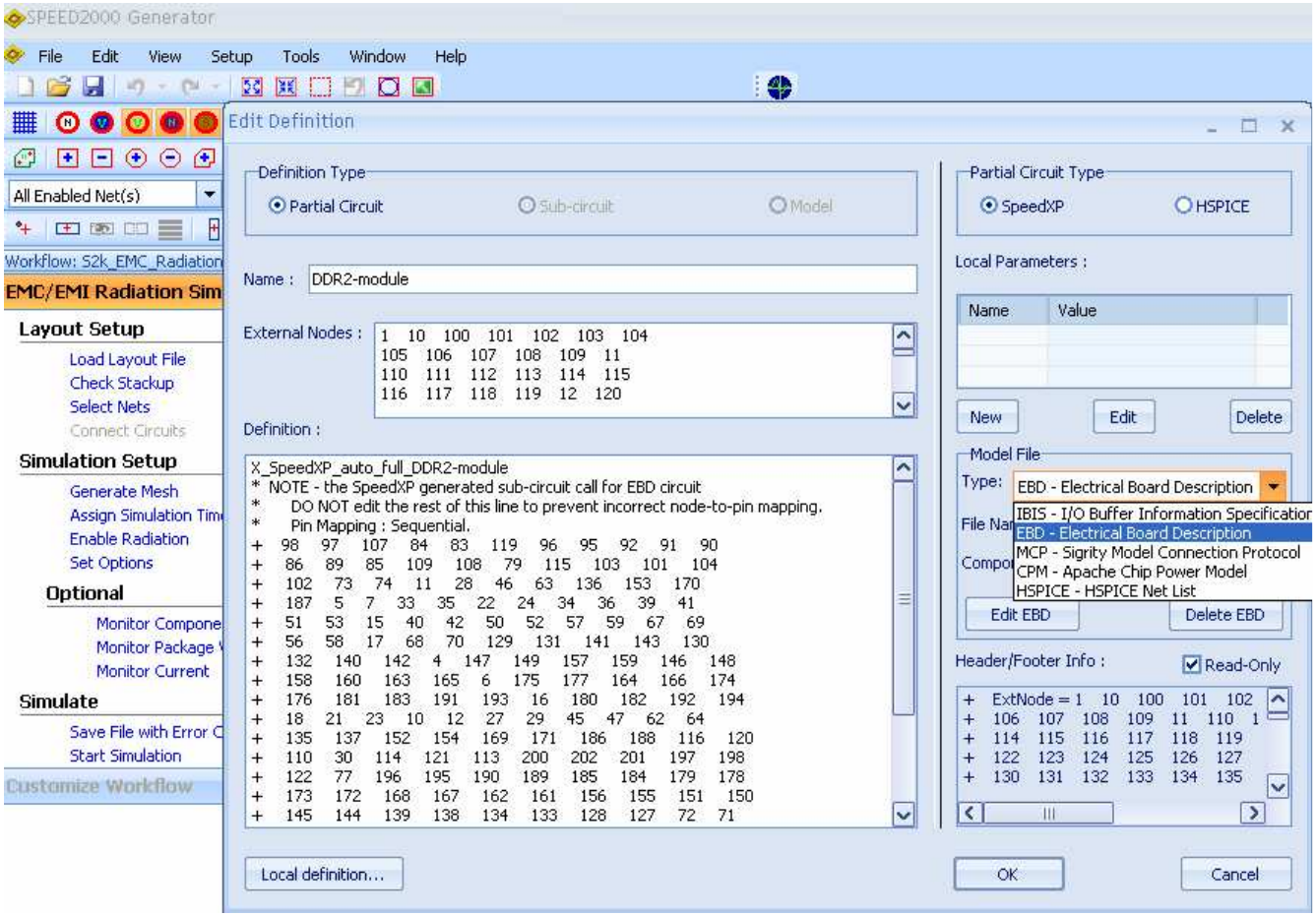
EDB used as DIMM module_ data strobe path

- [Path Description] DQS0
- Pin 13
- Len = 0.00316589 L = 3.6198e-07 C = 9.34292e-11 R = 6.47878 /
- Node RP42.5
- Node RP42.4
- Len = 0.00206140 L = 3.6198e-07 C = 9.34292e-11 R = 6.47878 /
- Len = 0 L = 1.886294e-10 C = 1.0395e-13 /
- Len = 0 L = 1.886294e-10 C = 1.0395e-13 /
- Len = 0.02299734 L = 3.29692e-07 C = 1.41546e-10 R = 11.1876 /
- Len = 0 L = 1.25753e-10 C = 6.93e-14 /
- Fork
- Len = 0 L = 1.25753e-10 C = 6.93e-14 /
- Len = 0.00176569 L = 3.6198e-07 C = 9.34292e-11 R = 6.47878 /
- Node D8.C3
- Endfork
- Len = 0 L = 1.25753e-10 C = 6.93e-14 /
- Len = 0.00176569 L = 3.6198e-07 C = 9.34292e-11 R = 6.47878 /
- Node D0.C3
- |
- [Path Description] DQS0-
- Pin 27
- .....

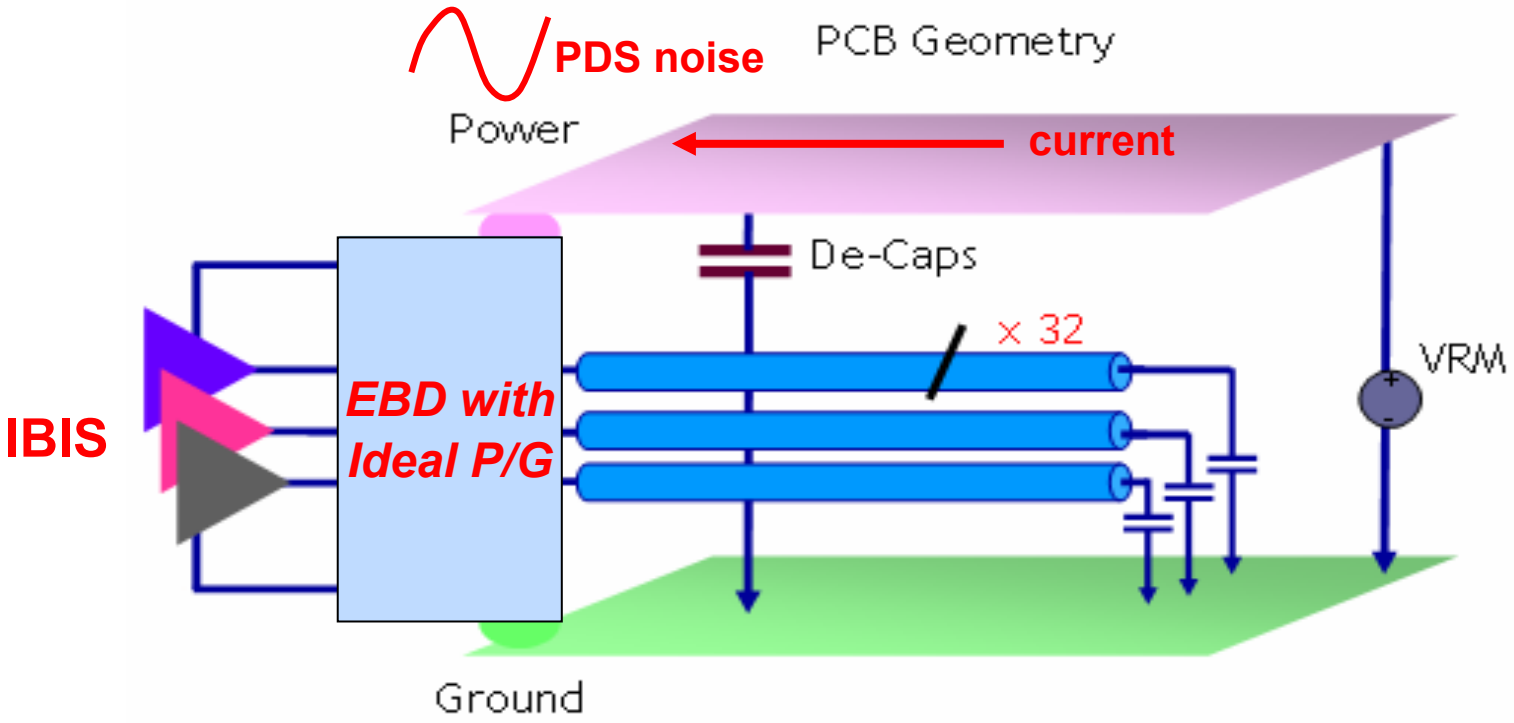


EBD usage for memory channel simulation

- EDA tools support IBIS EBD model
- Automatically linkage to EBD file makes usage very convenient

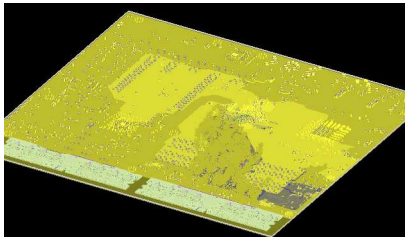


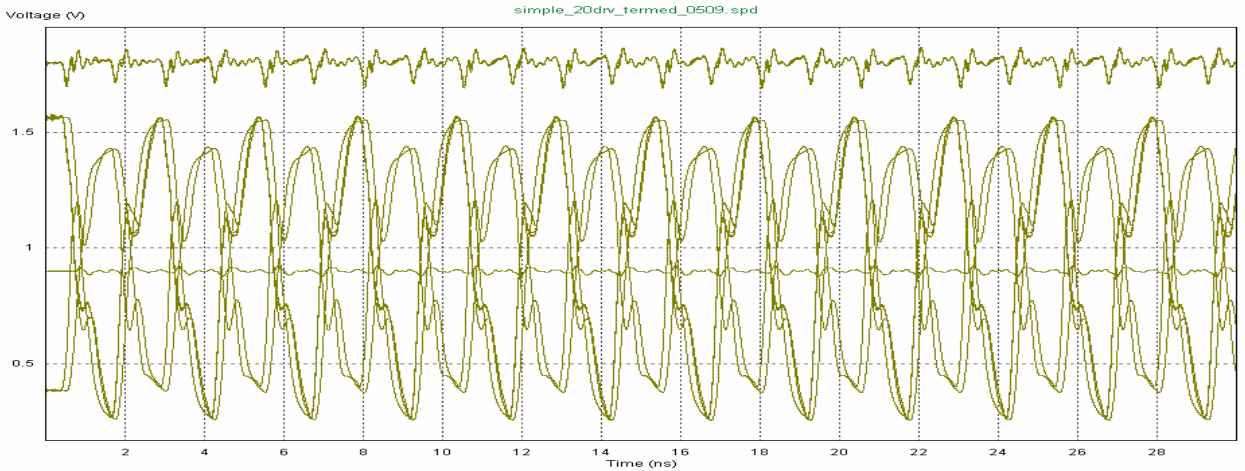
EBD Simulation Problem

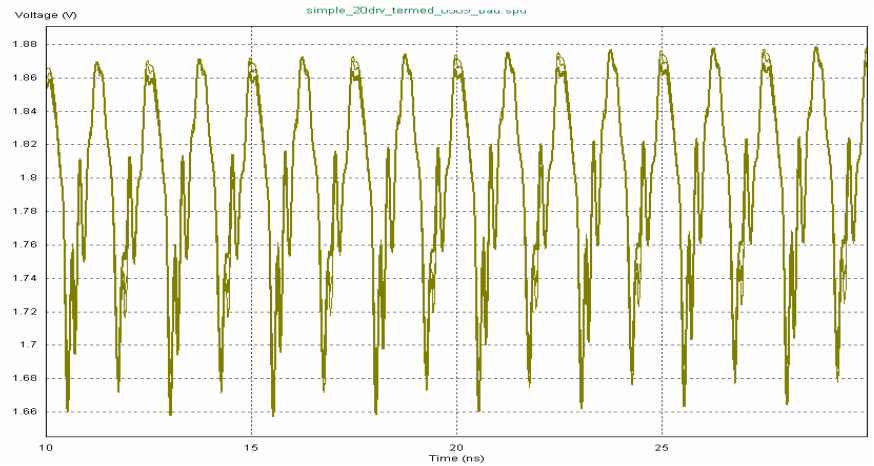


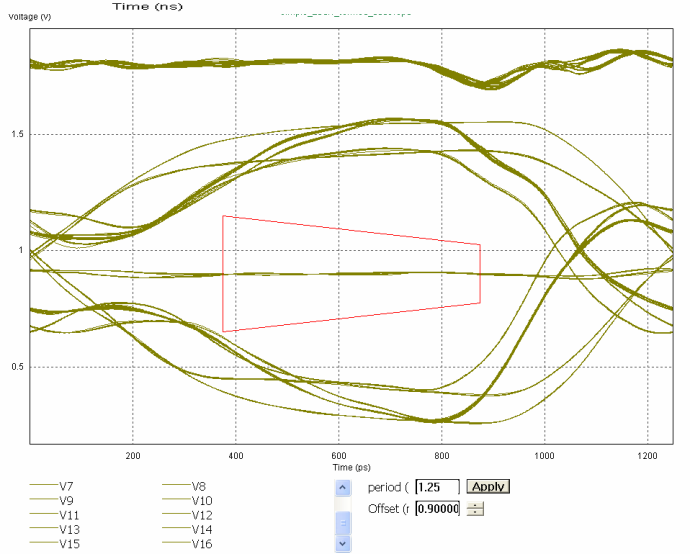
- Power/Ground are ideal in EBD
- PDS noise is contributed by PCB power/ground planes design
- All coupling effect among signals only occurred on PCB level
- Return current issue can't be considered completely due to idea P/G and lost interaction between signal and P/G

Simulation structure and result









- Power and signal result
- SSN result (got from motherboard only, that is, power pin in chips on EBD has similar waveform as power pin at connector)
- Signal result (in EBD part only ideal Tline effect was considered)

Pros and Cons

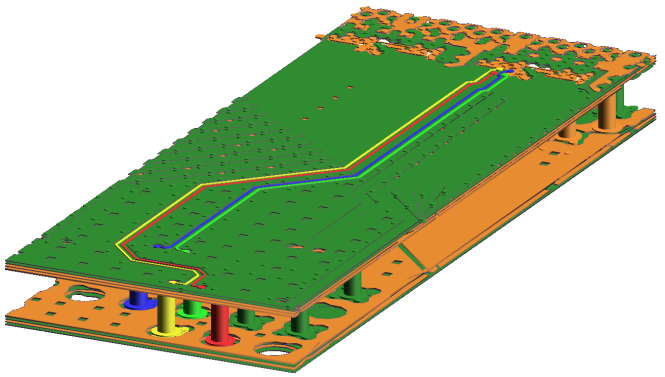
- Pros
  - Full topology of board component was described.
  - Most manufactures provide the model – easy to get
  - Easy to be used in EDA tools for system level analysis.

- Cons
  - Don’t have coupling information for crosstalk analysis among traces. Differential signal was considered separately
  - Ideal ground and power assumption that make PDS analysis not complete.

EBD enhancement –Cross talk

- Why important?
  - Most of memory bus now is parallel. Cross talk effect is obvious among signals.
  - Differential signaling is common for DQS and Clock.

- How ?
  - Mutual R, L, C can solve the issue in some degree.
  - S parameter matrix

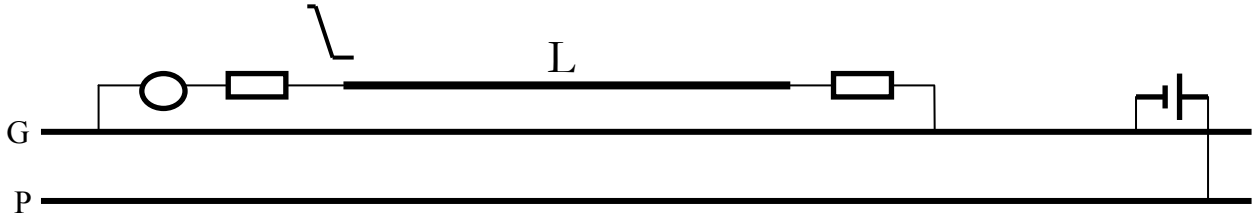


EBD enhancement– real power and ground

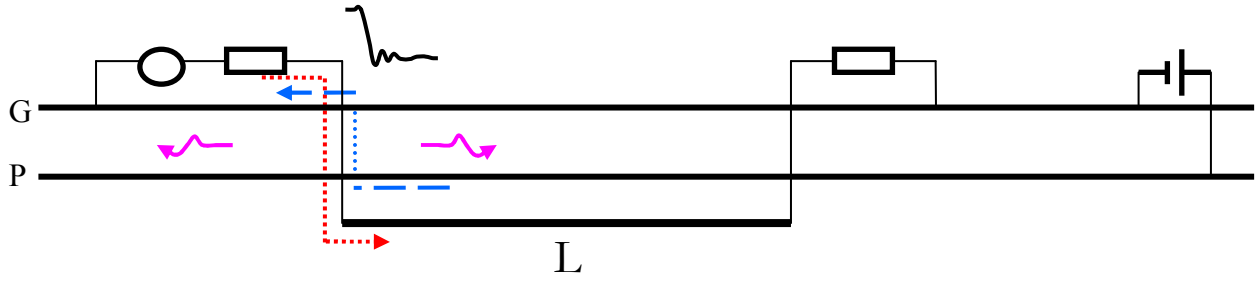
- Why important?
  - SSN analysis is very important for parallel bus such as memory bus.
- How?
  - Path for power and ground description was added into also

Power integrity *versus* signal integrity ?

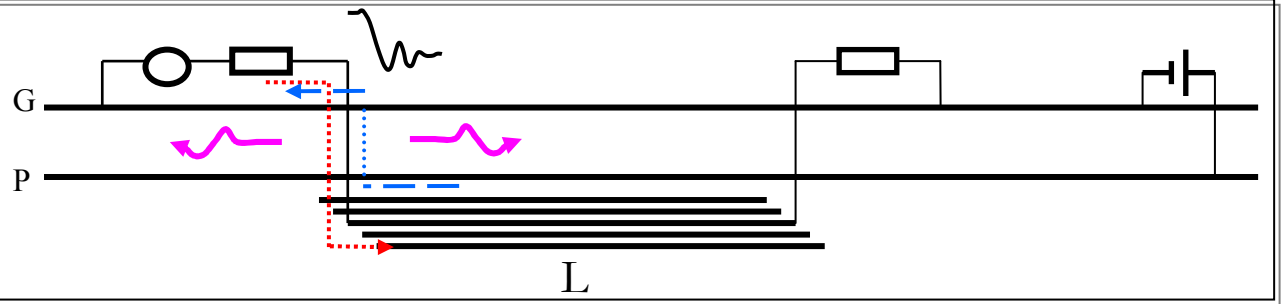
One signal switching without reference plane change



One signal switching with reference plane change

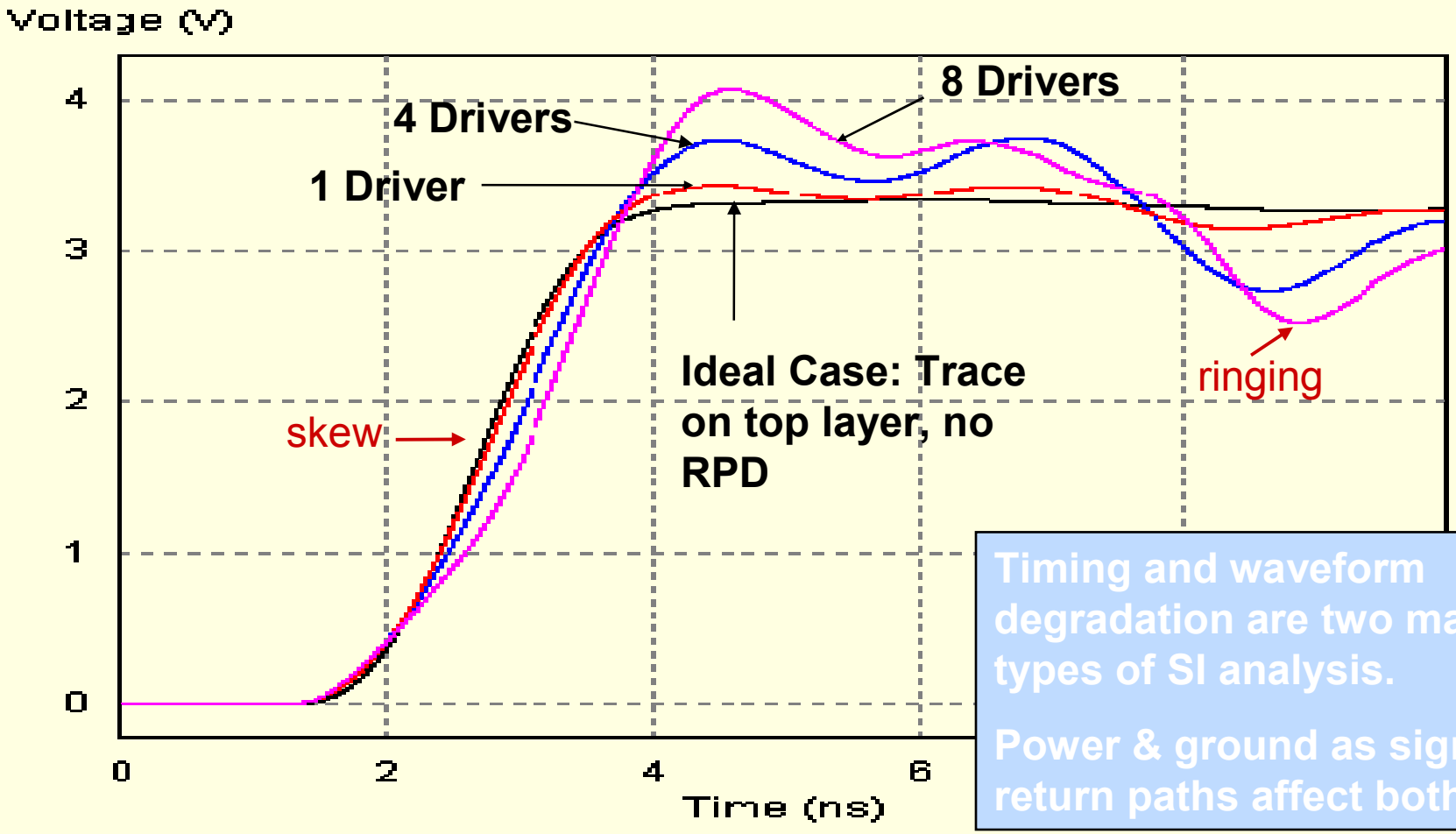


Multiple signals switching with reference plane change



Power integrity *and* signal integrity !

SSN/SSO – Simultaneous Switching Noise/Output

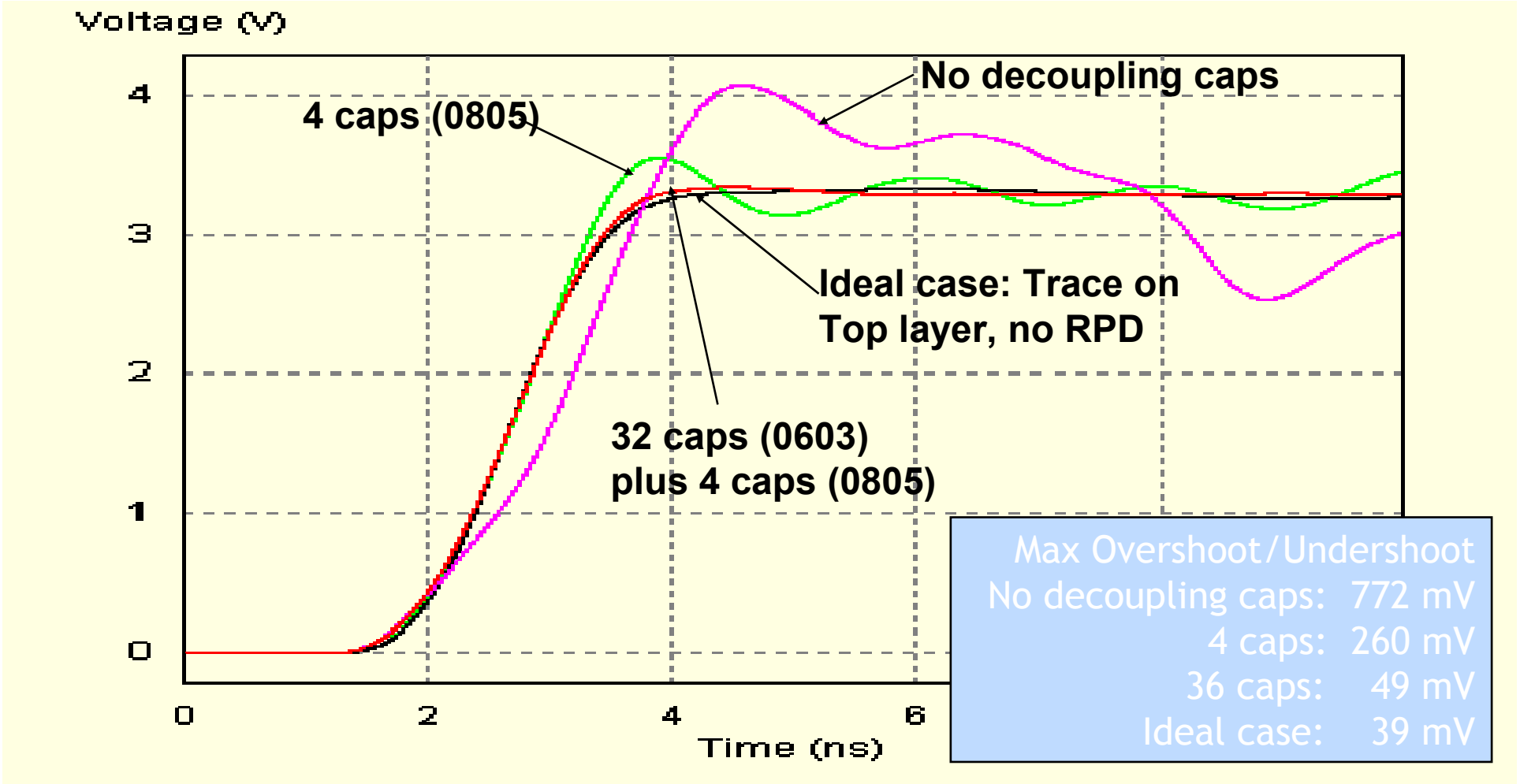


Timing and waveform degradation are two major types of SI analysis.

Power & ground as signal return paths affect both.

Power integrity *and* signal integrity !

effect of adding decaps



Conclusion

- EBD is good to be used as module model in IBIS family
- EBD has weakness in modeling crosstalk and real power/ground
- Enhancement was required with today's design trend.