IBIS Update

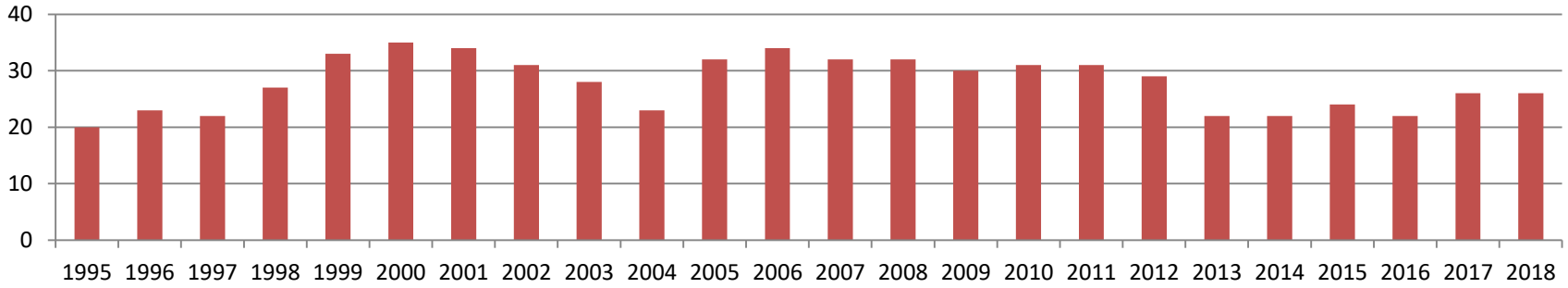
Mike LaBonte
SiSoft
Chair, IBIS Open Forum

2018 IEEE SPI IBIS Summit
Brest, France
May 25, 2018

http://www.ibis.org/

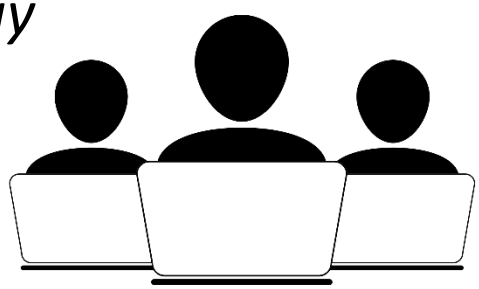
26 IBIS Members

Number of Members by Year



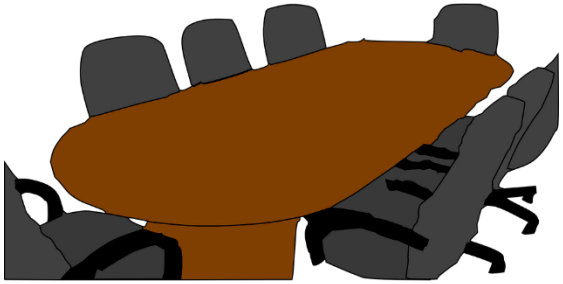
IBIS Officers 2017-2018

Chair:	*Mike LaBonte, SiSoft*
Vice-Chair:	*Lance Wang, IO Methodology Inc.*
Secretary:	*Randy Wolff, Micron Technology*
Treasurer:	*Bob Ross, Teraspeed Labs*
Librarian:	*Anders Ekholm, Ericsson*
Postmaster:	*Curtis Clark, ANSYS*
Webmaster:	*Mike LaBonte, SiSoft*



2018 Officer Election nominations are open now

IBIS Meetings



- Weekly teleconferences
  - Quality Task Group (Tuesdays)
  - Advanced Technology Modeling Task Group (Tuesdays)
  - Interconnect Task Group (Wednesdays)
  - Editorial Task Group (some Fridays)
- IBIS Open Forum teleconference every 3 weeks
  - 505 meetings so far
- IBIS Summit meetings: DesignCon, IEEE SPI, EDICON USA, EPEPS, Shanghai, Taipei, Tokyo

SAE ITC

- SAE Industry Technologies Consortia is the parent organization of the IBIS Open Forum
- IBIS is assisted by SAE employees José Godoy, Phyllis Gross, Dorothy Lloyd
- SAE ITC provides financial, legal, and other services
- http://www.sae-itc.org/

Task Groups

- Interconnect Task Group
  - Chair: Michael Mirmak
  - http://ibis.org/interconn_wip/
  - Develop on-die/package/module/connector interconnect modeling BIRDs
- Advanced Technology Modeling Task Group
  - Chair: Arpad Muranyi
  - http://ibis.org/atm_wip/
  - Develop most other technical BIRDs
- Quality Task Group
  - Chair: Mike LaBonte
  - http://ibis.org/quality_wip/
  - Oversee IBISCHK parser testing and development
- Editorial Task Group
  - Chair: Michael Mirmak
  - http://ibis.org/editorial_wip/
  - Produce IBIS Specification documents

BIRD = Buffer Issue Resolution Document

IBIS Milestones

I/O Buffer Information Specification

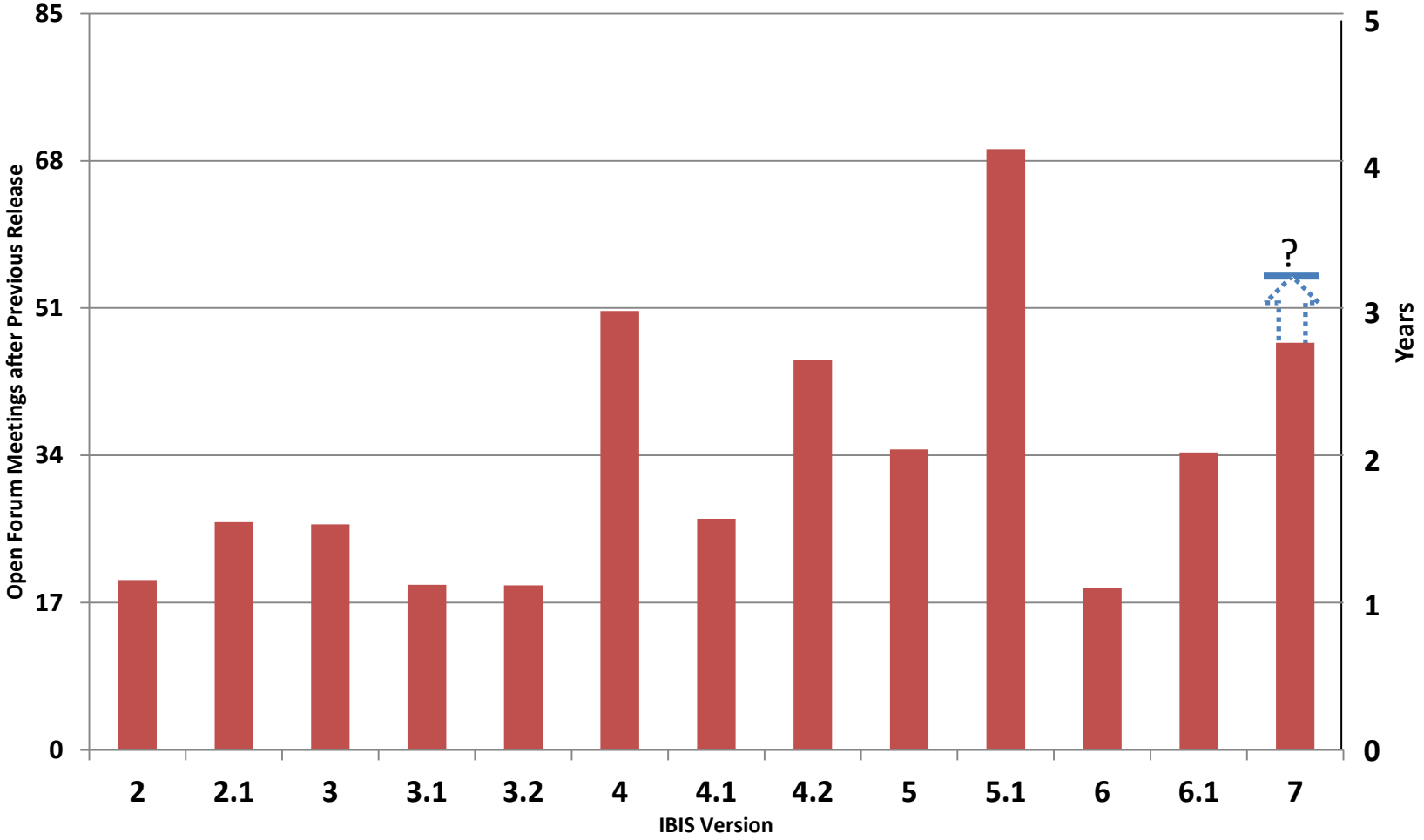
- 1993-1994 **IBIS 1.0-2.1**:
  - Behavioral buffer model (fast simulation)
  - Component pin map (easy EDA import)
- 1997-1999 **IBIS 3.0-3.2**:
  - Package models
  - Electrical Board Description (EBD)
  - Dynamic buffers
- 2002-2006 **IBIS 4.0-4.2**:
  - Receiver models
  - AMS languages
- 2007-2012 **IBIS 5.0-5.1**:
  - IBIS-AMI SerDes models
  - Power aware
- 2013-2015 **IBIS 6.0-6.1**:
  - PAM4 multi-level signaling
  - Power delivery package models
- **2018? IBIS 7.0**

Current development

Other Work

- 1995: **ANSI/EIA-656**
  - IBIS 2.1
- 1999: **ANSI/EIA-656-A**
  - IBIS 3.2
- 2001: **IEC 62014-1**
  - IBIS 3.2
- 2003: **ICM 1.0**
  - Interconnect Model Specification
- 2006: **ANSI/EIA-656-B**
  - IBIS 4.2
- 2009: **Touchstone 2.0***
- 2011: **IBIS-ISS 1.0**
  - Interconnect SPICE Subcircuit specification

IBIS Version Development



As of 2-Feb-2018

Possible IBIS 7.0 Timeline

Meeting Date	Milestone
4/21/2017	Vote to establish 7.0 as the next IBIS version passes
5/12/2017	*BIRD review and acceptance (24 meetings)*
…	
6/8/2018	Vote to approve BIRD189.6 scheduled for next meeting
6/29/2018	Vote to approve 7.0 BIRD set scheduled for next meeting
7/20/2018	7.0 BIRD set accepted. Editorial work begins (2 meetings)
8/10/2018	
8/31/2018	Editorial announces IBIS 7.0 ready. Review period begins
9/21/2018	
10/12/2018	Vote to ratify 7.0 scheduled for next meeting
11/2/2018	IBIS 7.0 ratified

BIRDs Possibly Included in IBIS 7.0

BIRD	Title
147.6	Back-channel Support
165	Parameter Passing Improvements for [External Circuit]s
179	New IBIS-AMI Reserved Parameter Special_Param_Names
180	Require Unique Pin Names in [Pin]
182	POWER and GND [Pin] signal_name as [Pin Mapping] bus_label
183	[Model Data] Matrix Subparameter Terminology Correction
184.2	Model_name and Signal_name Restriction for POWER and GND Pins
185.2	Section 3 Reserved Word Guideline Update
186.4	File Naming Rules
187.3	Format and Usage Out Clarifications
188.1	Expanded Rx Noise Support for AMI
189.6	Interconnect Modeling Using IBIS-ISS and Touchstone
191.2	Clarifying Locations for Si_location and Timing_location
192.1	Clarification of List Default Rules
193	Figure 29 corrections
194	Revised AMI Ts4file Analog Buffer Models

Green = currently accepted BIRD

White = currently not an accepted BIRD

BIRDs Possibly Excluded from IBIS 7.0

BIRD	Title
125.1	Make IBIS-ISS Available for IBIS Package Modeling
145.3	Cascading IBIS I/O buffers with [External Circuit]s using the [Model Call] keyword
158.7	AMI Ts4file Analog Buffer Models
163	Instantiating and Connecting [External Circuit] Package Models with [Circuit Call]
164	Allowing Package Models to be defined in [External Circuit]
166.2	Resolving problems with Redriver Init Flow
181.1	I-V Table Clarifications
190	Clarification for Redriver Flow

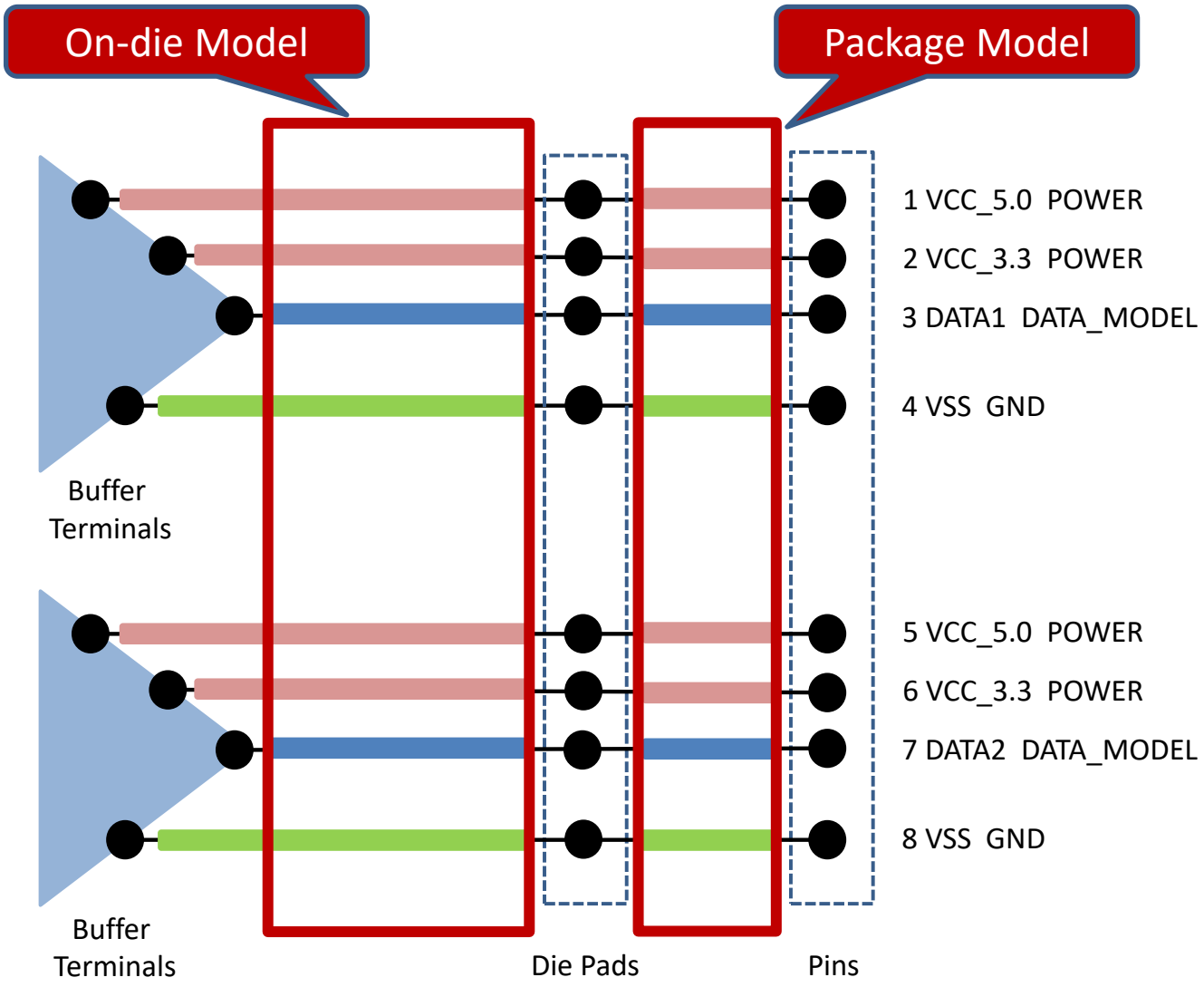
Red = superseded, likely to be rejected

White = for future consideration

BIRD189.6

- New package and on-die model formats:
  - IBIS-Interconnect SPICE Subcircuits (IBIS-ISS)
  - Touchstone
- On-die model separate from package model
- Separate model sets for different analyses:
  - Uncoupled signal integrity
  - Coupled crosstalk
  - Power delivery

New for IBIS: Die Pads



BIRD189.6: IBIS-ISS and Touchstone

```
[Interconnect Model Set]      A1_A3_DQ_TS_XTALK_ISS_PDN

[Interconnect Model]          A1_A3_DQ_TS_buf_pin_XTALK
File_TS  dq_buf_pin_xtalk.s6p
Number_of_terminals = 7
1  Pin_I/O      pin_name      A1    Aggressor_Only
2  Buffer_I/O   pin_name      A1    Aggressor_Only
3  Pin_I/O      pin_name      A2
4  Buffer_I/O   pin_name      A2
5  Pin_I/O      pin_name      A3    Aggressor_Only
6  Buffer_I/O   pin_name      A3    Aggressor_Only
7  Pulldown_ref pin_name      A1
[End Interconnect Model]

[Interconnect Model]          Full_ISS_buf_pin_PDN_2
File_IBIS-ISS   full_iss_buf_pin_pdn_2.iss   full_iss_buf_pad_PDN_2
Number_of_terminals = 4
1  Pin_Rail     signal_name   VDD   |  VDD          POWER
2  Buffer_Rail  signal_name   VDD   |  VDD          POWER
3  Pin_Rail     signal_name   VSS   |  VSS          GND
4  Buffer_Rail  signal_name   VSS   |  VSS          GND
[End Interconnect Model]

[End Interconnect Model Set]
```

Coupled Model

PDN Model

[Thank You]

IBIS Open Forum:
Web: http://www.ibis.org
Email: ibis-info@freelists.org

We welcome participation by all IBIS model makers, EDA tool vendors, IBIS model users, and interested parties.