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Using IBIS-AMI Models to Maximize Performance Given SerDes EQ and Channel ISI & Loss

Donald Telian, SiGuys
Signal Integrity Consultant

AGENDA

- Introduction
- AMI & Equalization
- Maximizing Performance
- Summary

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- Introduction
  - System-level Analysis
  - How SI is Changing
  - SerDes EQ Settings
- AMI & Equalization
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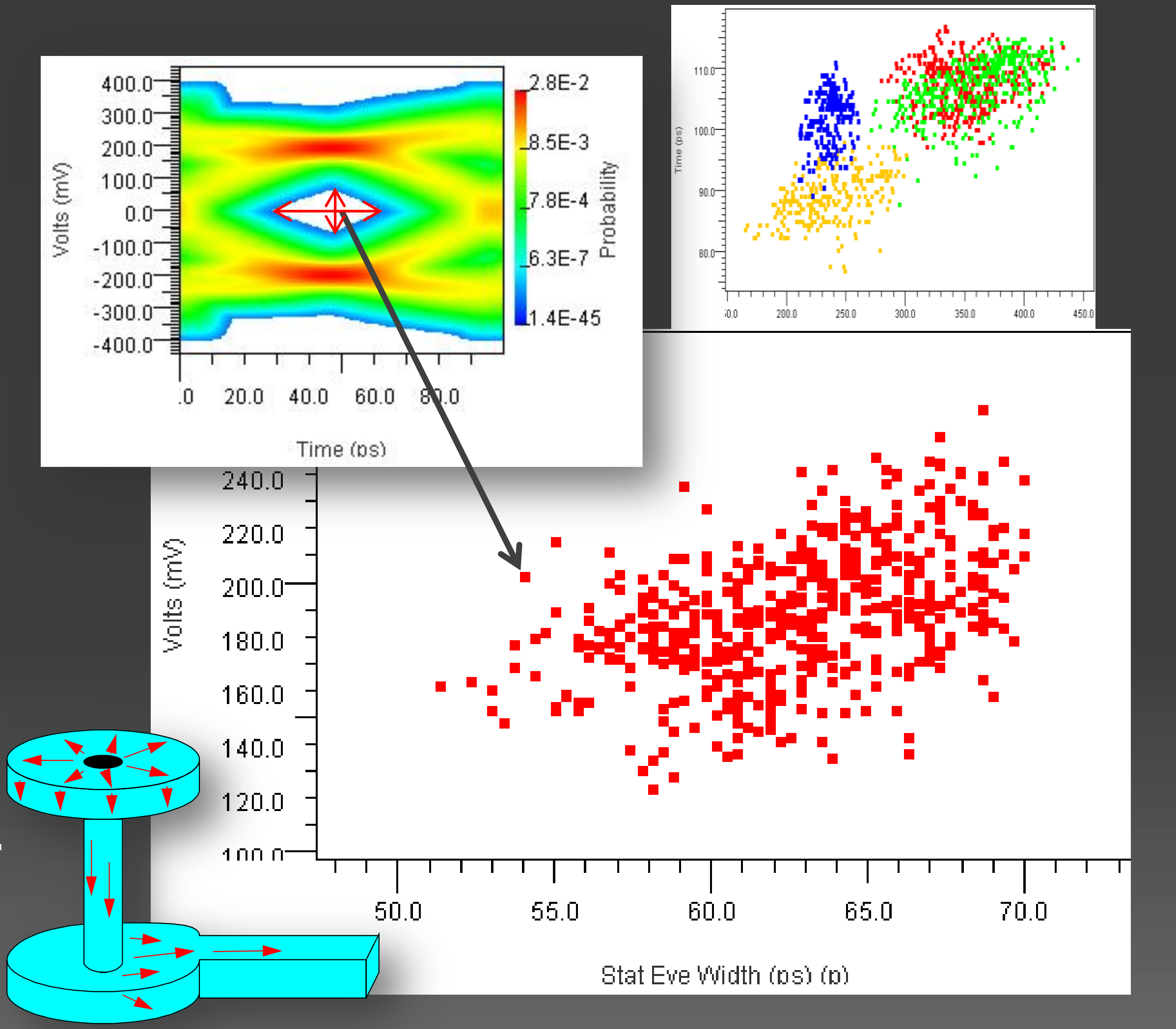
- Summary

SI GUYS

Working at the System-Level

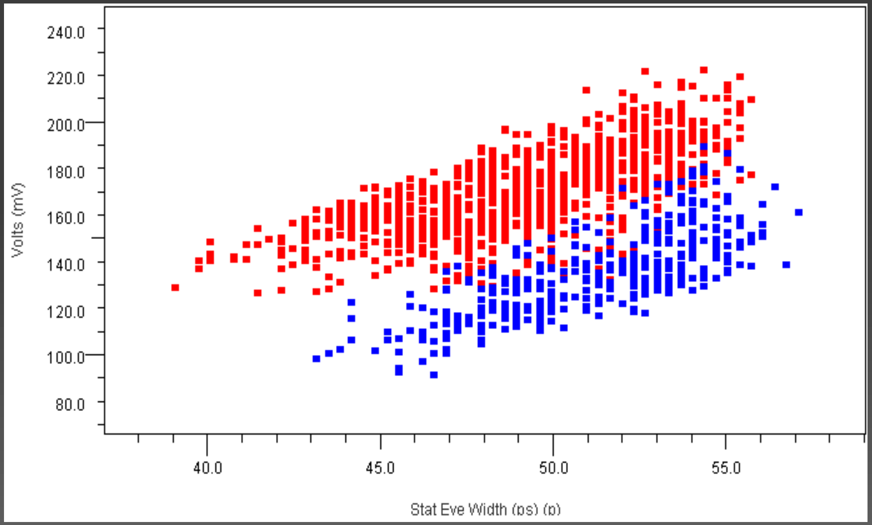
- AMI Models
- Equalization
- Automation
- Visualization
- Abstraction
- Compute Power



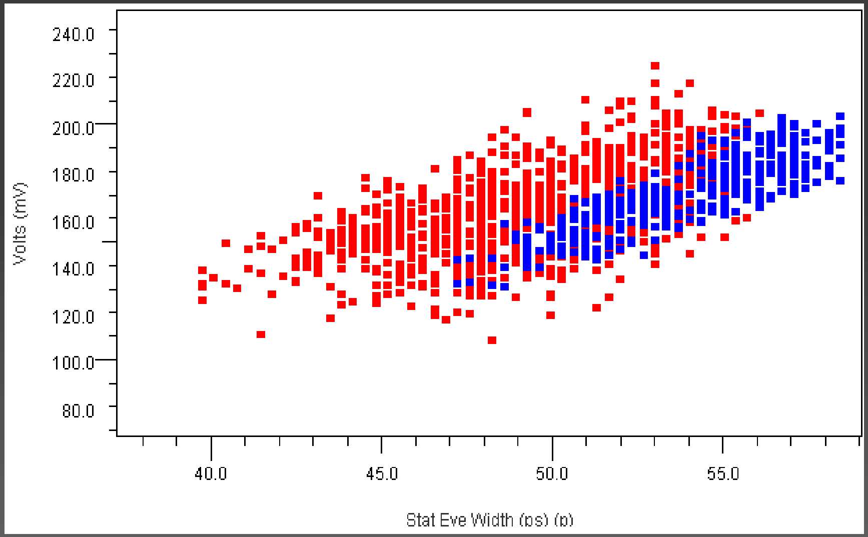
Design Example

- Thousands of links ("serial?")
- "Default" settings typically not ideal
- Blue = long / amplitude_constrained

Default settings



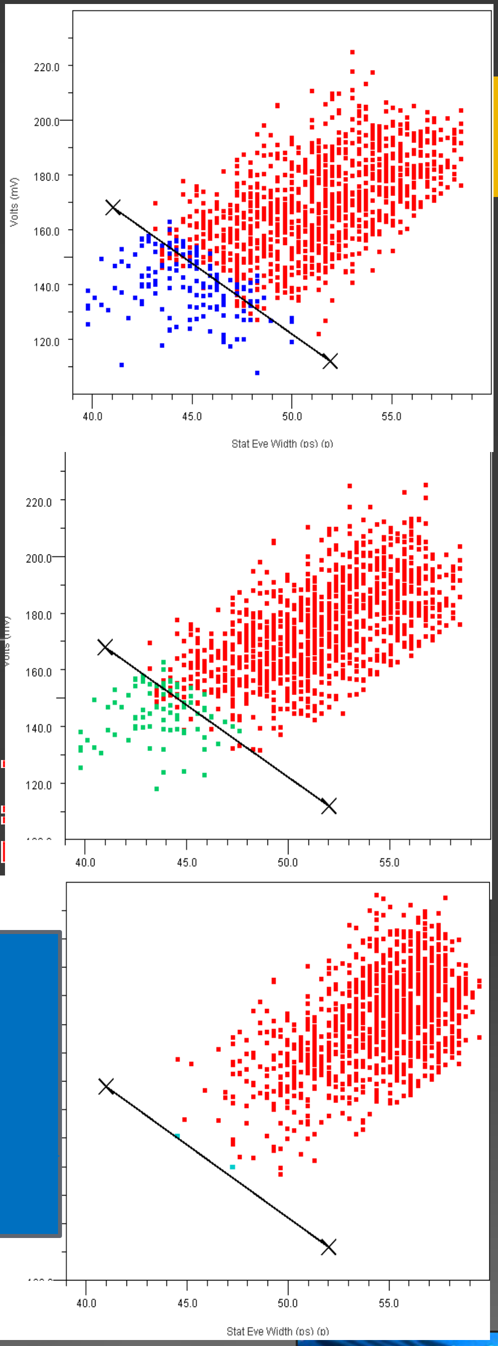
Main Cursor +



"[Moving Higher Data Rate Serial Links into Production](#)" DesignCon 2014 best paper

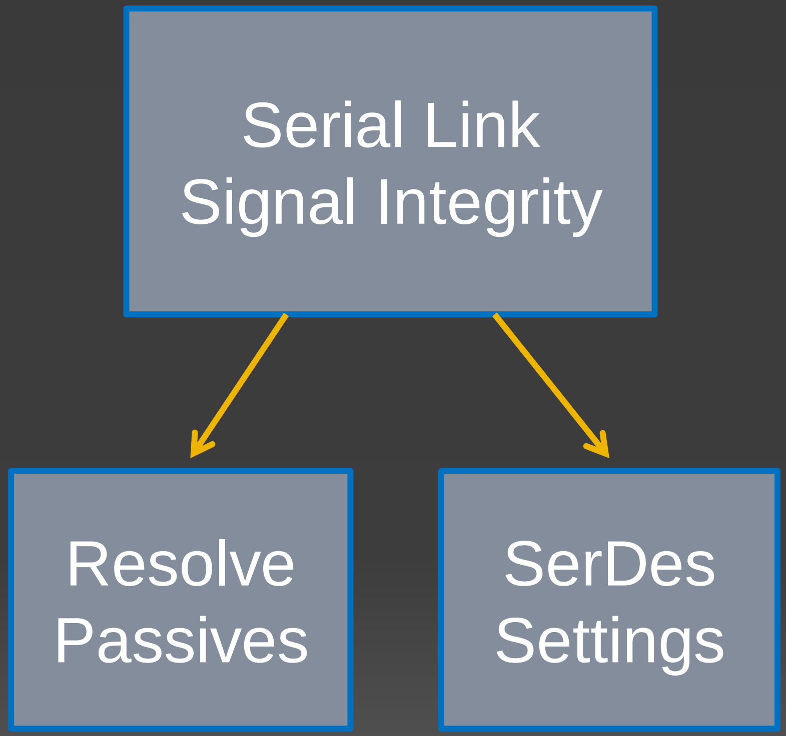
Resolving Performance

- Relevant metric is BER
  - Not eye height and width
    - Combination of eye metrics
  - Diagonal line
- Two corrections necessary
  - Amp+ on medium length links
  - Improve discontinuity on short links
- Significant improve
  - BER=ok
  - Signals clustered



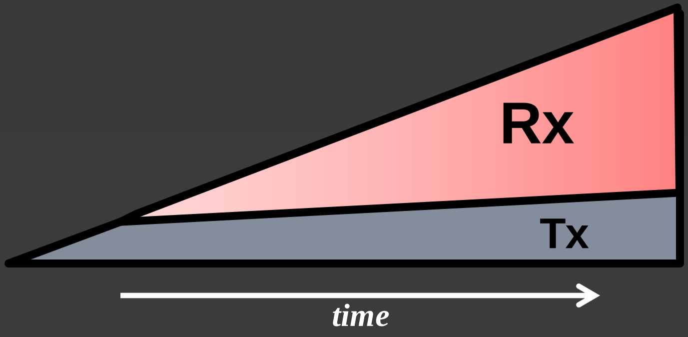
The Changing Face of SI

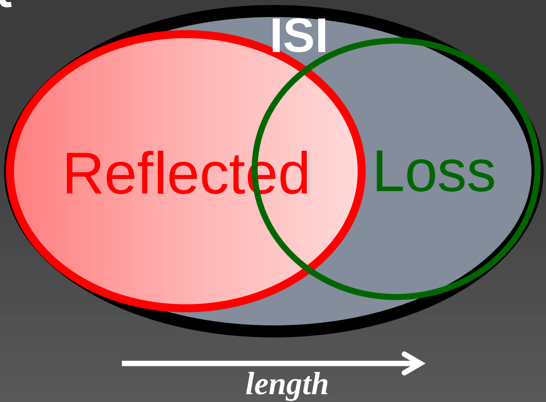
- Passive channel
  - Loss
  - Discontinuities
  - (flight times?!)
- Moving inside ICs
  - Thousands of options
  - Cross-functional
  - More impact



Working with SerDes Settings

- Newer space, growing importance
  - 10” << 01 or 10
- EQ complexity / options
  - PAM4, decreasing margin
  - Must balance Tx with Rx
- “Auto-Negotiation/Training” often isn’t
  - Good goal, will take time to achieve
- Problems not only loss
  - Traditional EQ targets loss
- SW-only fix
  - Rescues failing links





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  - Types of Equalization
  - Pulse Response Analysis
  - Tx/Rx Setting Co-Optimization
- Maximizing Performance
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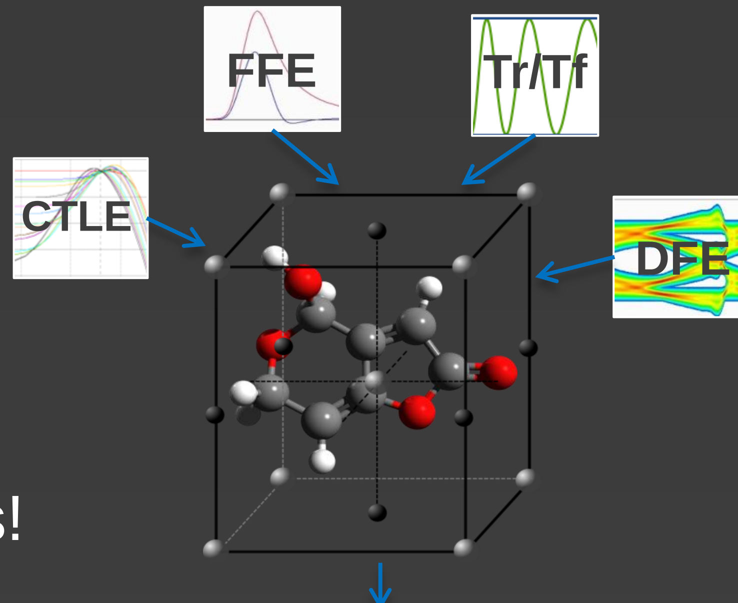
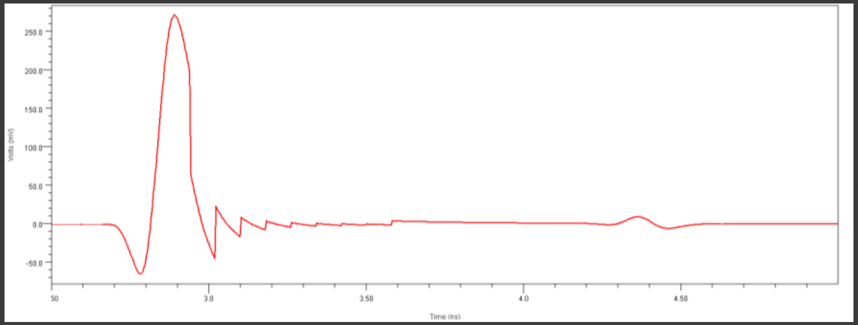
Equalization Using IBIS-AMI

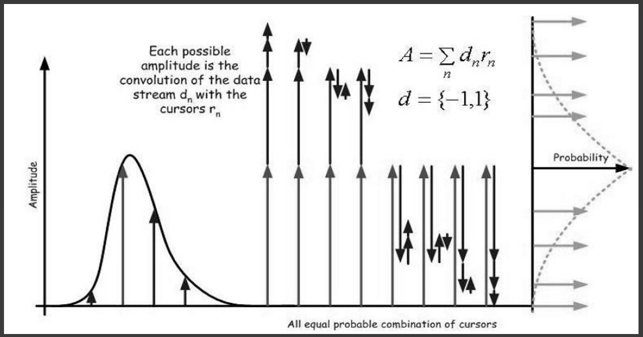
- AMI models
  - Tx = FFE
  - Rx = CTLE, DFE
- Warning:
  - AMI model EQ settings do not always match register settings!
- Need to know
  - What, when, where, how, why
  - Key: pulse response analysis

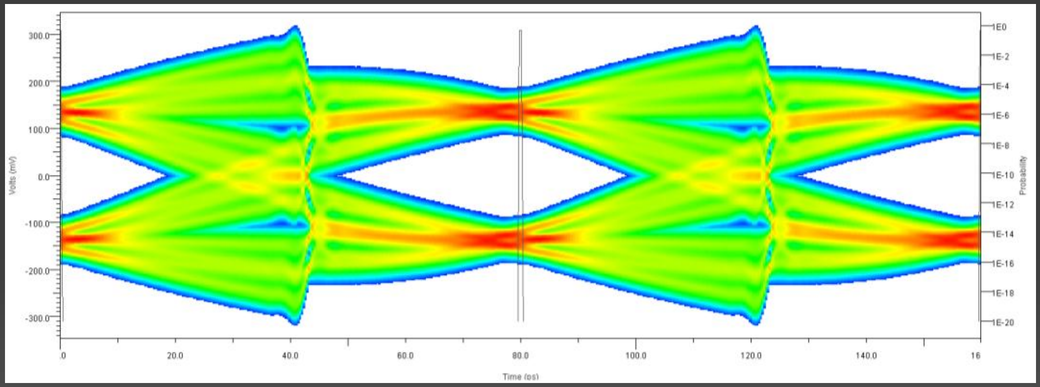


AMI Model

Pulse Response Analysis



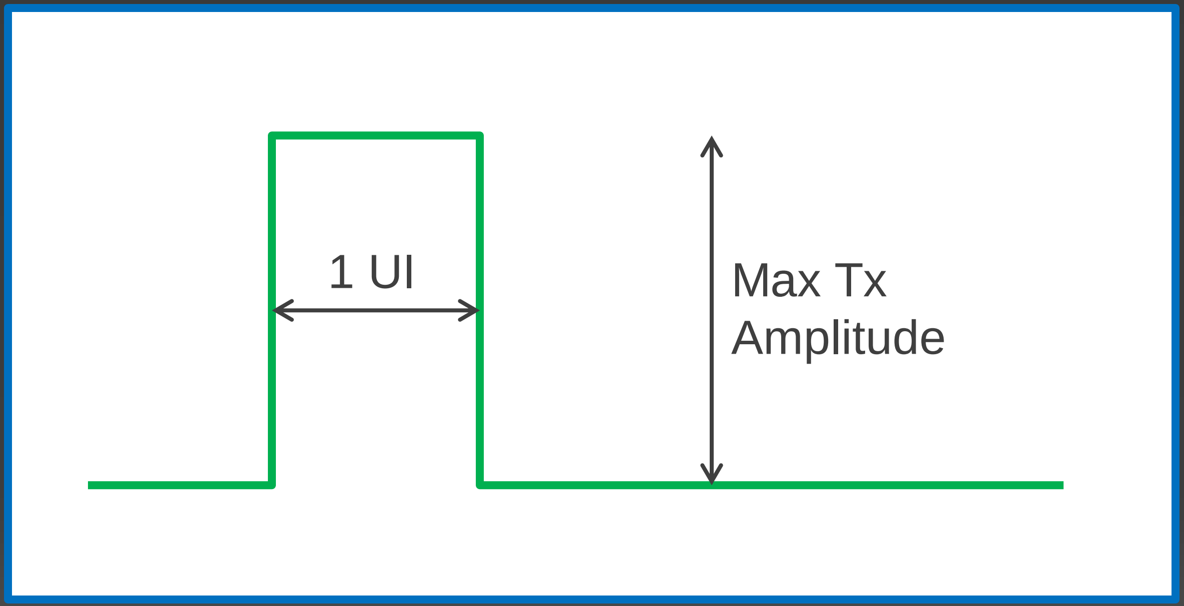




"Channel Compliance Testing Utilizing Novel Statistical Eye Methodology", Anthony Sanders, DesignCon 2004

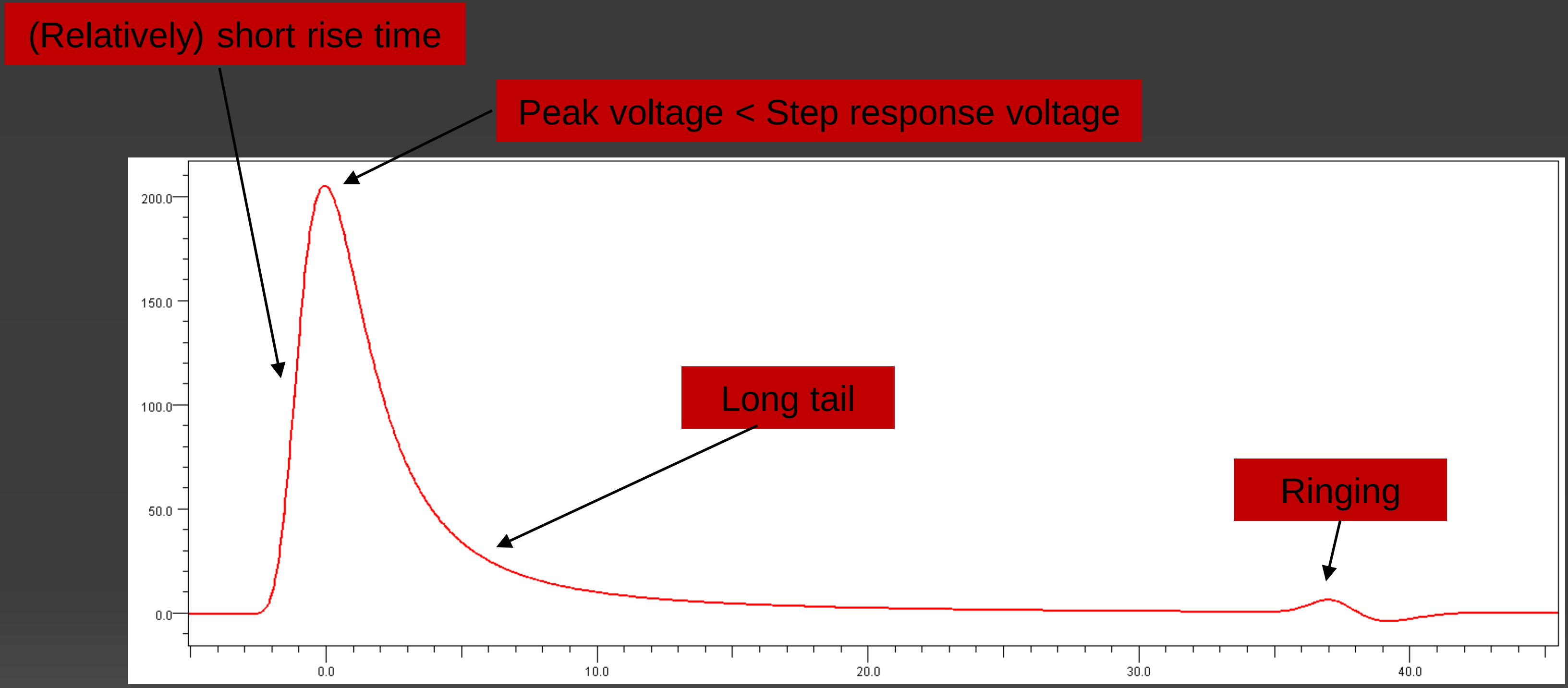
- Eye diagram derived from pulse response through recursive convolution

Ideal Pulse Response



Real Pulse Response

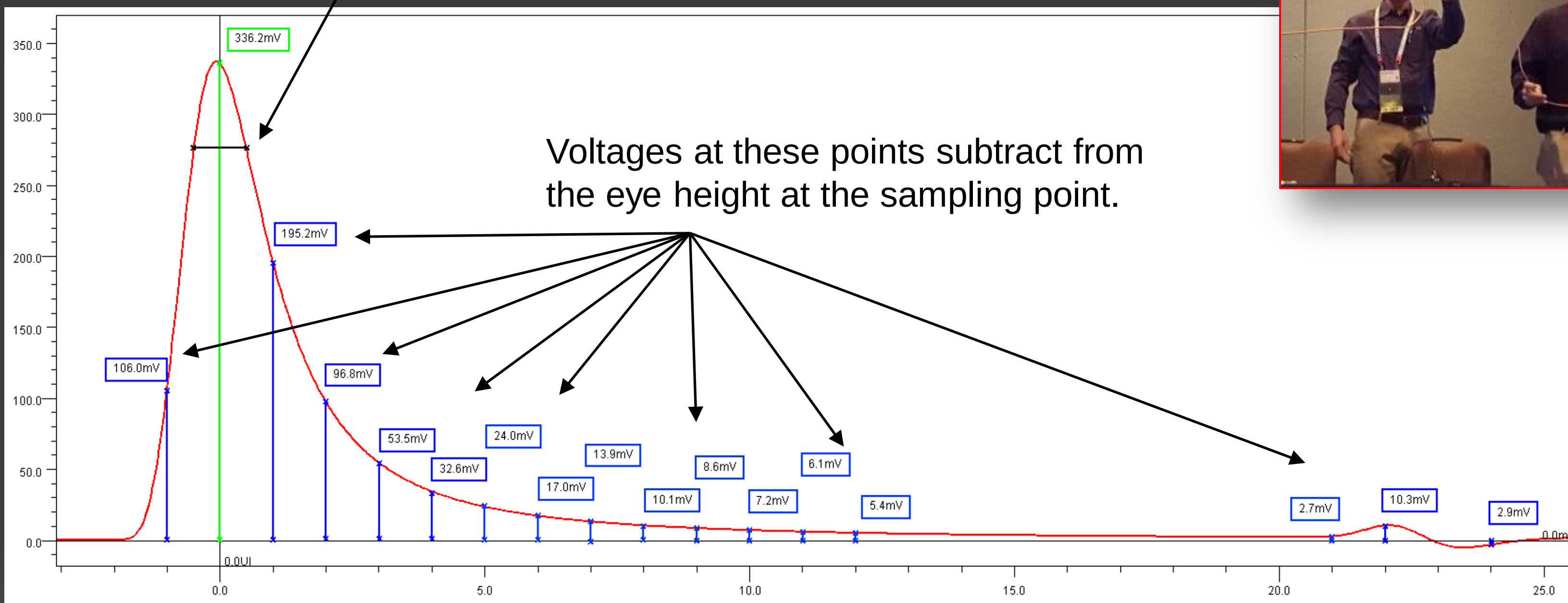
(a.k.a. the Channel Response)



- Requires accurate Tx/Rx analog models to correctly predict ringing due to reflections

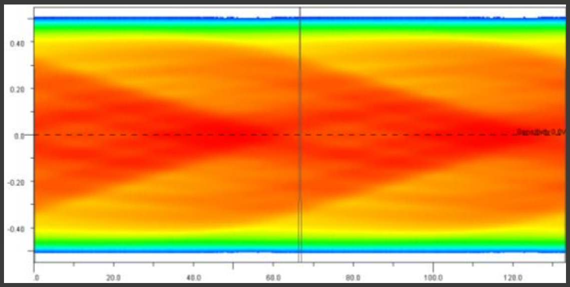
The ISI Pulse Response

Hula hoop algorithm determines clock sampling time.
This is the maximum possible inner eye height.

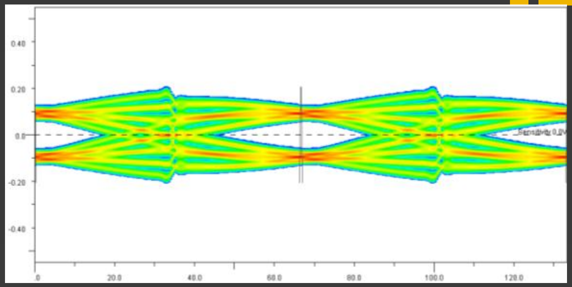


- Voltage and time scales show ISI contributions
- Useful in evaluating EQ & predicting eye opening

Equalization & the Pulse Response

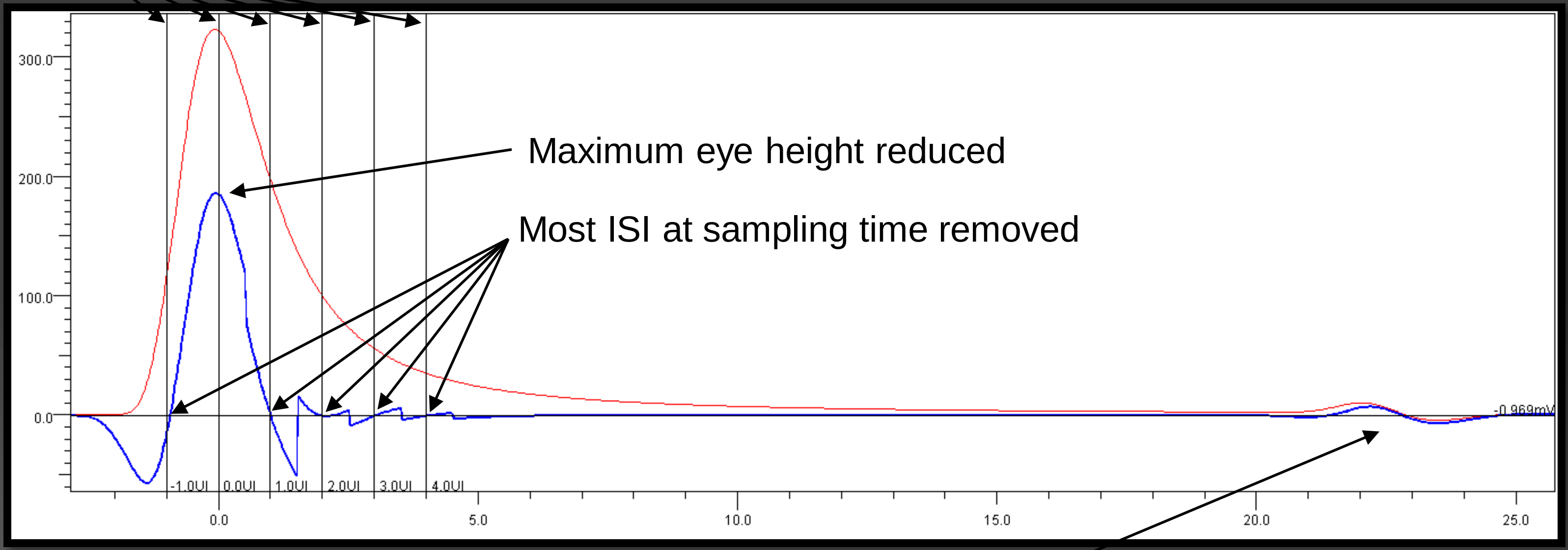


Unequalized



Equalized

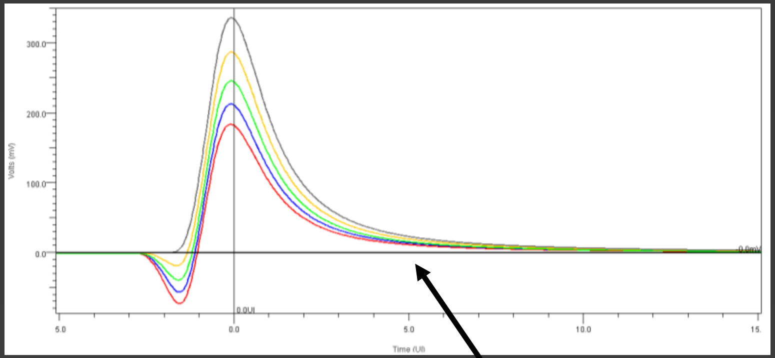
Tx & Rx taps affect the signal here



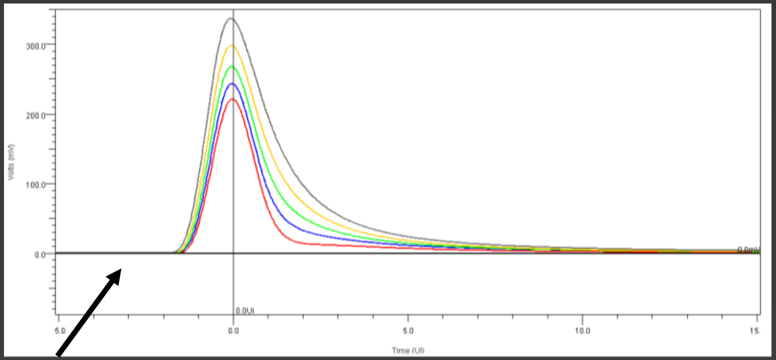
Some ISI cannot be removed

Types of Equalization

Tx Pre-Cursor

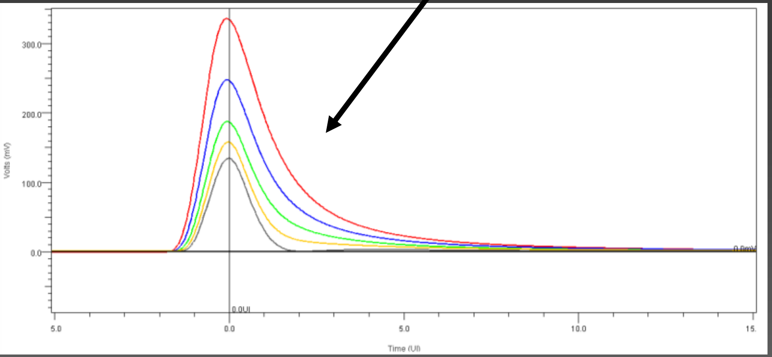


Tx Post-Cursor

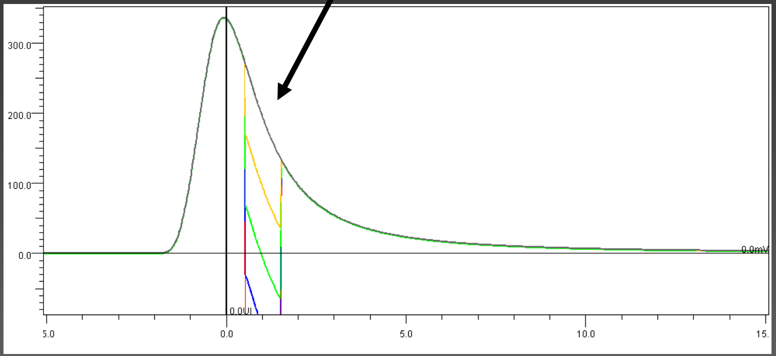


Multiple bit times affected

Single bit time affected



Rx CTLE



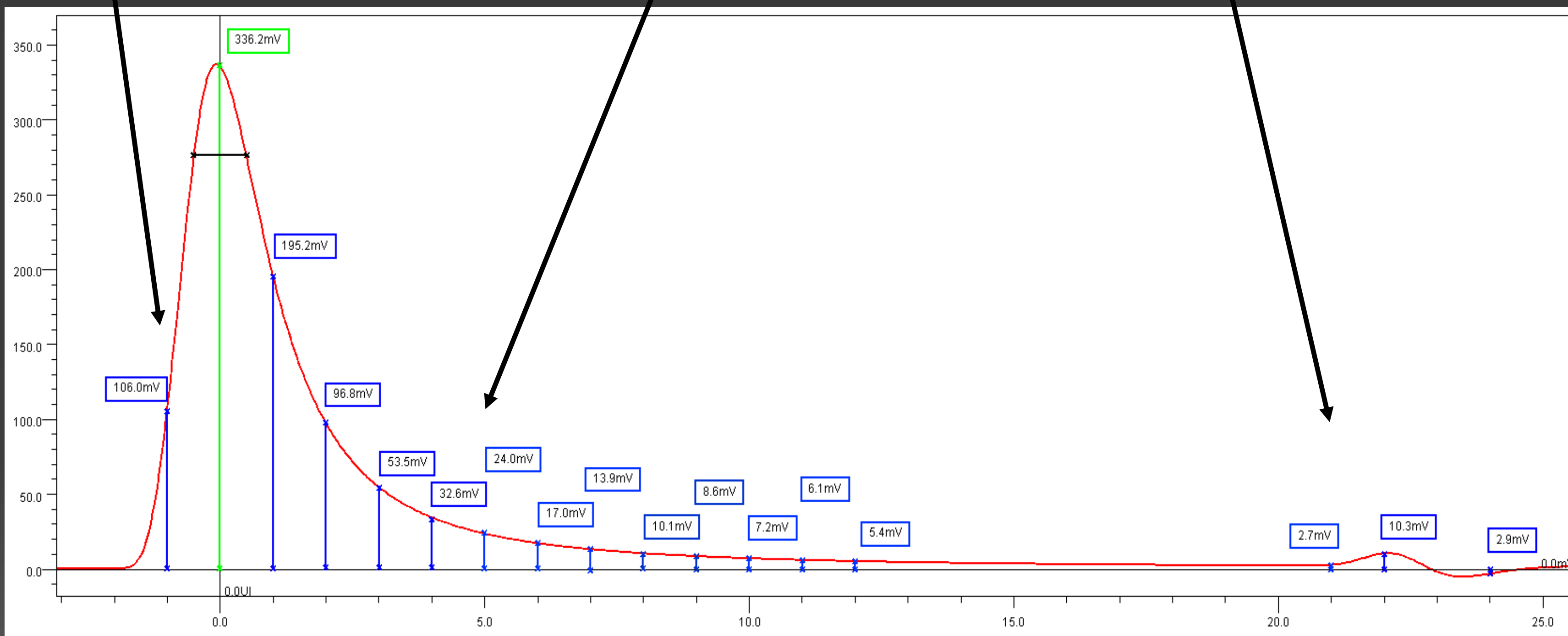
Rx DFE (Tap 1)

Equalizing Pulse Responses

Pre-cursor ISI
Tx pre-cursor is most effective
RX CTLE can help
RX DFE doesn't help at all

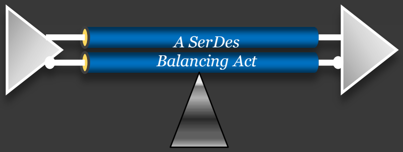
Long tails
Tx post cursor is effective
RX CTLE is sometimes better
RX DFE has limited range

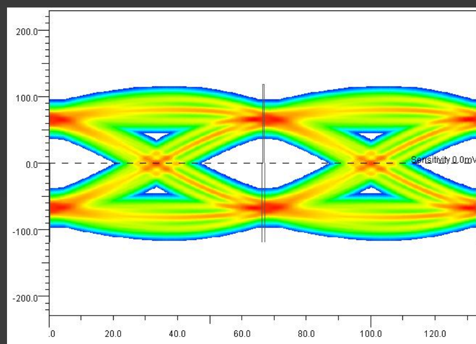
Ringing
Tx and RX CTLE not much help
RX DFE floating taps may help
Bigger issue with short channels



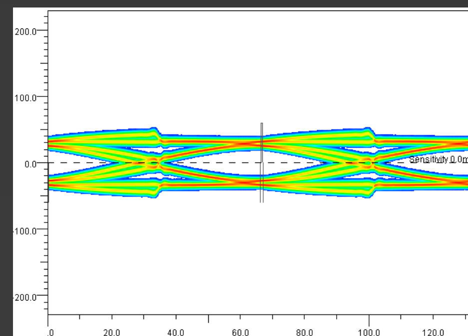
- Long channels: pre-cursor & tail ISI is usually the challenge
- Short channels: ringing is usually the challenge

Evaluating EQ Tradeoffs

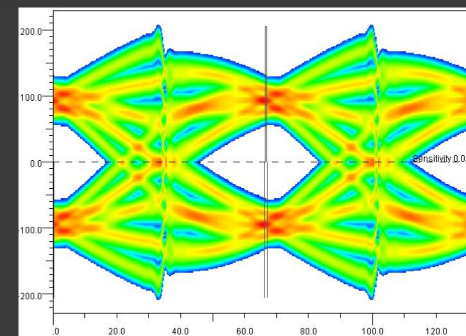




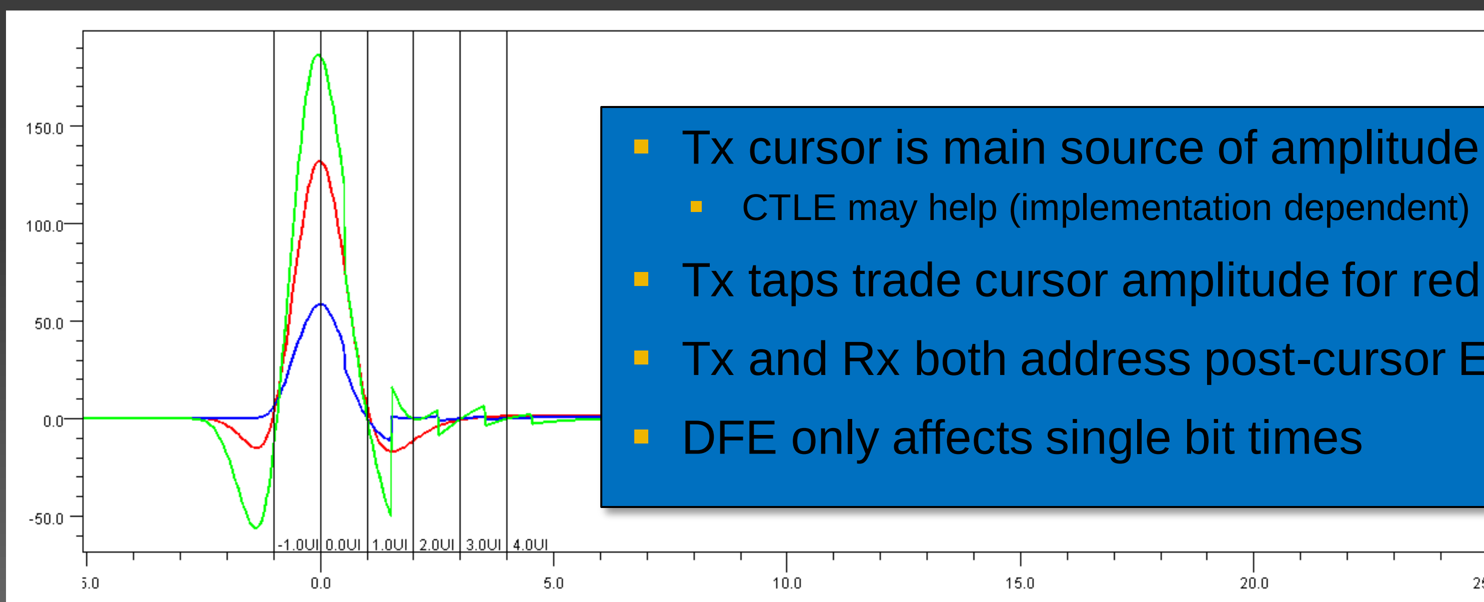
TX Only



RX Only



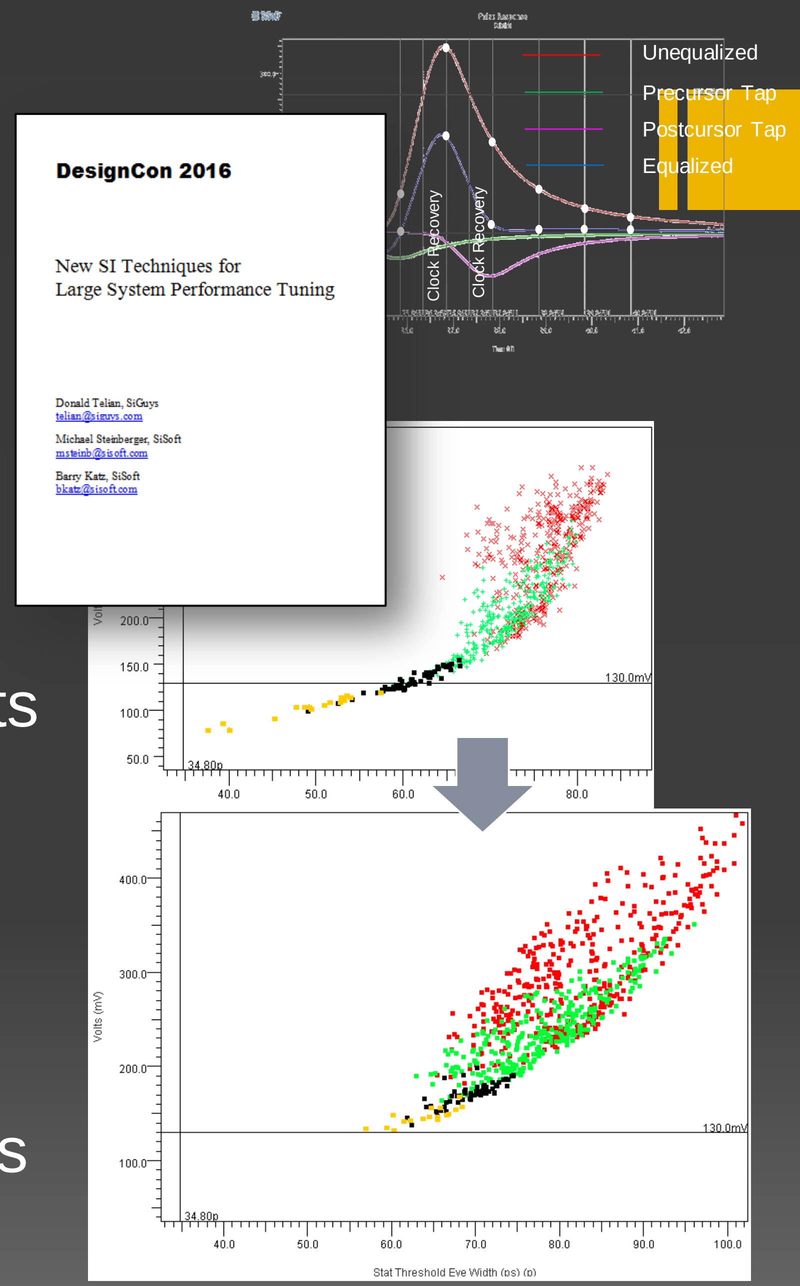
Tx & Rx



- Tx cursor is main source of amplitude
  - CTLE may help (implementation dependent)
- Tx taps trade cursor amplitude for reduced ISI
- Tx and Rx both address post-cursor EQ
- DFE only affects single bit times

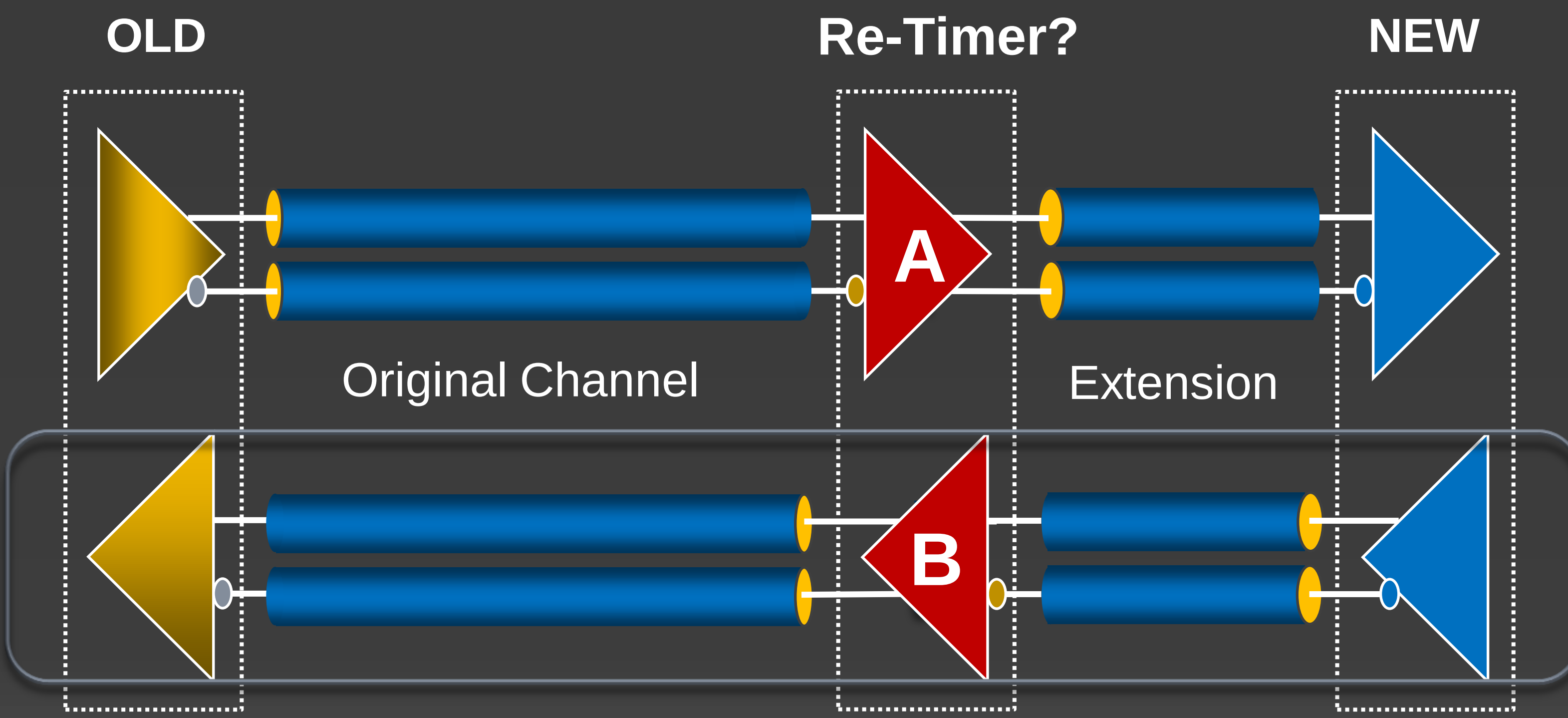
“Co-Optimize” Tx/Rx

- Case Study
  - 60%+ performance gains
  - Allowed 25% longer links
  - Enabled by AMI modeling
  - Removed dozens of components
- Co-Optimization techniques
  - Hula-hoop algorithm
  - Equations for reducing ISI
  - System-level Tx/Rx EQ tradeoffs



“*[New SI Techniques for Large System Performance Tuning](#)*” *DesignCon 2016*

Case Study Scenario



- New cards, newer SerDes, extends channel length
- Can older SerDes succeed? …need a Re-Timer?

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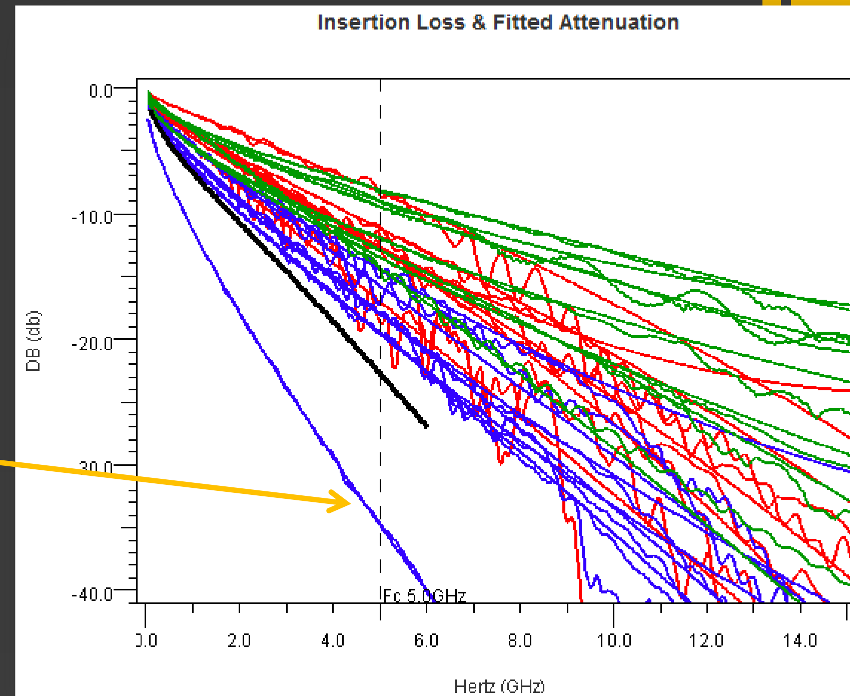
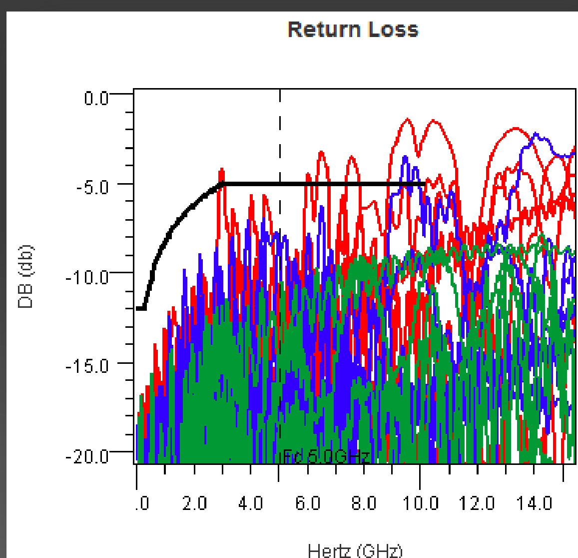
  - S-Parameter Channels
  - Circuit-based Channels
  - PAM4 Channels
- Summary

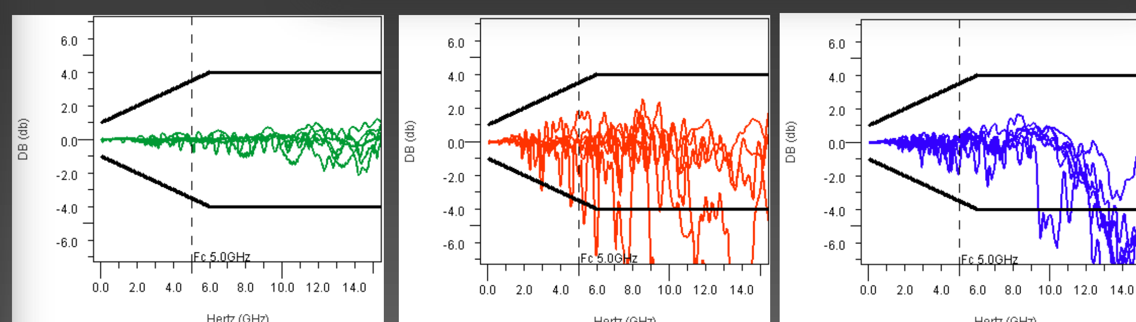
S-Parameter Channels

Range of characteristics

- 7 Industry Channels
- 6 Reflection Channels
- 6 Loss Channels
- 1 Failing Channel

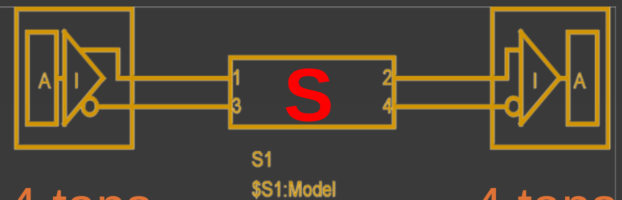






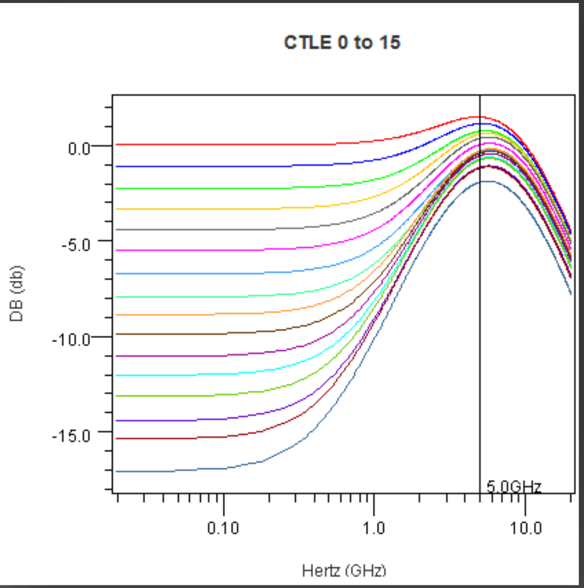
Insertion Loss Deviation

Analysis Setup



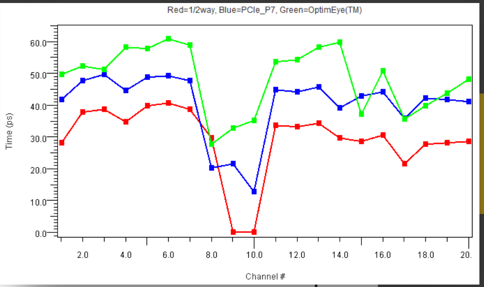
4 taps 4 taps

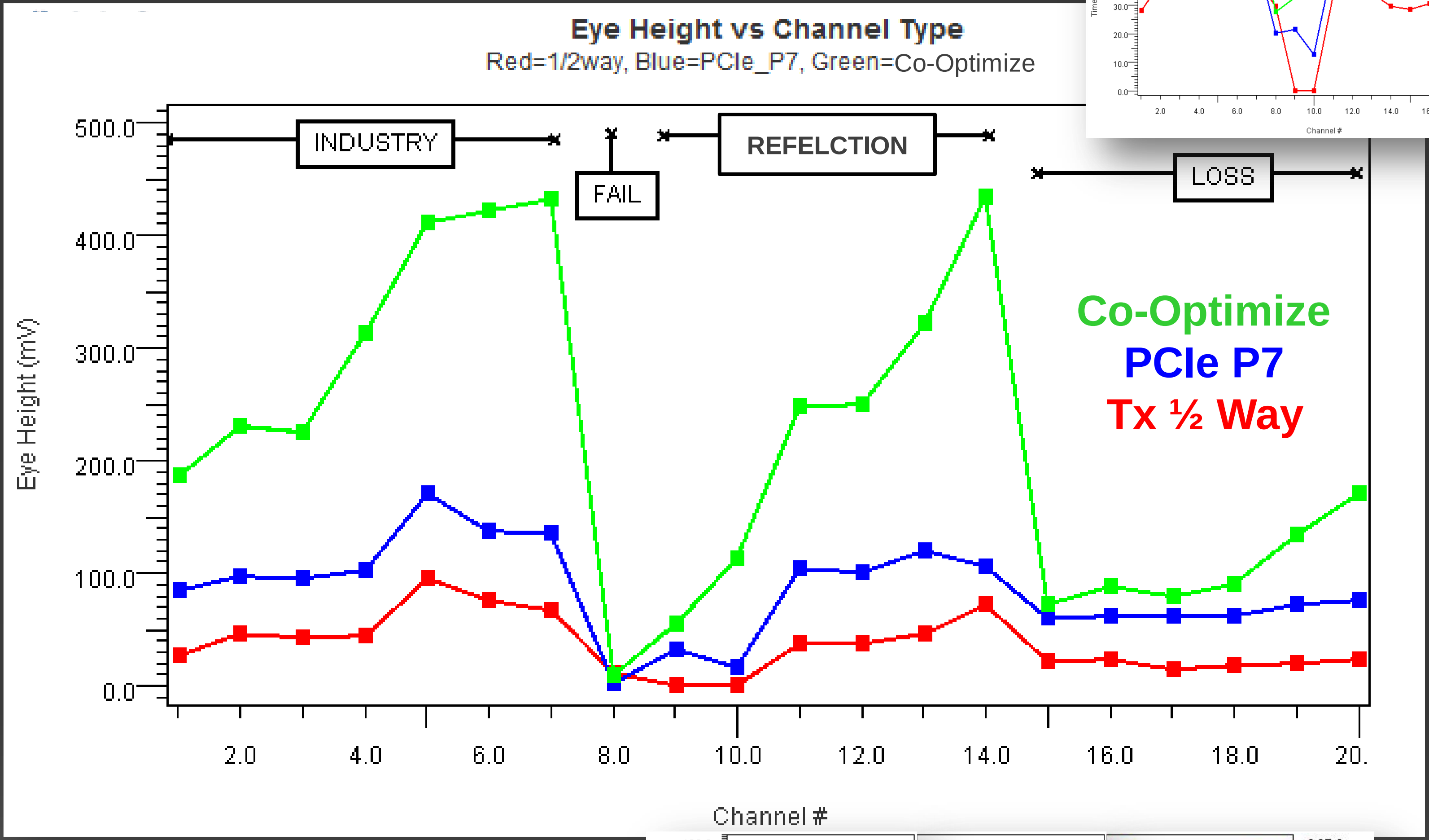
- Circuit
  - s4p channels, 10 Gbps
  - Advanced Tx/Rx w/ Dj, Rj, DCD
- SerDes EQ
  - 4-taps in Tx FFE and Rx DFE
  - Rx CTLE, 0-15, ~0-15dB boost
- EQ Preset Scenarios
  - 1: Tx taps ~half, CTLE=12
  - 2: Tx taps ~PCIe P7, CTLE=8
  - 3: Co-Optimize Tx & Rx CTLE
  - Rx DFE always “auto”



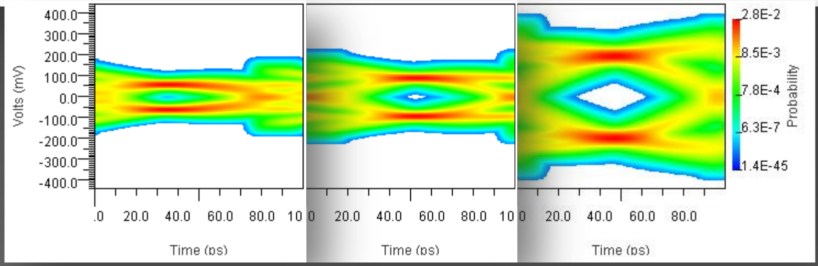
Eye Height Results

Widths:





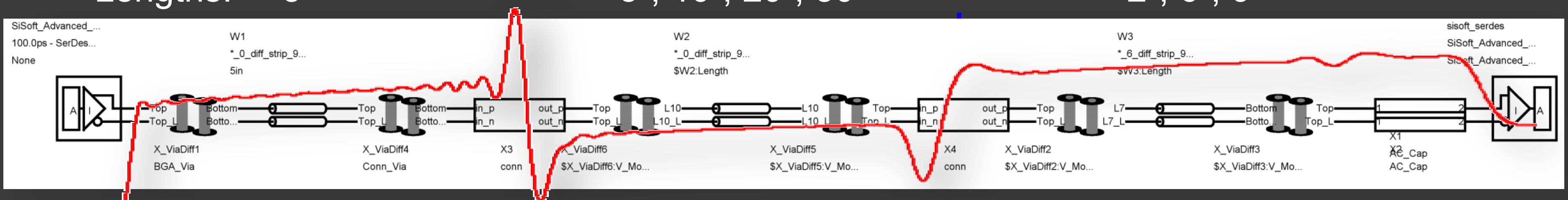
- Typically 2x better
- Eyes for Channel 10:



Circuit-based Channels

Tx Card | **Backplane** | **Rx Card**

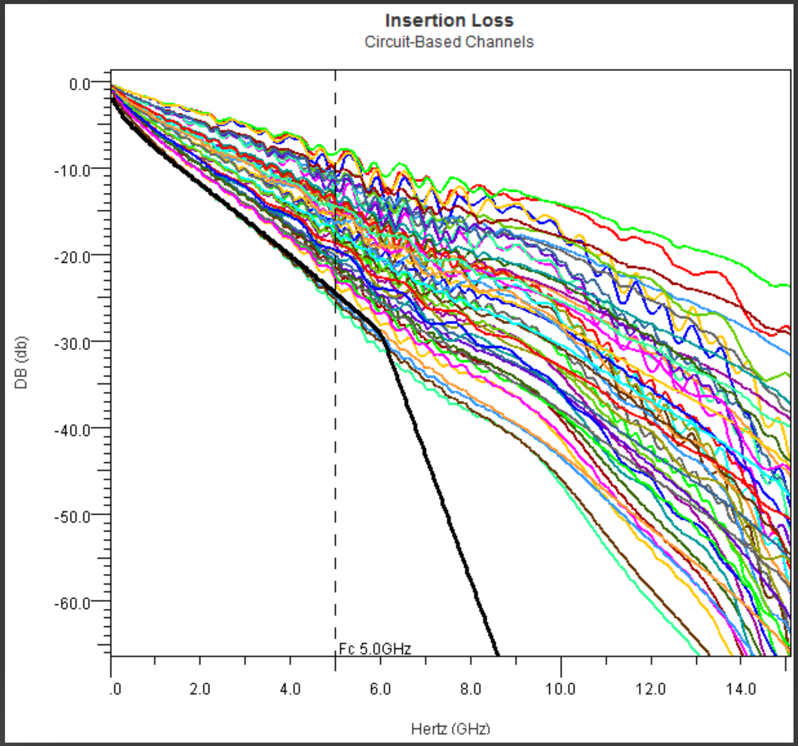
Lengths: 3” | 5”, 10”, 20”, 30” | 2”, 6”, 9”

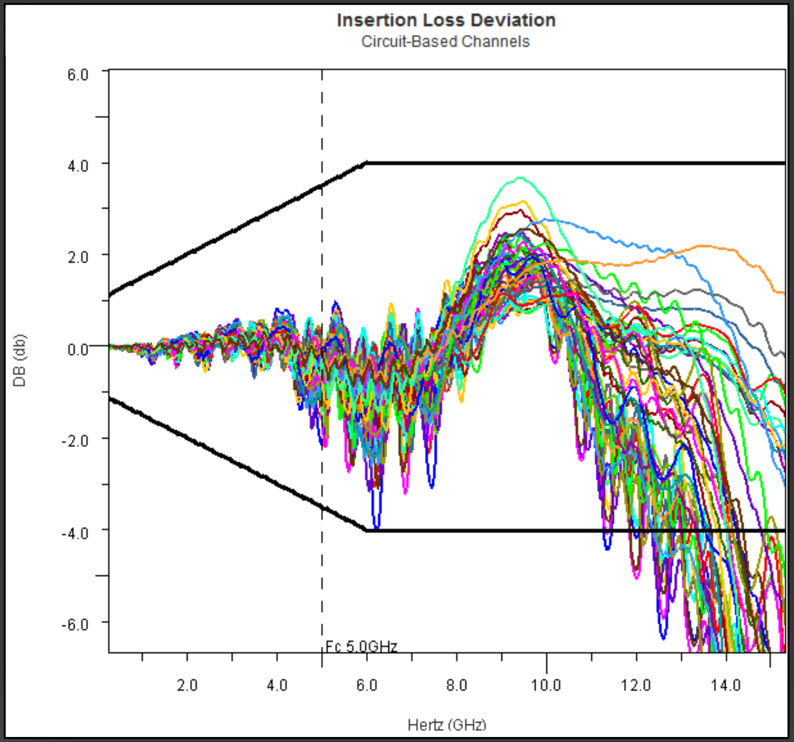


Vias: Long | Long or Shorter w/ Stubs | Long or Shorter w/ Stubs

- 10 Gbps, same EQ options and jitter as S-param channels
- Length: 10” to 42”, Lt_cd/bp: 0.015/0.009, ISI & Loss channels
- Permutations: 4 bp_len * 3 rx_len * 2 bp_via * 2 rx_via = 48
- Total Simulations: 48 * 3 EQ options = 144
- Manufacturing tolerances

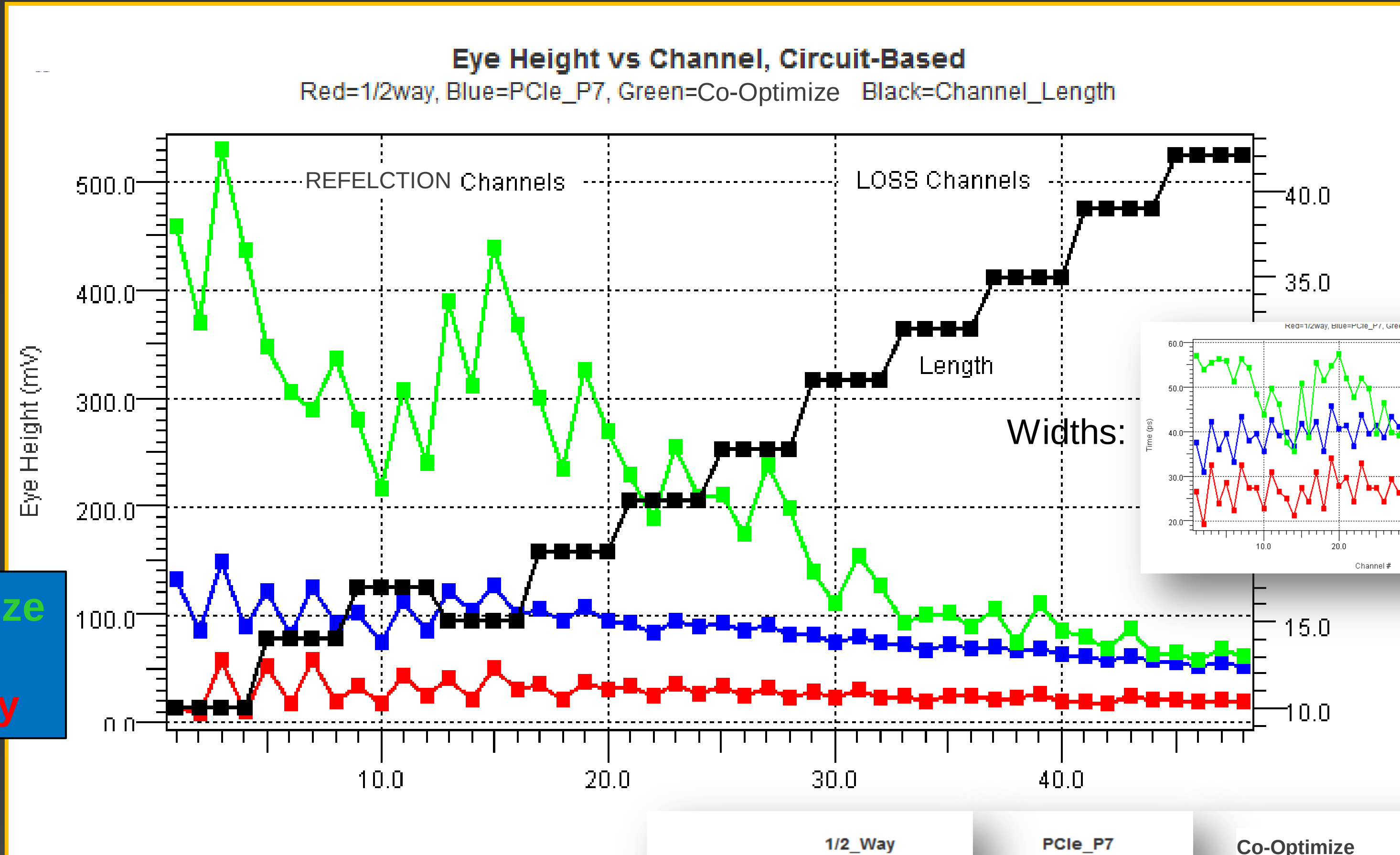
Passive Characteristics, 48 Channels





- Mix of Reflection- & Loss-Dominated Channels
- 20 dB Insertion Loss variation at 5 GHz

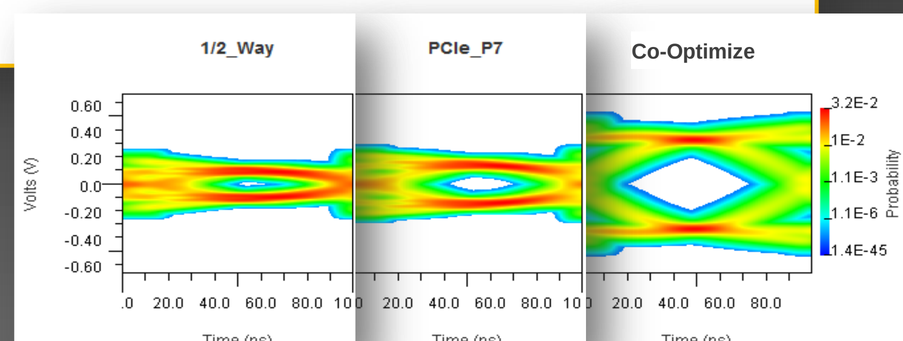
Eye Height Results



Widths:

Co-Optimize
PCIe P7
Tx ½ Way

- Similar trends
- Eyes for Channel 2:

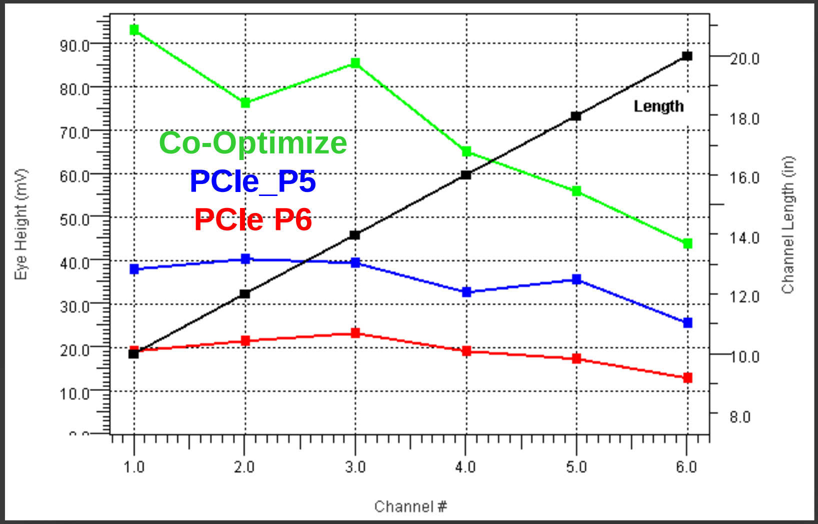


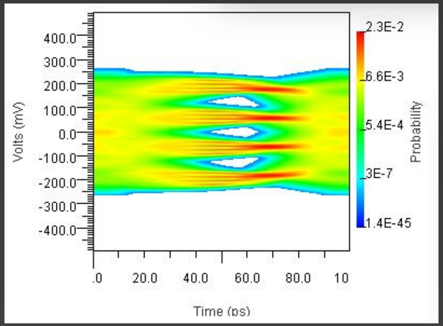
PAM4

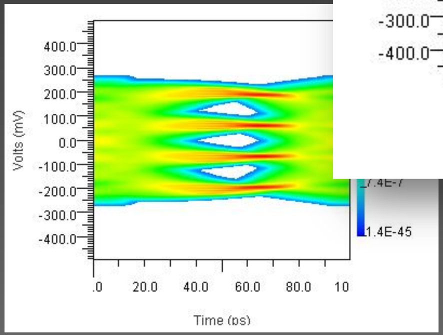
- Co-Optimization becomes imperative

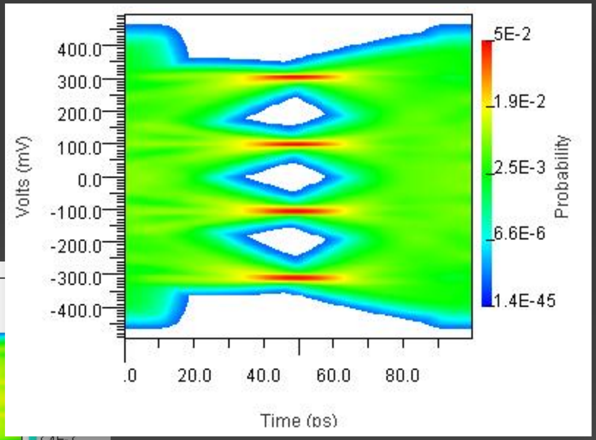
- Channels 10”-20”
- Eye Height vs EQ
  - PCIe_P6
  - PCIe_P5
  - Co-Optimize

- OptimEye ~2x improvement
  - Channel 3 eyes shown









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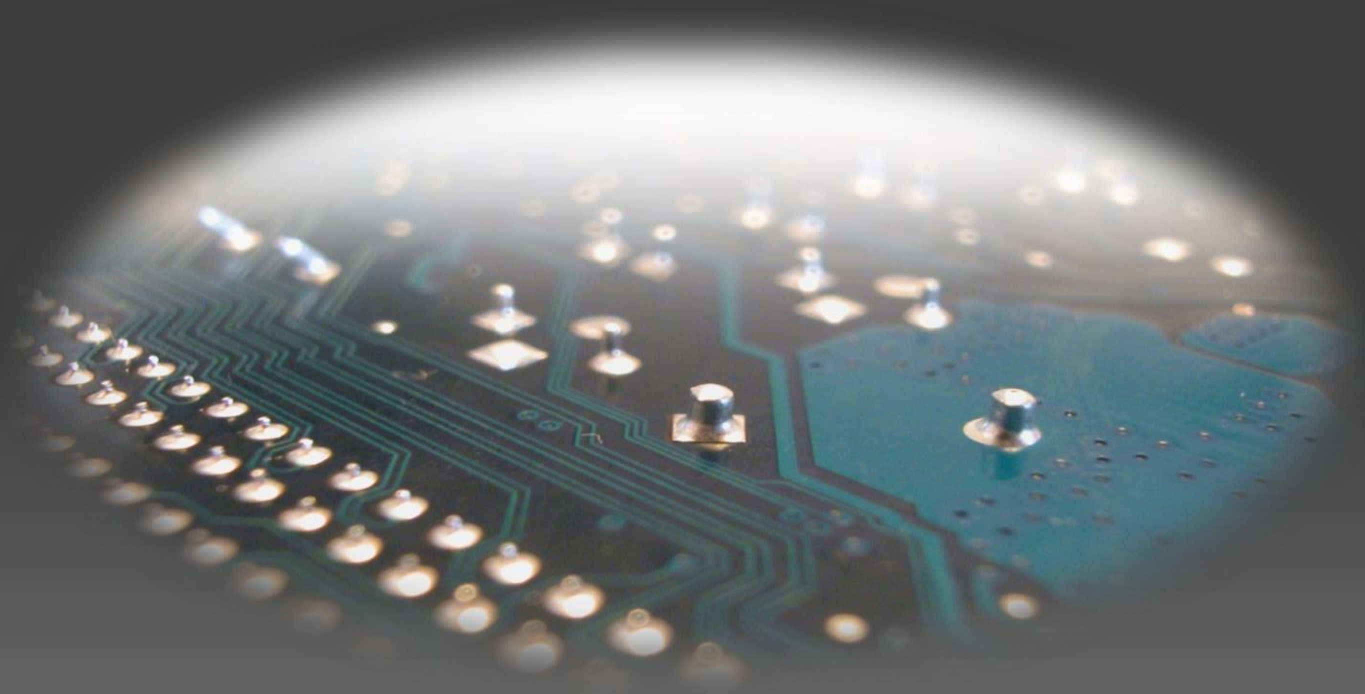
Summary

- Serial Links have gone parallel
- Channel-specific SerDes equalization settings
  - Becoming imperative, new SI task
- Tools for deriving EQ settings
  - IBIS-AMI models
  - Pulse response analysis
  - Tx/Rx co-optimization
- 100% performance gains possible
  - Particularly on reflective channels

THANK YOU



Questions ?