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IBIS + Mpilog: Current and Future Developments on I/O-Buffer Modeling

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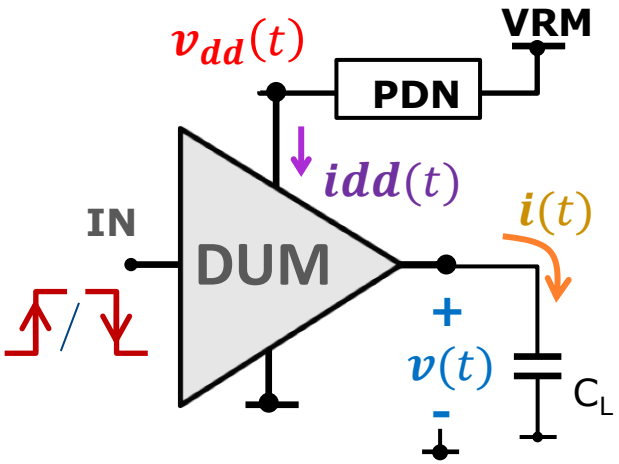
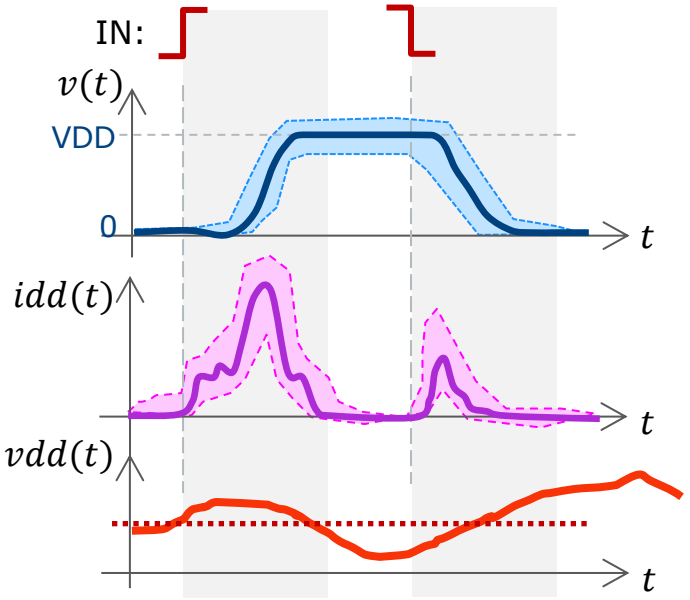
Agenda

1. Macromodels for SI&PI: Requirements
2. IBIS, Two-piece Macromodels & Power-Awareness (?)
3. Enhanced Macromodels (Mpilog-class)
4. Possible Enhancements to IBIS
5. Conclusions

Requirements for I/O Macromodels





Accuracy at Output Port ($v(t)$, $i(t)$)

\+ Supply-Current Profile ($i_{dd}(t)$)

\+ Supply-Voltage Noise ($v_{dd}(t)$)

\+ Supply-Noise Effects ($f(\Delta v_{dd})$)

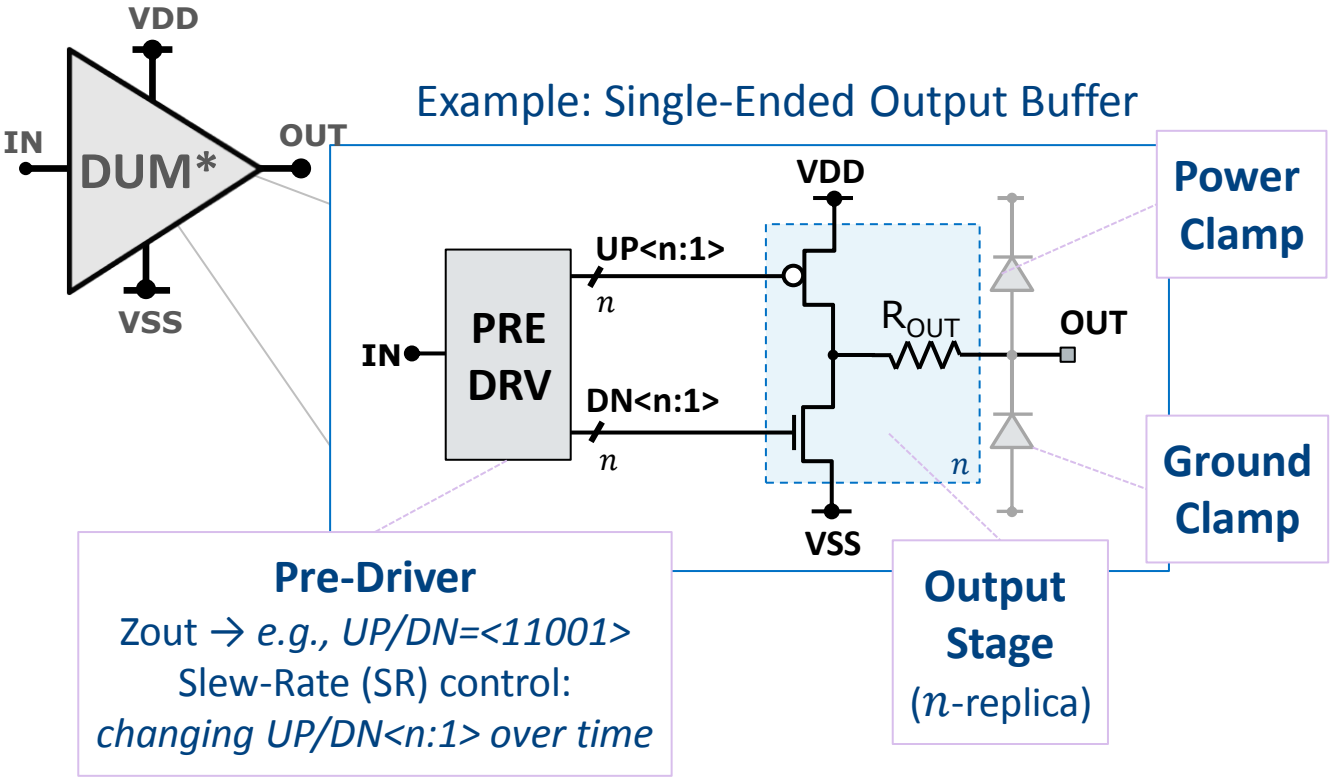
= I/O-buffer model for SI&PI

Targets:

$$\begin{cases} v(t), i(t) \\ v_{dd}(t), i_{dd}(t) \\ \Delta t, \Delta v_{out}, \Delta i_{dd} = f(\Delta v_{dd}) \end{cases}$$

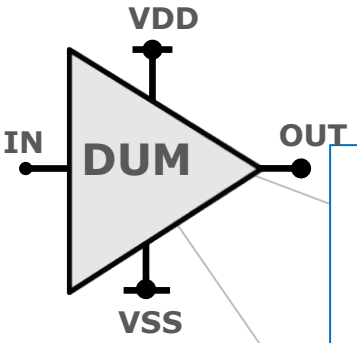
Two-piece Model Structure

**DUM = Device Under Modeling*

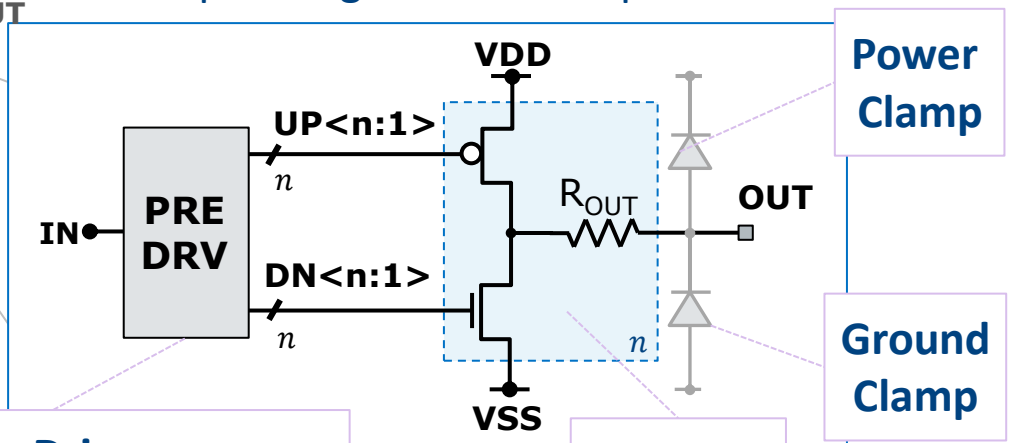


Physical Topology

Two-piece Model Structure



Example: Single-Ended Output Buffer



Pre-Driver

Zout → *e.g., UP/DN=<11001>*

Slew-Rate (SR) control:

changing UP/DN<n:1> over time

Output Stage

(n-replica)

Physical Topology

Pull-Up ***Pull-Down*** ***"Dynamic"***

$$i(t) = w_H(t) \cdot I_{PU}(v) + w_L(t) \cdot I_{PD}(v) - C_{COMP}\frac{\partial v}{\partial t}$$

Up/Down Events

Two-piece Model

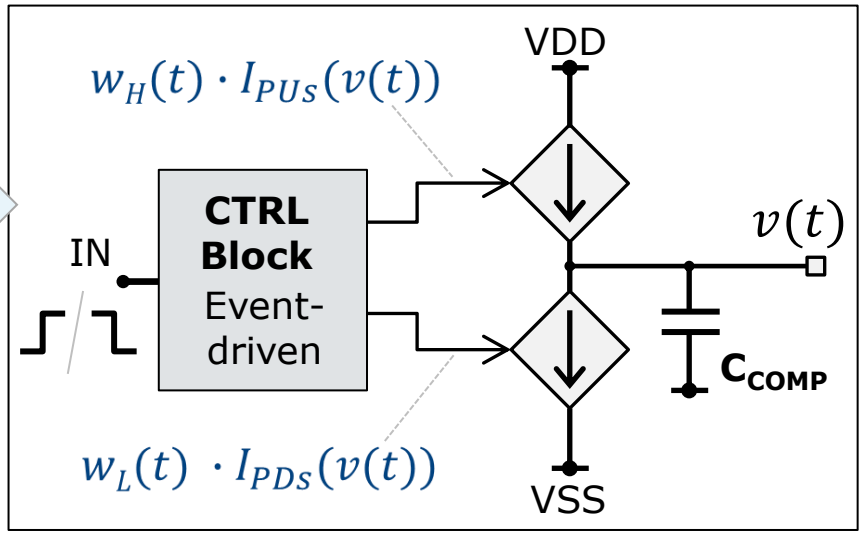
IBIS v3.2 & Two-piece Model Structure

$$i(t) = w_H(t) \cdot I_{PU}(v) + w_L(t) \cdot I_{PD}(v) - C_{COMP}\frac{\partial v}{\partial t}$$

my_ibis.ibs

```
[Model]
 [Pull-Up]
    v1   i1
    v2   i2
    …
 [Pull-Down]
 [C_comp]
 [Rising Waveform]
    t1   v1
    t2   v2
    …
 [Falling Waveform]
```

IBIS v3.2 Equivalent Electrical Circuit



$$i(t), v(t)\ @\ VDD_{NOM} = \text{☺}$$

Limitation: $\begin{cases} i_{dd}(t) = \text{?} \ / \ \text{☹} \\ v_{dd}(t) \neq VDD_{NOM} \Rightarrow \text{???} \ / \ \text{☹} \end{cases}$

Power-awareness in IBIS (v5.0)

$$i(t) = w_H(t) \cdot I_{PU}(v) + w_L(t) \cdot I_{PD}(v) - C_{COMP}\frac{\partial v}{\partial t}$$ *IBIS v3.2*

"Power-Aware" Two-piece Model

$$i(t) = w_H(t) \cdot K_{SSOPU}(\Delta v_{dd}) \cdot I_{PU}(v) + w_L(t) \cdot K_{SSOPD}(\Delta v_{ss}) \cdot I_{PD}(v) - C_{COMP}\,\partial v/\partial t$$

$$i_{dd}(t) = w_H(t) \cdot K_{SSOPU}(\Delta v_{dd}) \cdot I_{PU}(v) + \partial i(t)$$

IBIS v5.0

KSSO_PU/PD introduce **approximations** of supply/ground noise on output static characteristics

Supply-current is explicitly modeled, and corresponds to **pull-up** and **"crow-bar"/other current** contributions

Power-awareness in IBIS (v5.0)

"Power-Aware" Two-piece Model = IBIS v5.0

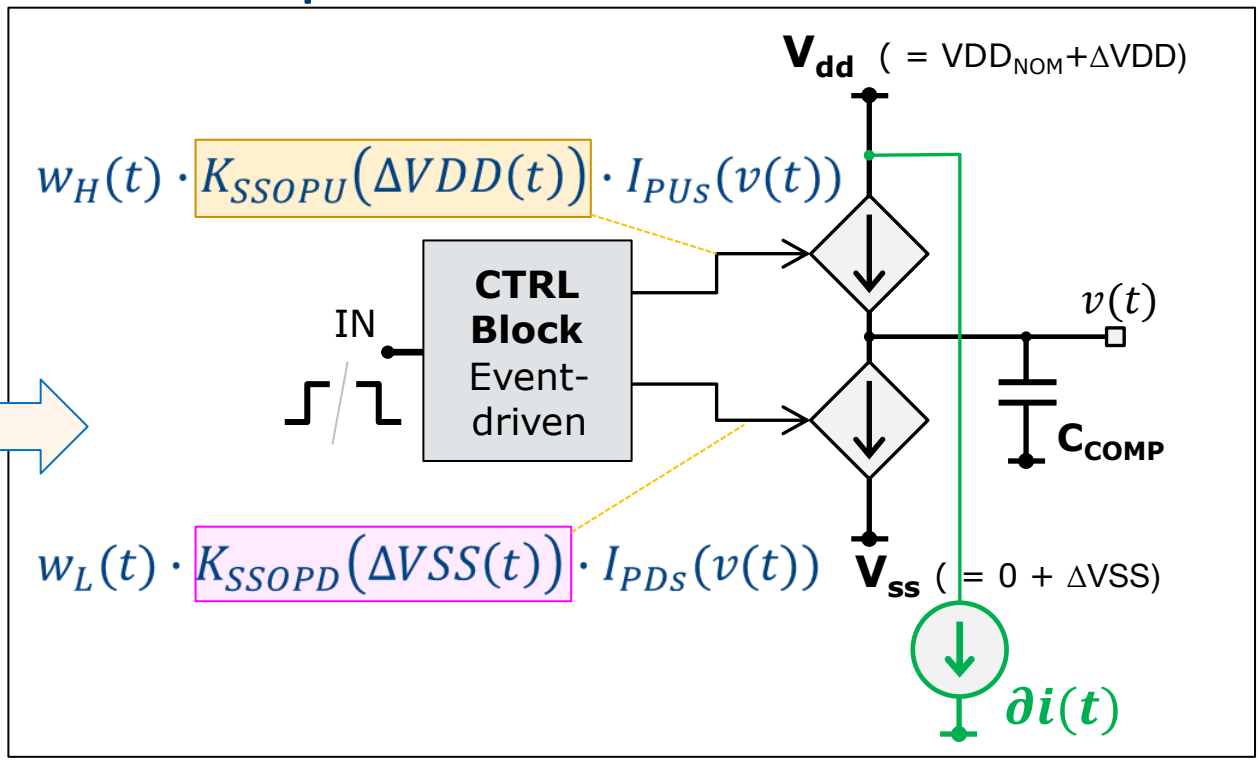
$$i(t) = w_H(t) \cdot K_{SSOPU}(\Delta v_{dd}) \cdot I_{PU}(v) + w_L(t) \cdot K_{SSOPD}(\Delta v_{ss}) \cdot I_{PD}(v) - C_{COMP}\frac{\partial v}{\partial t}$$

$$i_{dd}(t) = w_H(t) \cdot K_{SSOPU}(\Delta v_{dd}) \cdot I_{PU}(v) + \partial i(t)$$

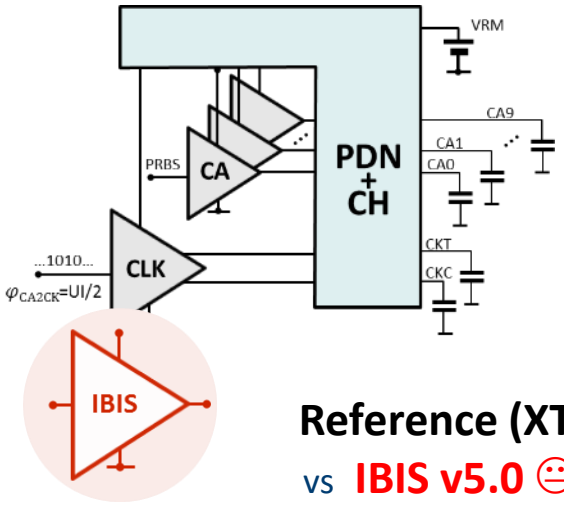
my_ibis_v5.ibs

```
[Model]
   [Pull-Up]
   [Pull-Down]
   [ISSO PU]
   [ISSO PD]
   [C_comp]
   [Rising Waveform]
     [Composite Current]
   [Falling Waveform]
     [Composite Current]
```

IBIS v5.0 Equivalent Electrical Circuit



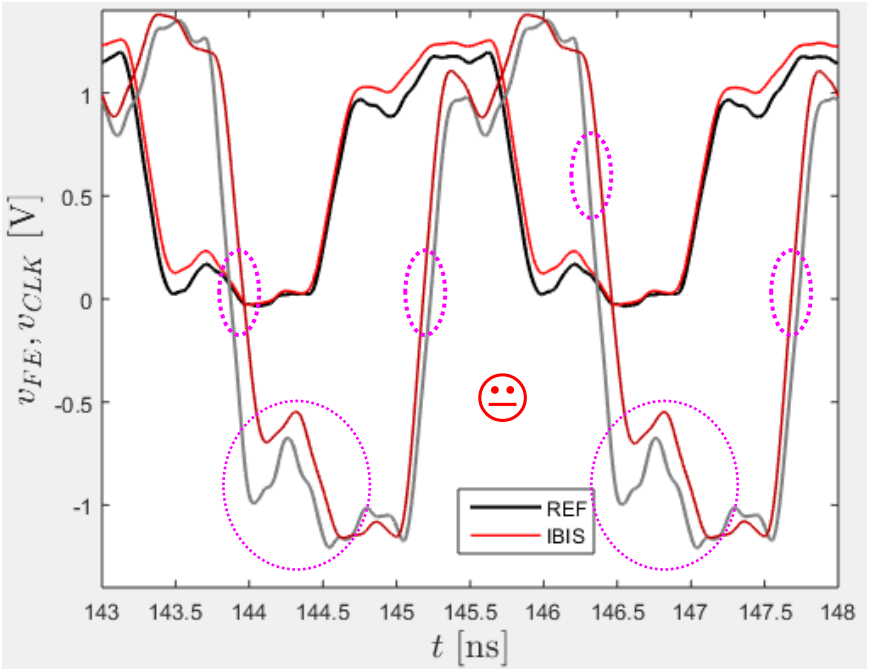
Validation



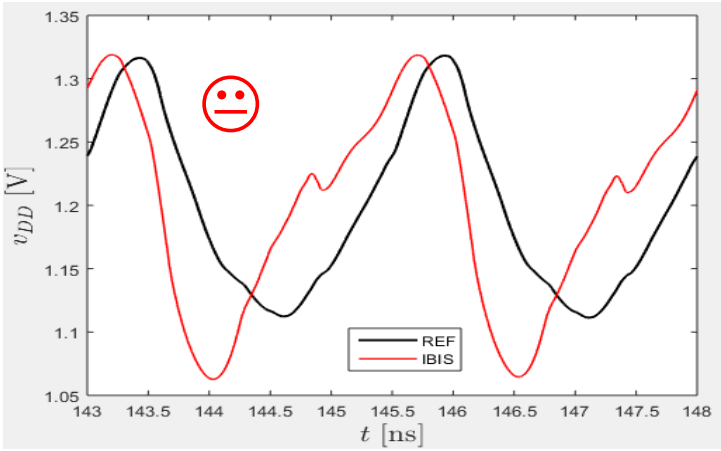
Reference (XTOR-level)

vs **IBIS v5.0** 😐

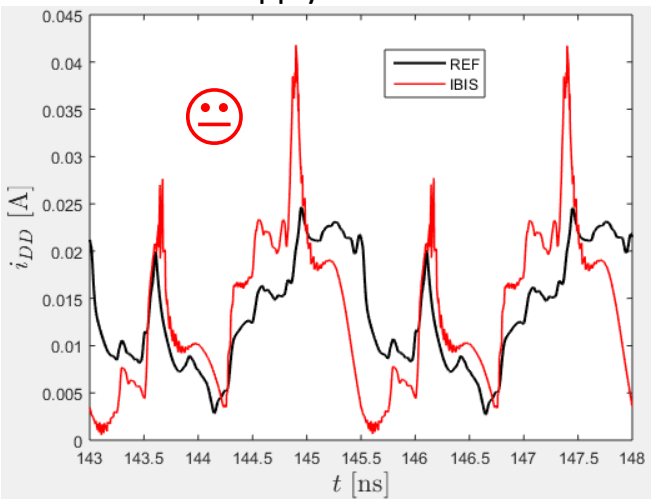
CLK/DATA Far-End Signals



Supply-Noise

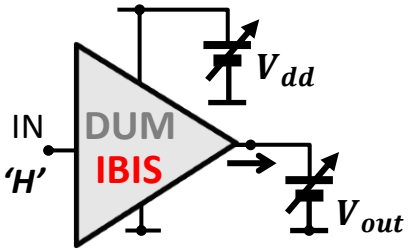


Supply-Current

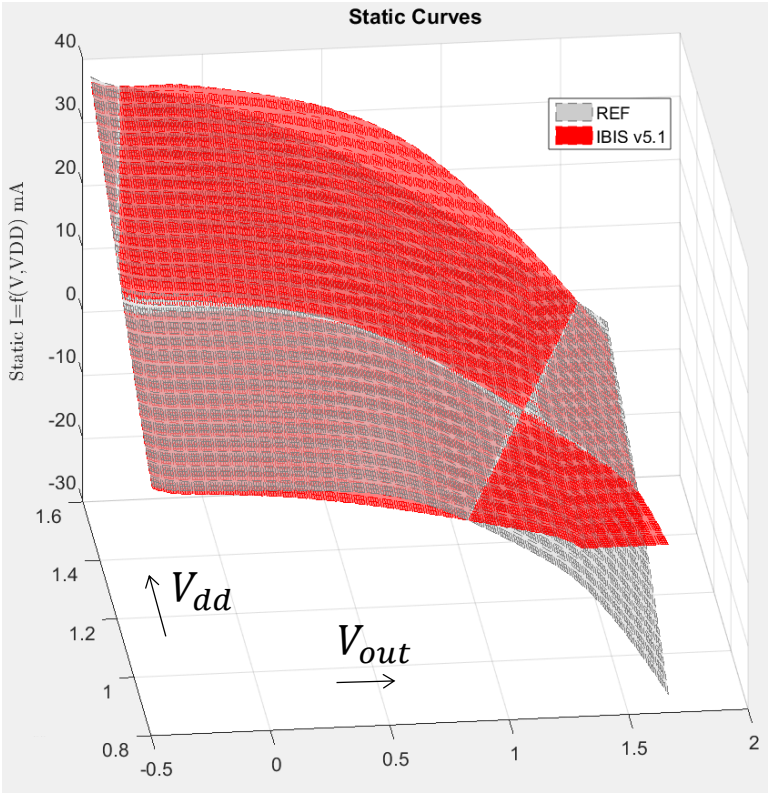


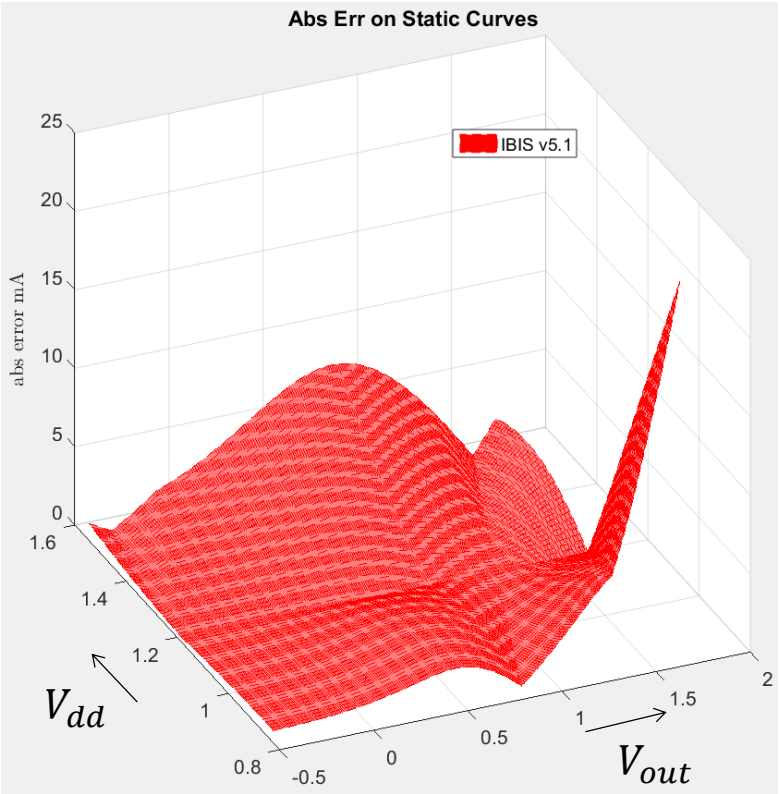
VDD ⇔ Static Characteristics

Nested .DC sweep
on Output and Supply ports



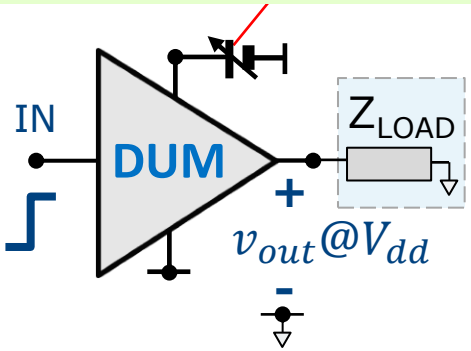
Possible inaccuracy with ISSO_PU(PD) approximation ?

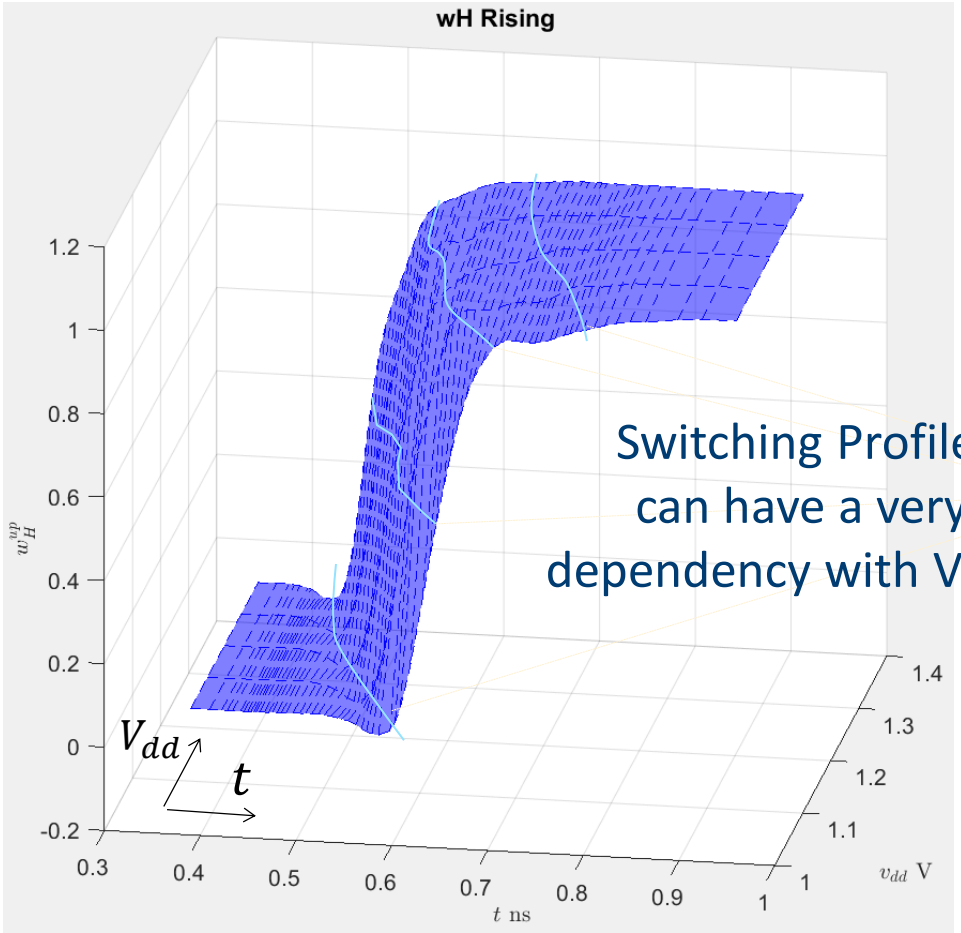




VDD ⇔ Rising/Falling Waveforms

$V_{dd} \in [80\%, \ldots, 100\%, \ldots, 120\%] \times V_{DD,NOM}$



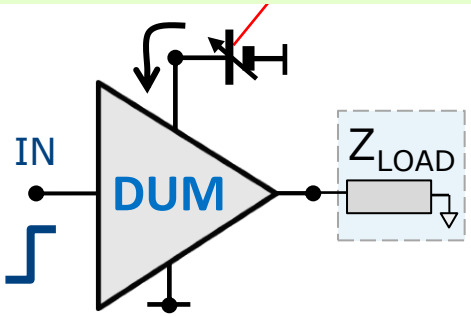


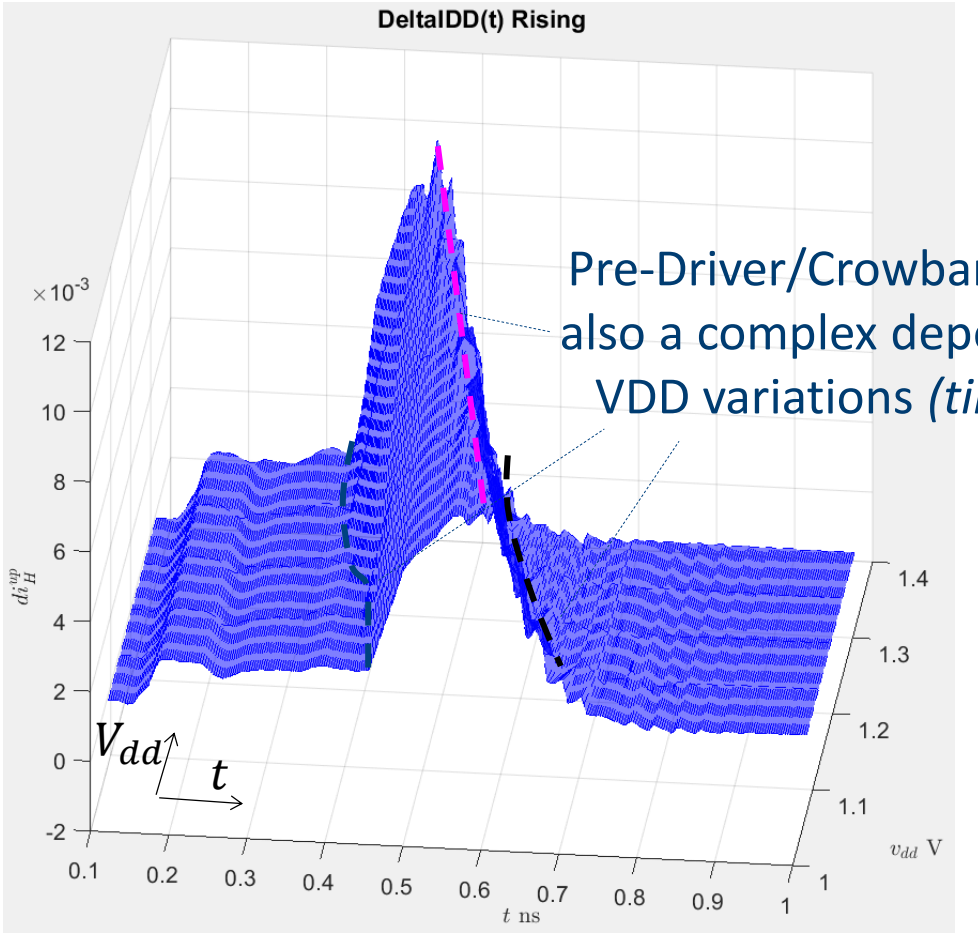
Switching Profiles (w_H, w_L) can have a very complex dependency with VDD variations

IBIS v5.0 model structure may be limited in representing this behavior

VDD ⇔ Supply-Current [I_{COMP}]

$$V_{dd} \in [80\%, \ldots, 100\%, \ldots, 120\%] \times V_{DD,NOM}$$

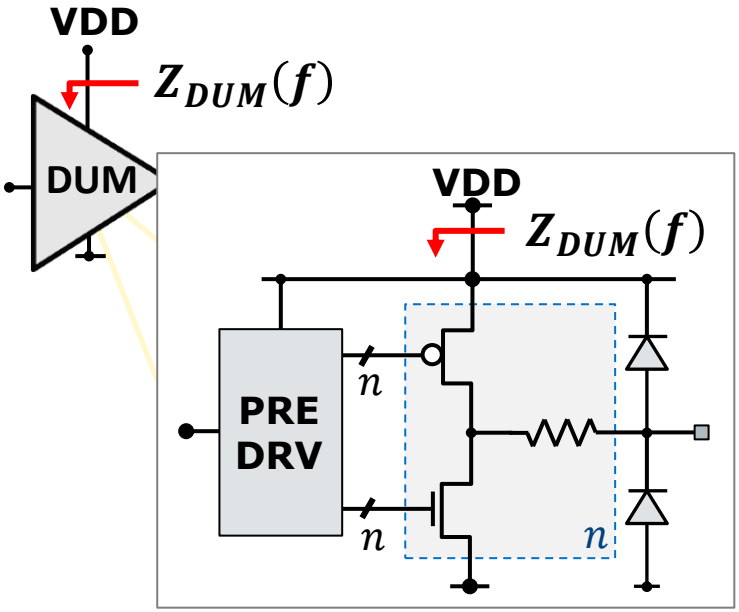




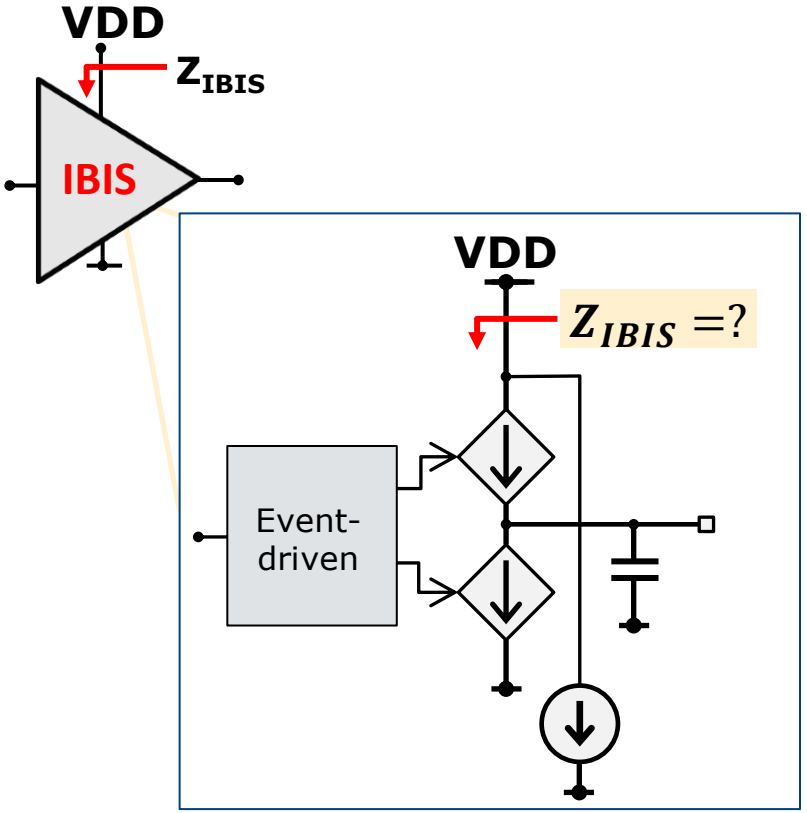
Pre-Driver/Crowbar Current has also a complex dependency with VDD variations *(timing, peak)*

IBIS v5.0 model structure may also be limited in representing this behavior

Dynamic Contribution to Supply-Current



$\neq$



How to correctly model
I/O-Buffer "supply-port impedance"?

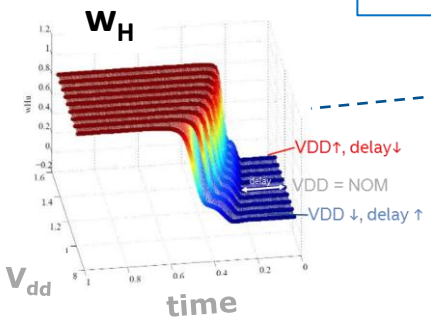
Enhanced I/O-Buffer Macromodels

Mpilog-class

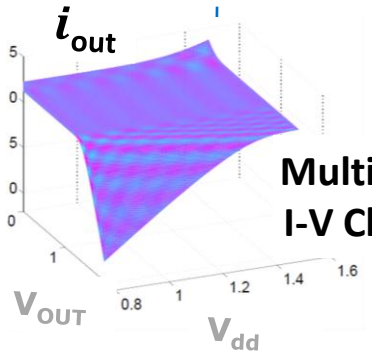
Enhanced Two-Piece Models: R&D work

$$i(t) = w_H(t, v_{dd}) \cdot [I_{PU}(v, v_{dd}) + f_H(v, v_{dd})] + w_L(t, v_{dd}) \cdot [I_{PD}(v, v_{dd}) + f_L(v, v_{dd})]$$

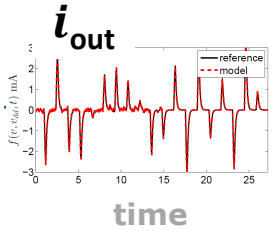
$$i_{dd}(t) = w_H(t, v_{dd}) \cdot [I_{PU,S}(v, v_{dd}) + f_{H,S}(v, v_{dd})] + w_L(t, v_{dd}) \cdot [I_{PD,S}(v, v_{dd}) + f_{L,S}(v, v_{dd})] + \partial i(t, v_{dd})$$



Multi-variate (3D) Switching Characteristics



Multi-variate (3D) I-V Characteristics

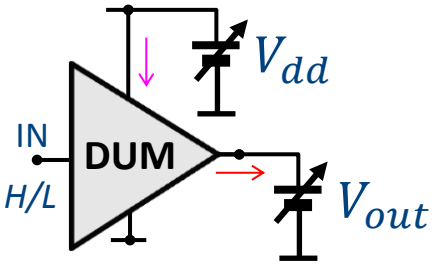


Multiple-Input Single-Output (MISO) Rational Functions (Time-Domain Vector-Fitting)

Explicit dependency with VDD in model sub-components

Mathematical structure ⇒ **re-cast** as **Verilog-A** or **SPICE** circuit

Proposed Enhancements: Static Characteristics

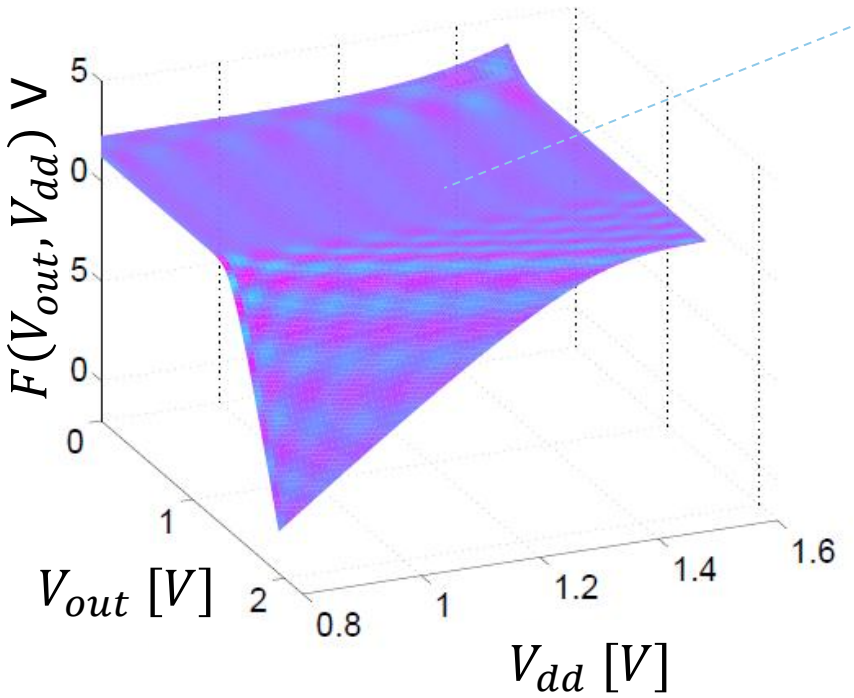


Static characterization Testbench

The static characteristics are now extracted with **nested .DC sweeps** at **output <u>and</u> supply** ports.

(e.g.,1 output, 1 supply, 1 current: 3D-surface)

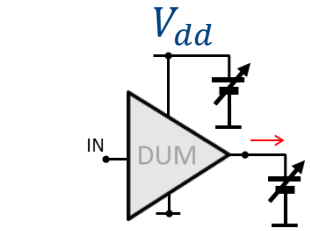
$$I_S = F(V_{out}, V_{dd})$$



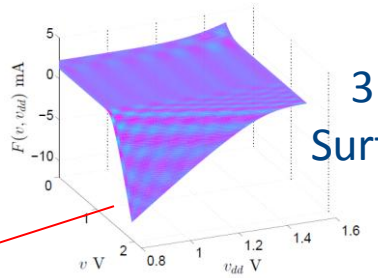
Such 3D surfaces are calculated for:

$$I_{SH}(V_{out}, V_{dd})$$
$$I_{SL}(V_{out}, V_{dd})$$
$$I_{dd,SH}(V_{out}, V_{dd})$$
$$I_{dd,SL}(V_{out}, V_{dd})$$

SVD Approximation of 3D Surfaces



Static Characterization Testbench



3D Surface

$\boldsymbol{Y}$, samples @ V_{out}, V_{dd} from SPICE and .dc sweeps

V_{out}

V_{dd}

y

$\cong \boldsymbol{U_1 \Sigma U_2^T} =$

$\boldsymbol{U_1}$ σ_k $\boldsymbol{U_2^T}$

Singular Value Decomposition **(SVD)**

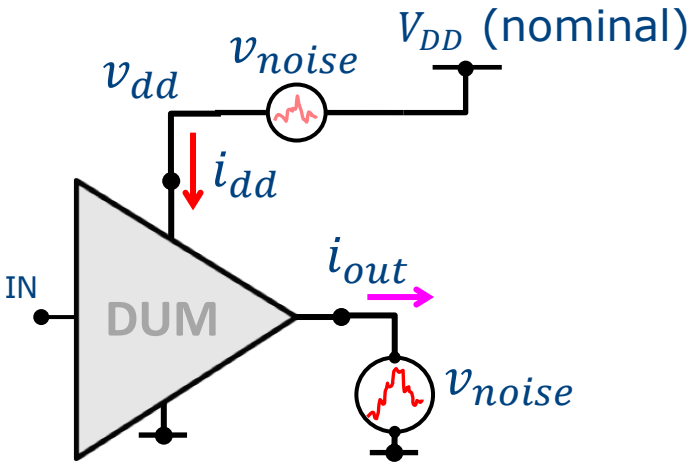
Truncation Process: Maximum compactness meeting target accuracy

$$y \cong F(V_{out}, V_{dd}) = \sum_{k=1}^{N} \sigma_k \varphi_{1,k}(V_{out}) \varphi_{2,k}(V_{dd})$$

SVD-approximation $\Rightarrow$

- SPICE Netlist *(VCVS, CCCS, …)*
- Verilog-A Code

Proposed Enhancements: Dynamic Characteristics

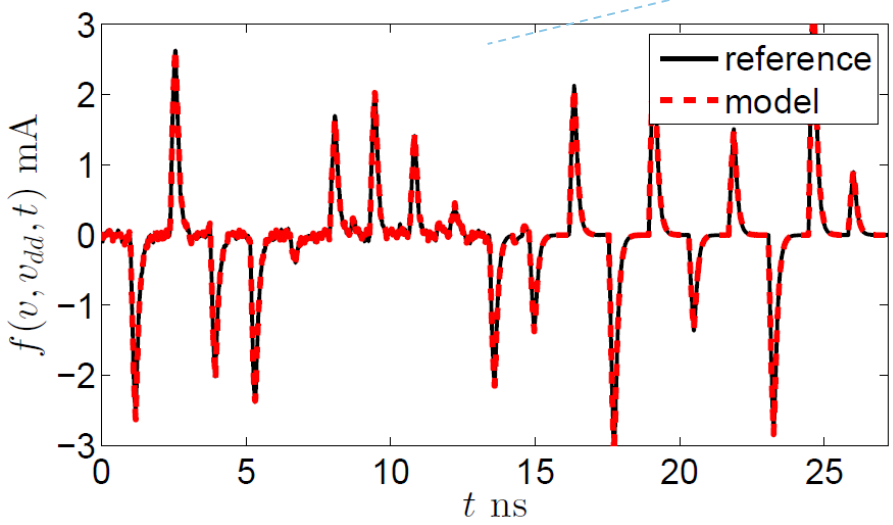


Dedicated $v_{out}(t)$ and $v_{dd}(t)$ stimuli are applied, simultaneously.

Dynamic characteristics = **rational approximations** using **Time-Domain Vector-Fitting** (**TD-VF**) algorithms.

$$i_{out,H} = f(v_{out}, v_{dd})$$

(e.g., pull-up dynamic MISO TDVF model)



Similar models are computed for:

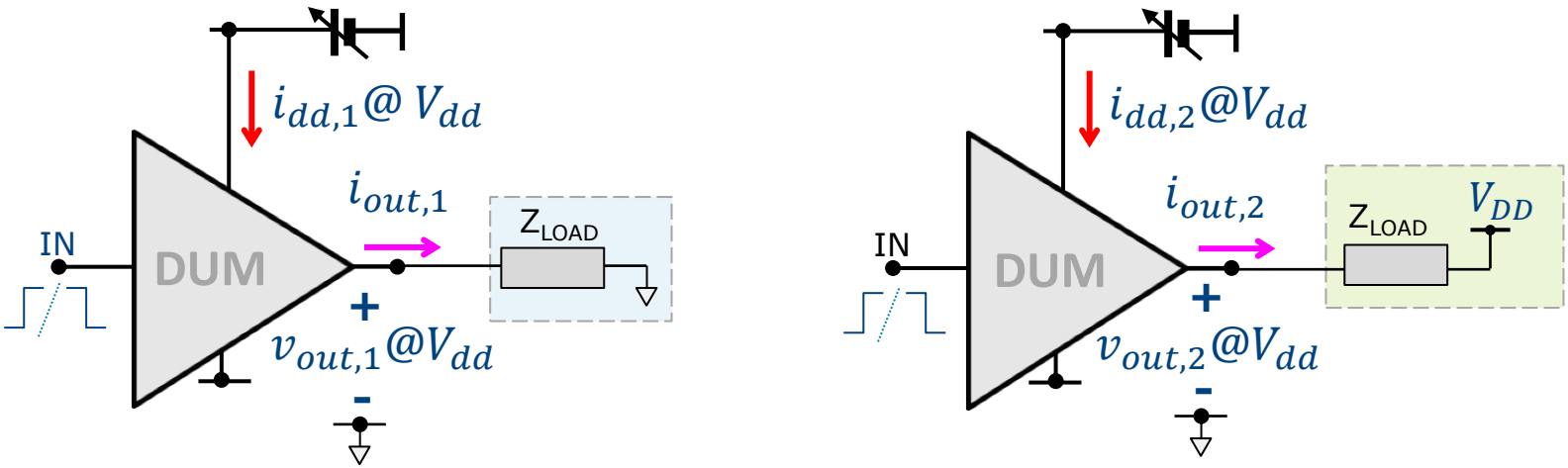
$$i_{out,H}(v_{out}, v_{dd})$$
$$i_{out,L}(v_{out}, v_{dd})$$
$$i_{dd,H}(v_{out}, v_{dd})$$
$$i_{dd,L}(v_{out}, v_{dd})$$

and implemented as:

- SPICE Netlist
- Verilog-A models

Proposed Enhancements: Weighting Functions

$$V_{dd} \in [80\%, \ldots, 100\%, \ldots, 120\%] \times V_{DD,NOM}$$

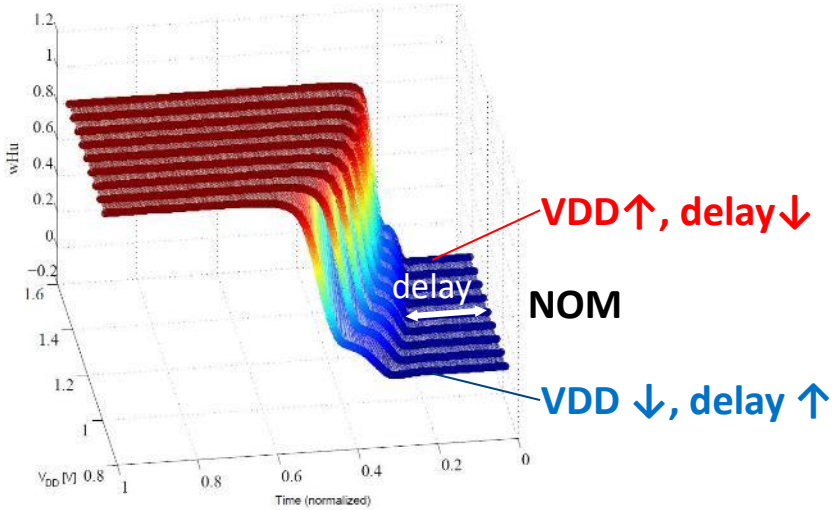


Weighting functions w_H and w_L are calculated for several V_{dd} values.

This allows the creation of 3D-surfaces

$\boldsymbol{w_H(t, v_{dd})}$ and $\boldsymbol{w_L(t, v_{dd})}$

reproducing the complex dependency of the switching events with VDD.



Comparative Summary

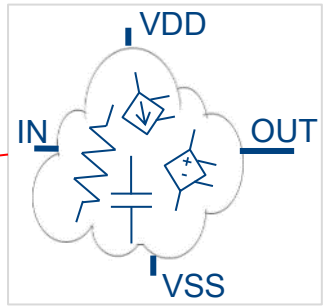
	IBIS v5.0	Enhanced Models
OUTPUT STATIC	2D I-V Tables	3D Surfaces $F_x(V_{out}, V_{dd})$
OUTPUT DYNAMIC	Capacitive C_{COMP}	State-space models $f_x(v_{out}, v_{dd})$
WEIGHTING FUNCTIONS	2EQ/2UK @VDD_{NOM} $k_U(t)$ and $k_D(t)$	3D Surfaces $w_{L2H}(t, v_{dd})$ and $w_{H2L}(t, v_{dd})$
SUPPLY CURRENT	$I_{COMP} - t$ Table	3D Surface $\delta_i(t, v_{dd})$
SUPPLY EFFECTS	Static Modulation $K_{SSO\_PU(PD)}$	3D surfaces & MISO models Static/Dyn/Timing Effects

MPILOG Model Implementation

Mpilog models can be synthesized as:

- **SPICE Netlists**
- **Verilog-A** Modules
- IBIS (v5.1/6.0) 😐
- **IBIS** using **[External Model]**

mpilog.cir



mpilog.va

```
// Output + supply ports driver macromodel
// VERILOG-A implementation autogenerated by Mpilog

`include "constants.vams"
`include "disciplines.vams"
//*************************************************
// COMPLETE MACROMODEL
//*************************************************
module mpilog_model (v_in,v_io,vdd_io,ref_io,v_oe);

// ELECTRICAL VARIABLES
electrical v_in,v_io,vdd_io,ref_io,v_oe;
electrical w1,w2,f1,f2,fs1,fs2,f7,fs7;
electrical f3,f4,fs3,fs4,di,f8,fs8;
electrical u1,u2;

// PARAMETERS
parameter real PVDDcore=1; // logic core nominal voltage
parameter real PVDD=1.2; //output power-supply nominal voltage


analog begin
// MODEL STRUCTURE...
```

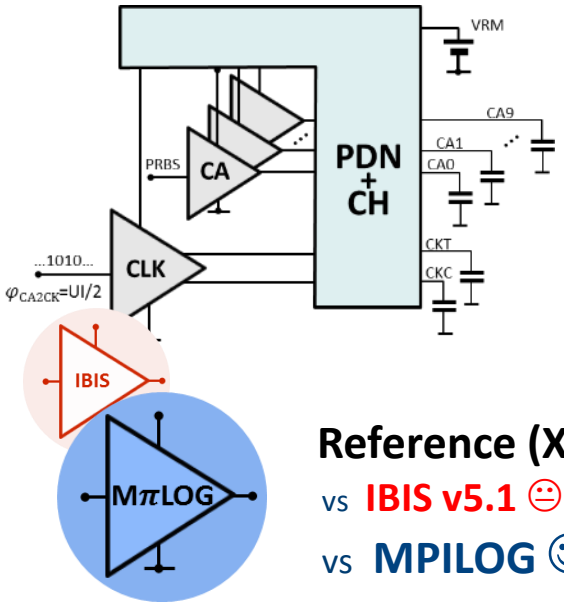
```
[External Model]
Language Verilog-A(MS)

| Corner corner_name file_name     circuit_name (module)
Corner       Typ       mpilog.va     mpilog_model
Corner       Min          NA             NA
Corner       Max          NA             NA

| Ports List of port names (in same order as in Verilog-A(MS))
|     v_in     v_out        vdd_io  ref_io  v_oe
Ports my_drive A_signal_pos A_puref A_pdref my_enable
|
| D_to_A d_port   port1     port2     vlow vhigh  trise tfall corner_name
D_to_A   D_drive  my_drive  A_pdref   0.0  1.1    0.1n  0.1n   Typ
D_to_A   D_enable my_enable A_pdref   0.0  1.1    0.1n  0.1n   Typ
|
[End External Model]
```

mpilog.ibs

Validations

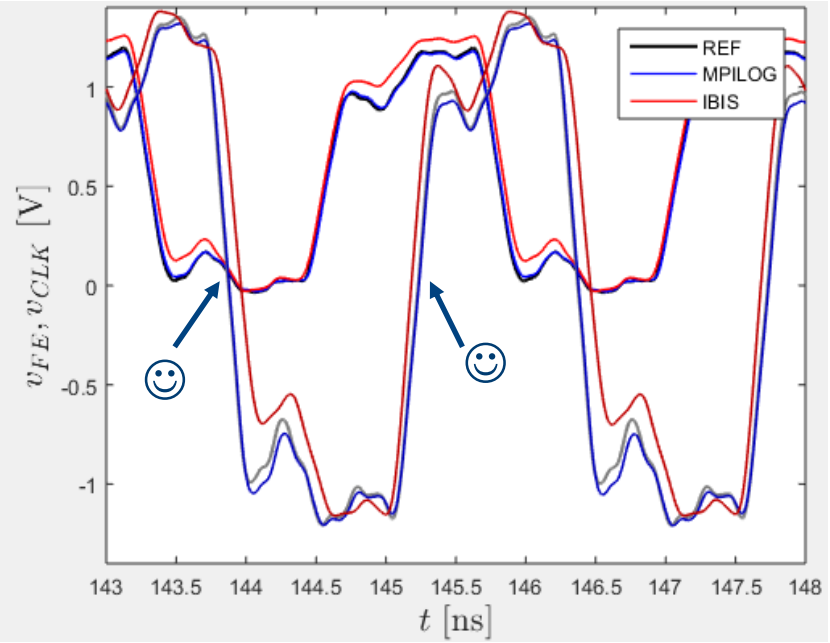


Reference (XTOR-level)

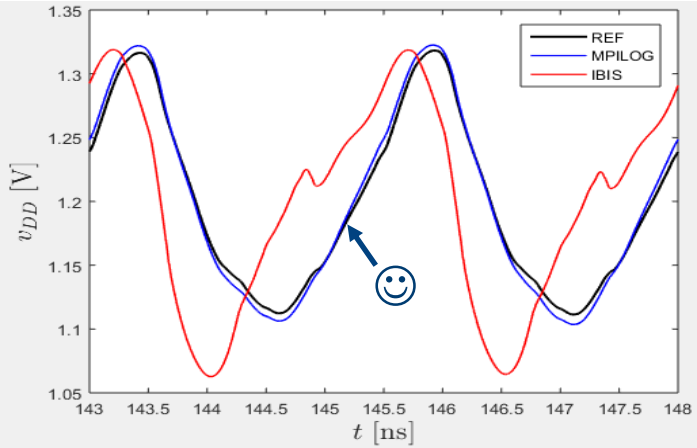
vs **IBIS v5.1** 😐

vs **MPILOG** ☺

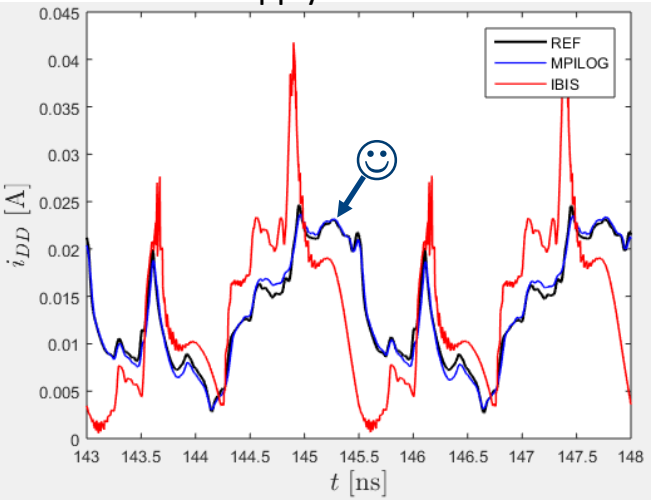
CLK/DATA Far-End Signals



Supply-Noise

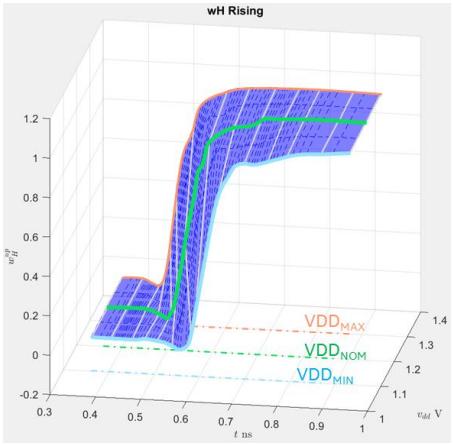


Supply-Current



Possible Enhancements to IBIS models?

3-curve approx. of 3D-Surfaces in IBIS



How to include 3-curve approx. data in an IBIS file?

```
[Model] DDR_PAD
| variable                typ    min    max
[Temperature Range]       25     -30    125
[Voltage Range]           1.2    1.1    1.3
[Rising Waveform]
| Time                    v(typ) v(min) v(max)
  0
  25ps
  …
  1.21ns
  1.22ns
```

IBIS v5.1:

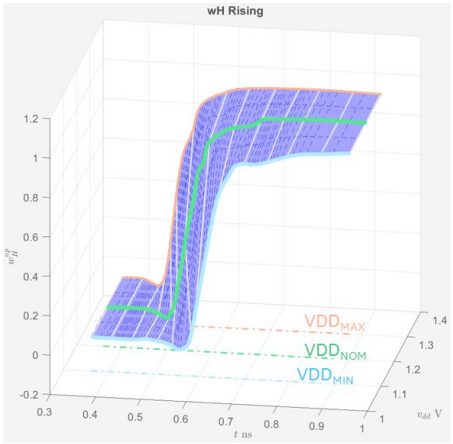
Process: TT	Process: SS	Process: FF
VDD: TYP	VDD: MIN	VDD: MAX
Temp: Typ	Temp: Max	Temp: Min

For all IBIS table …

- *PU/PD*
- *Rising/Falling V-t*
- *Rising/Falling I-t*

1 [Model],
3 PVT Corners

3-curve approx. of 3D-Surfaces in IBIS



How to include 3-curve approx. data in an IBIS file?

[Model] DDR_PAD

variable	*typ*	*min*	*max*
[Temperature Range]	25	-30	125
[Voltage Range]	1.2	1.1	1.3

[Rising Waveform]

Time	*v(typ)*	*v(min)*	*v(max)*
0			
25ps			
…			
1.21ns			
1.22ns			

For all IBIS table …
- *PU/PD*
- *Rising/Falling V-t*
- *Rising/Falling I-t*

~~**IBIS v5.1:**~~

~~Process: TT~~ ~~Process: SS~~ ~~Process: FF~~
~~VDD: TYP~~ ~~VDD: MIN~~ ~~VDD: MAX~~
~~Temp: Typ~~ ~~Temp: Max~~ ~~Temp: Min~~

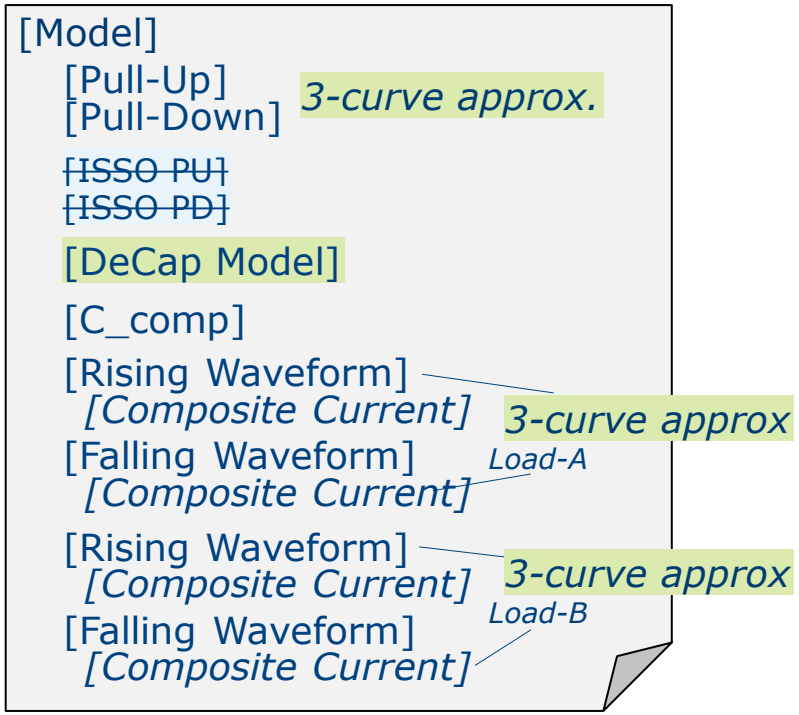
~~**1 [Model],**~~
~~**3 PVT Corners**~~

“enhanced” IBIS

Process: TT Process: TT Process: TT
VDD: TYP VDD: MIN VDD: MAX
Temp: 25 Temp: 25 Temp: 25

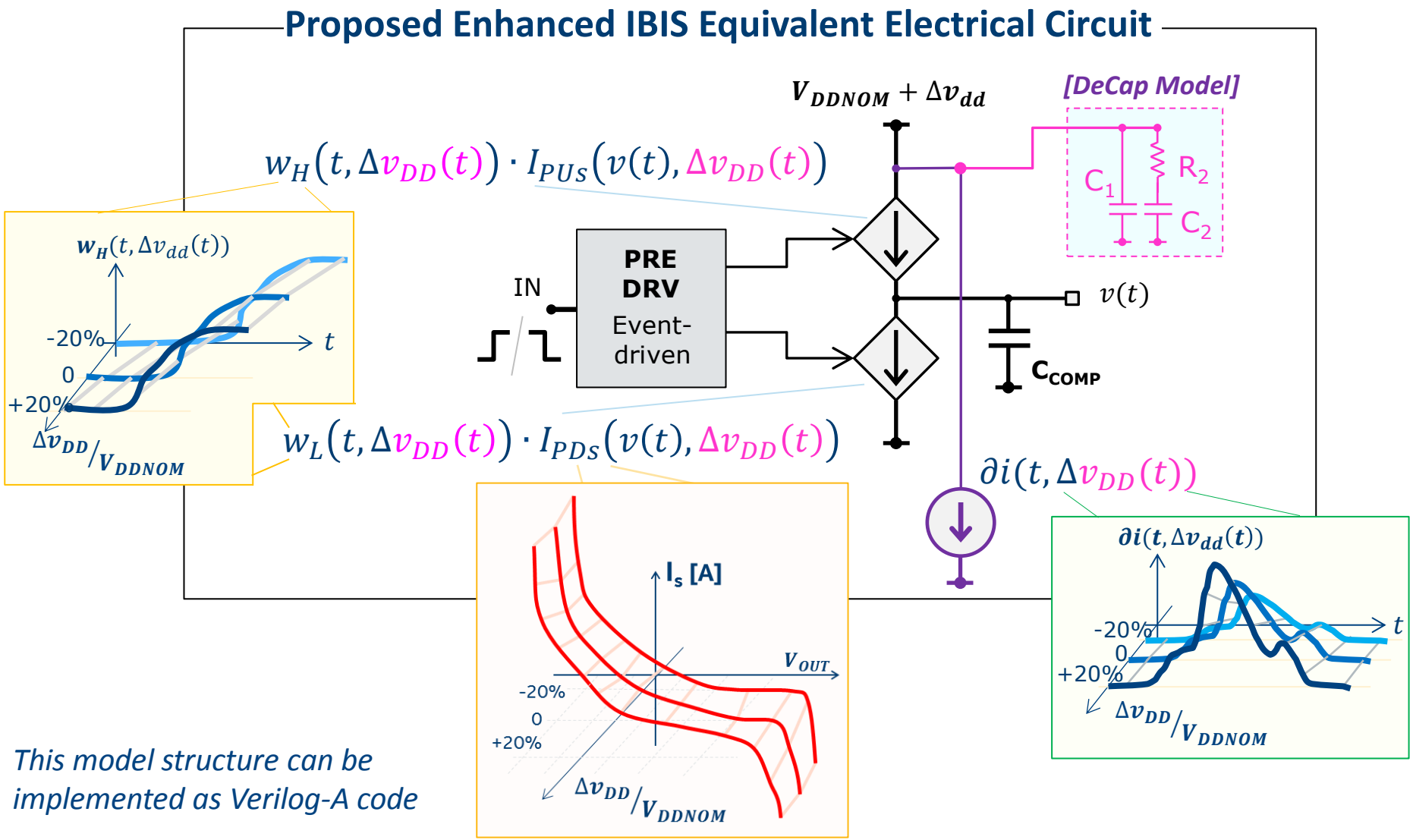
1 [Model],
1 PT Corner (e.g., TT/25C)
Accuracy @SI&PI
(capture VDD-effects)

(Proposed) “Enhancements” to IBIS Models



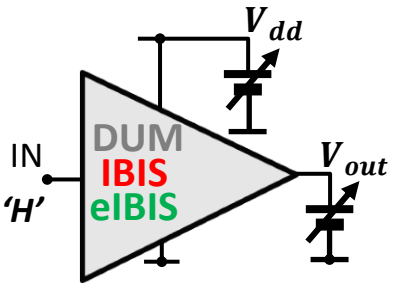
- Removal of [ISSO PU] and [ISSO PD]
- **3-curve approximations**
  - ✓ 3D PU/PD Characteristic
  - ✓ 3D Rising/Falling V-t Tables
  - ✓ 3D Rising/Falling [Composite Current]
- **[DeCap Model]**
  - ✓ C1 || (R2+C2) for “supply impedance”

(Proposed) "Enhanced" IBIS Models



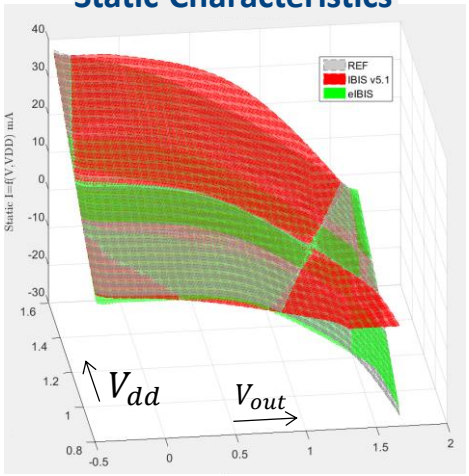
This model structure can be implemented as Verilog-A code

Multi-variate Surfaces

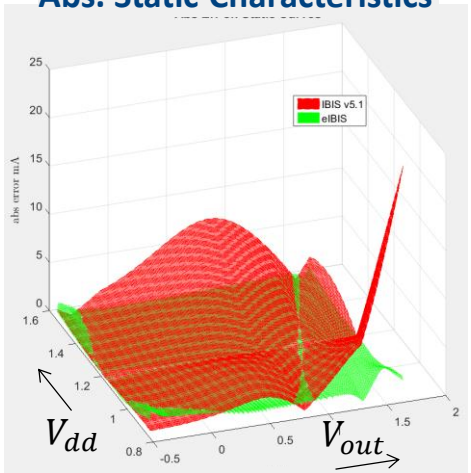


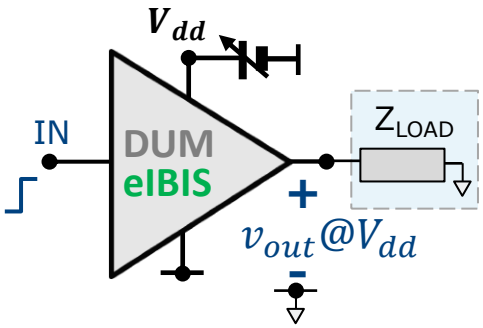
Nested .DC sweep
on Output and Supply ports

Static Characteristics



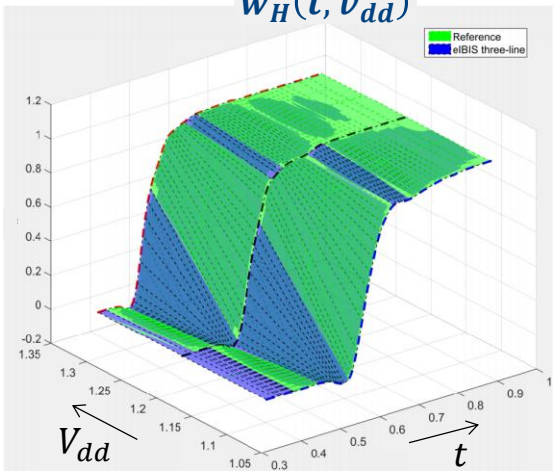
Abs. Static Characteristics



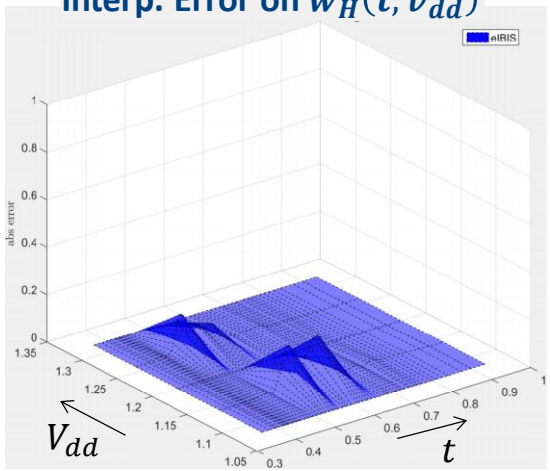


.TRAN Rising Waveforms applying
different VDD values

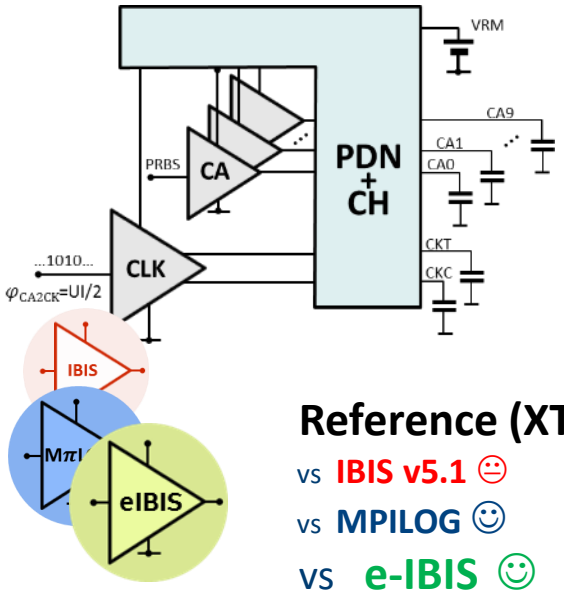
$w_H(t, v_{dd})$



Interp. Error on $w_H(t, v_{dd})$



Validation



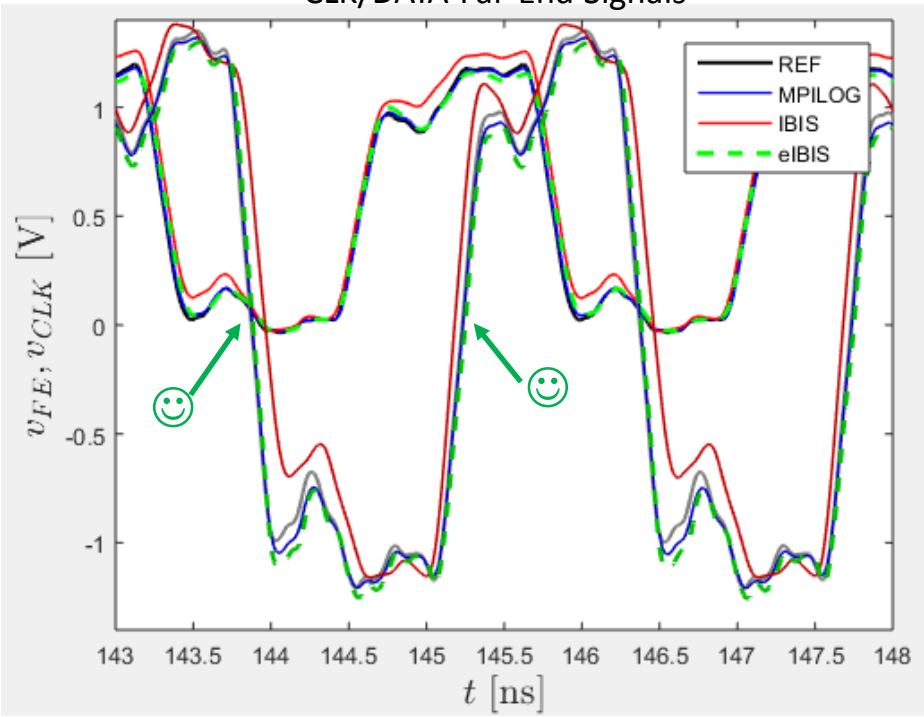
Reference (XTOR-level)

vs **IBIS v5.1** 😐

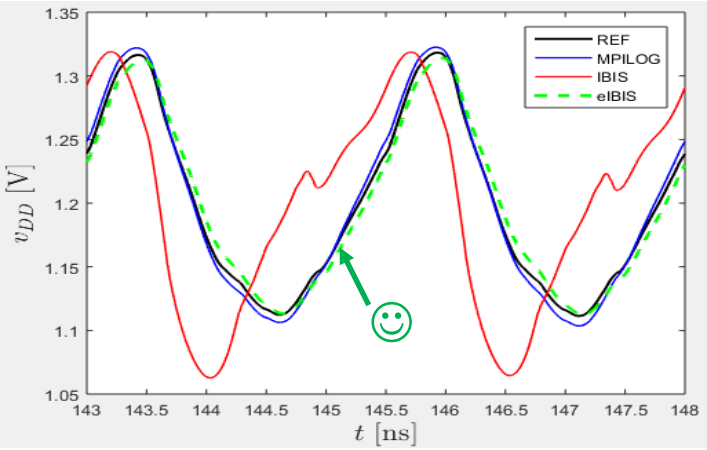
vs **MPILOG** ☺

vs **e-IBIS** ☺

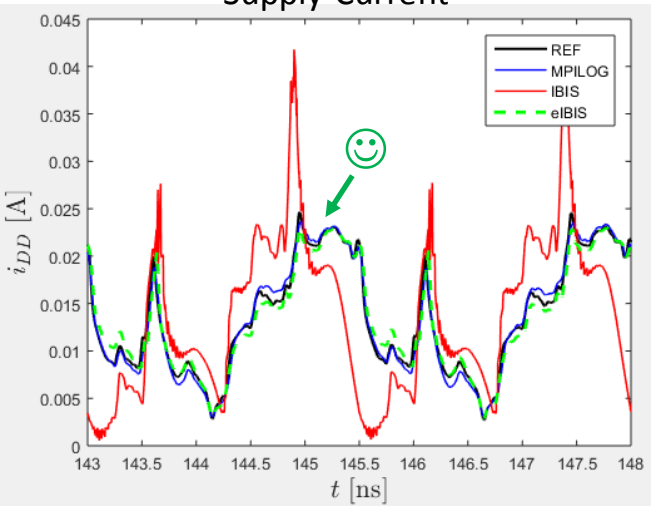
CLK/DATA Far-End Signals



Supply-Noise



Supply-Current



Conclusions

Enhanced two-piece model structure to accurately reproduce currents and voltages at **output** and **supply ports** :

- ✓ **SVD + truncation-process** for (multi-dimensional) Static Char.
- ✓ Multiple-Input **TDVF** for Dynamic Characteristics
- ✓ 3D switching characteristics $\boldsymbol{w(t, v_{dd})}$

Flexible and **modular** approach using **Mpilog**
Implementations possible in **SPICE/Verilog-A**

Identification of **potential limitations** of IBIS models power-awareness
Set of **possible enhancements** to IBIS
(*3-curve approx. & VDD-effects, impedance at supply-port, …*)

Validation tests highlight **excellent accuracy** in **SI/PI co-simulations**

Thank you for the attention!