European IBIS Summit Meeting

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Models for IC Buffers: A Top-down Approach

Taking the nonlinear Thévenin-like topology beyond the proof of concept

C. Diouf[1], M. Telescu[2], N.Tanguy[2], I.S. Stievano[3], F.G. Canavero[3]

[1]Ecole Nationale d'Ingénieurs de Brest, CNRS, UMR 6285, Lab-STICC

[2]Université de Brest; CNRS, UMR 6285, Lab-STICC

[3]Politecnico di Torino, Department of Electronics and Telecommunications, EMC Group

Outline

- Context
- Building a nonlinear Thévenin-like model for IC buffers
- Demonstrating the approach on a TI driver
- Discussing the implementation
- Extending the model to account for v_{dd} variations
- Conclusion

Context

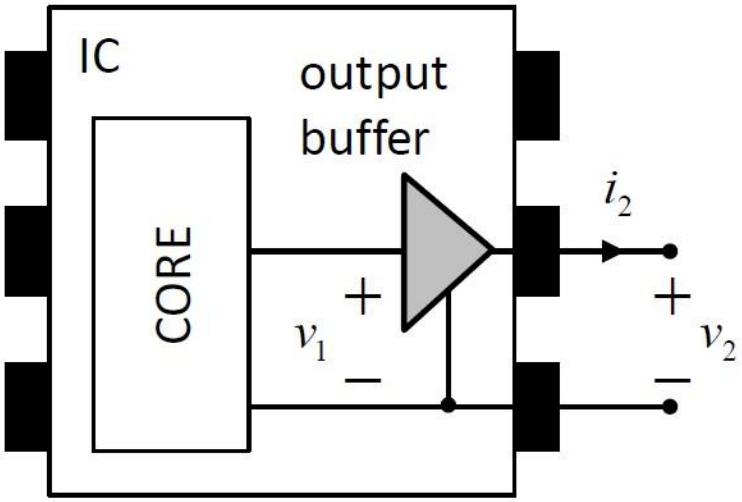
Joint research on buffer modeling

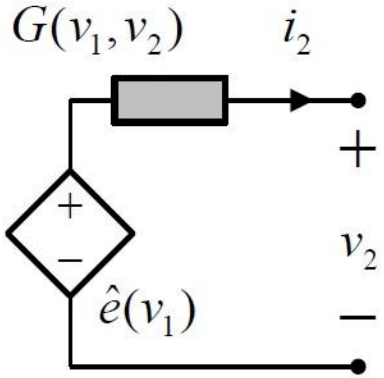
Politecnico di Torino, Italy and Université de Brest, France

Focus:

- New methodologies and approaches to IC buffer macromodeling
- Better accuracy in critical conditions, more general approach to modeling
- Particular focus on overclocking: issue present in literature, conferences and IBIS summit meetings

Nonlinear Thévenin-like model



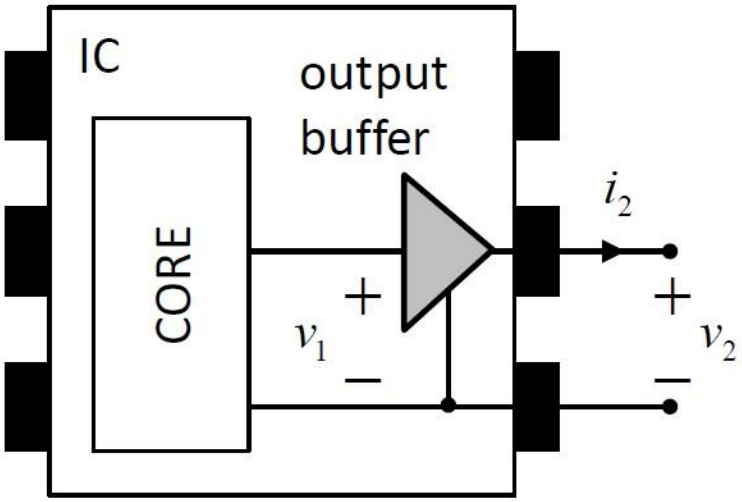


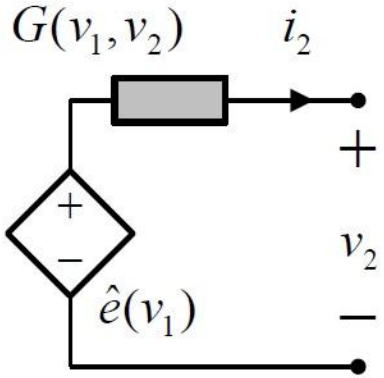
- General idea presented at the IBIS Summit Meeting in 2013

NEW!

- Implementation details for every block
- Extraction: full walkthrough
- Accounting for V_{DD} variation

Nonlinear Thévenin-like model



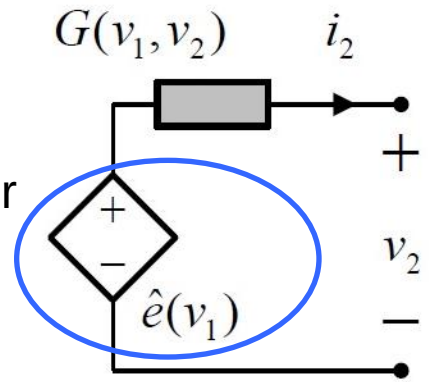


Example: Texas Instruments driver
SN74ALVCH16973, VDD = 2,5V

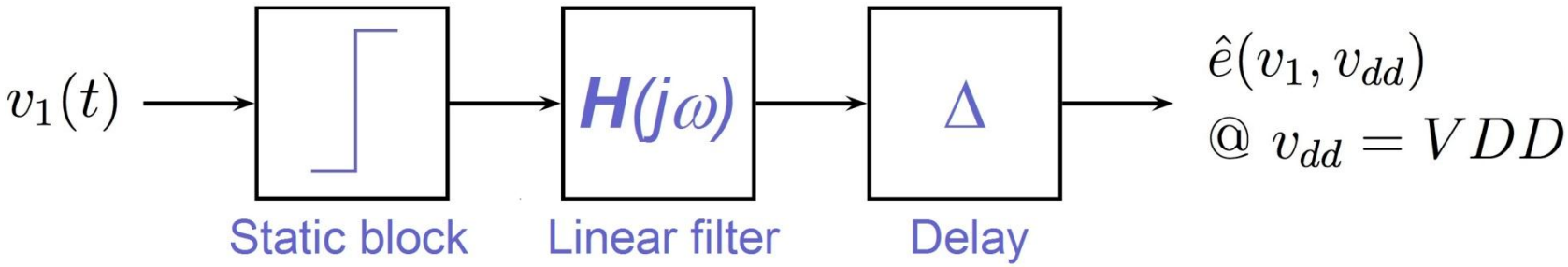
Nonlinear Thévenin-like model

OPEN CIRCUIT VOLTAGE

- Single-input-single-output nonlinear element
- Gives the input-output characteristic of the driver
- Can be modeled in different ways



Nonlinear Thévenin-like model



OPEN CIRCUIT VOLTAGE

- Hammerstein structure (well known in control-theory)
- Static bloc: Step like function, table-based implementation
- Linear filter identified via vector fitting
- Delay modeled by ideal transmission line

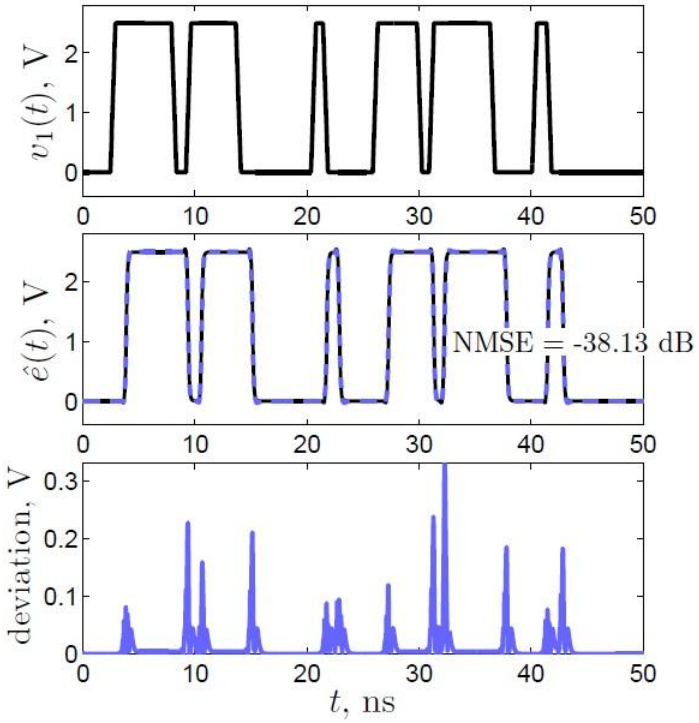
Nonlinear Thévenin-like model

OPEN CIRCUIT VOLTAGE

- Very accurate model using very simple and robust structure
- Dynamic elements could be added if needed

$$NMSE = 10\log_{10}\frac{\sum_{k=0}^{K-1}\left(y_{ref}(k)-y_{approx}(k)\right)^2}{\sum_{k=0}^{K-1}\left(y_{ref}(k)\right)^2}$$

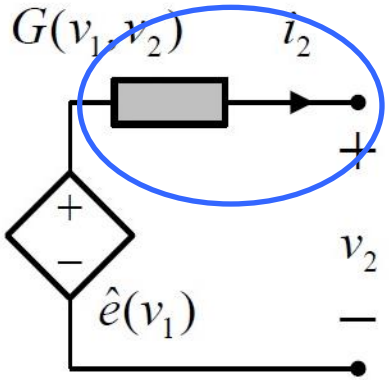
NMSE gives a measure of the accuracy over a finite number of samples K.



Nonlinear Thévenin-like model

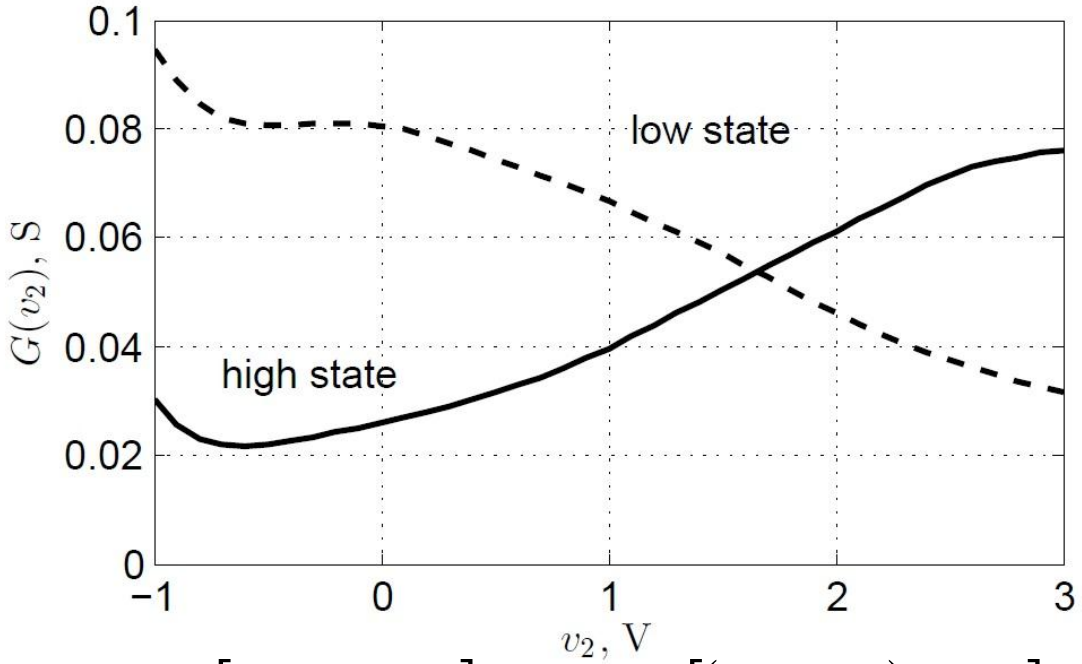
NONLINEAR CONDUCTANCE

- On state / off state separation
- Static table based model at this stage



$$G(v_1, v_2) = \left[\hat{e}(v_1)/V_{DD}\right] G_H(v_2) + \left[\left(1-\hat{e}(v_1)\right)/V_{DD}\right] G_L(v_2)$$
$$= \tilde{w}_H G_H(v_2) + \tilde{w}_L G_L(v_2)$$

Nonlinear Thévenin-like model

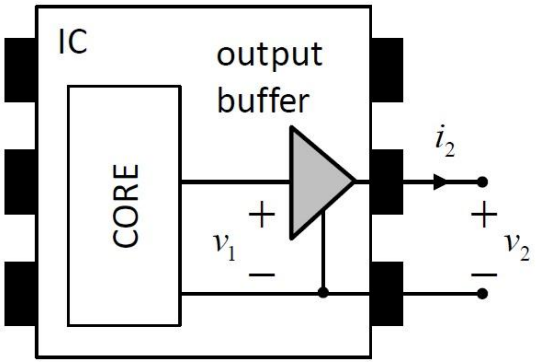


$$G(v_1, v_2) = \left[\hat{e}(v_1)/V_{DD}\right] G_H(v_2) + \left[\left(1-\hat{e}(v_1)\right)/V_{DD}\right] G_L(v_2)$$
$$= \tilde{w}_H G_H(v_2) + \tilde{w}_L G_L(v_2)$$

Relation with IBIS

Thévenin-like

$$i_2(t) = G(v_1, v_2)\left[\hat{e}(v_1) - v_2\right]$$
$$= \left[\left(\hat{e}(v_1)/V_{DD}\right)G_H(v_2) + \left(\left(1-\hat{e}(v_1)\right)/V_{DD}\right)G_L(v_2)\right]\left[\hat{e}(v_1) - v_2\right]$$
$$= \left[\tilde{w}_H G_H(v_2) + \tilde{w}_L G_L(v_2)\right]\left[\hat{e}(v_1) - v_2\right]$$
$$= \tilde{w}_H\left[\hat{e}(v_1) - v_2\right]G_H(v_2) + \tilde{w}_L\left[\hat{e}(v_1) - v_2\right]G_L(v_2)$$
$$= \tilde{w}_H\,\tilde{f}_H(v_1, v_2) + \tilde{w}_L\,\tilde{f}_L(v_1, v_2)$$



IBIS-like

$$i_2(t) = w_H\, f_H(V_{DD} - v_2) + w_L\, f_L(v_2)$$

- Static characteristics of the output port in high and low state
- Weighting functions computed from devices responses on two resistive loads

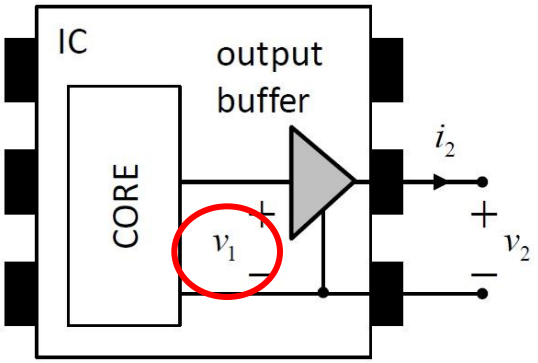
Relation with IBIS

Thévenin-like

$$i_2(t) = G(v_1, v_2)\left[\hat{e}(v_1) - v_2\right]$$
$$= \left[\left(\hat{e}(v_1)/V_{DD}\right)G_H(v_2) + \left(\left(1-\hat{e}(v_1)\right)/V_{DD}\right)G_L(v_2)\right]\left[\hat{e}(v_1) - v_2\right]$$
$$= \left[\tilde{w}_H G_H(v_2) + \tilde{w}_L G_L(v_2)\right]\left[\hat{e}(v_1) - v_2\right]$$
$$= \tilde{w}_H\left[\hat{e}(v_1) - v_2\right]G_H(v_2) + \tilde{w}_L\left[\hat{e}(v_1) - v_2\right]G_L(v_2)$$
$$= \tilde{w}_H\,\tilde{f}_H(v_1, v_2) + \tilde{w}_L\,\tilde{f}_L(v_1, v_2)$$

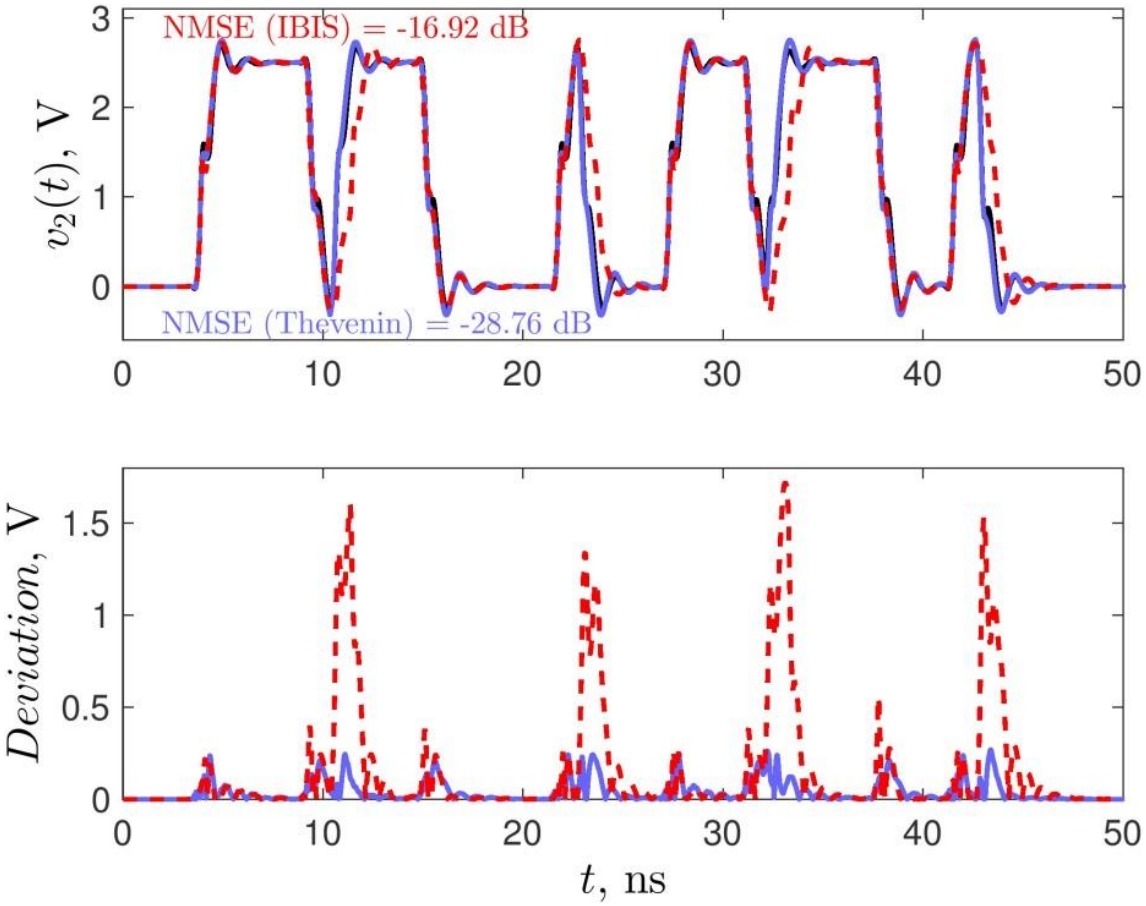
IBIS-like

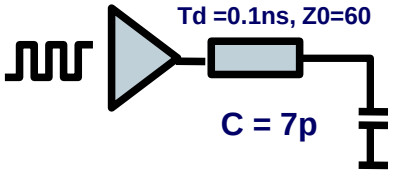
$$i_2(t) = w_H\, f_H(V_{DD} - v_2) + w_L\, f_L(v_2)$$



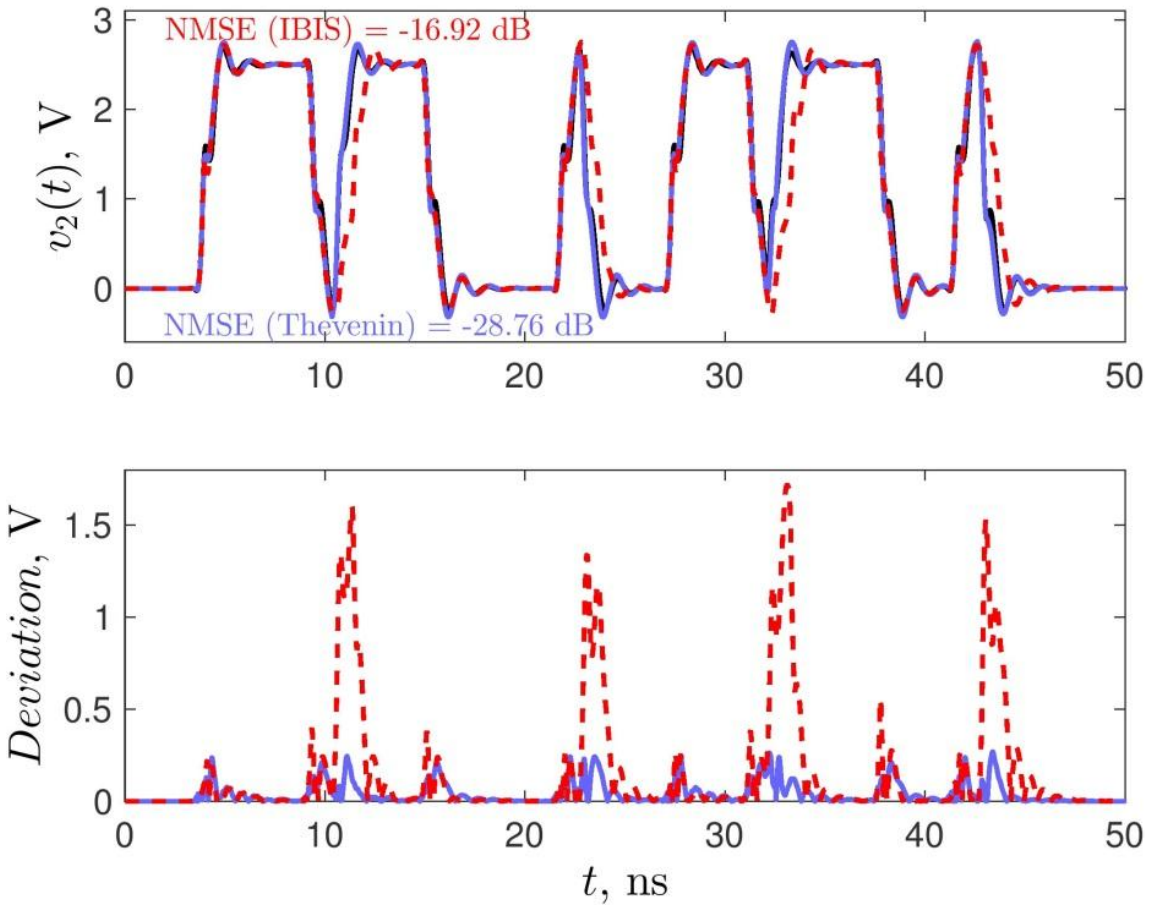
In the Thévenin-like model both $\tilde{w}_{H,L}$ and $\tilde{f}_{H,L}$ depend on v_1
In the IBIS-like model only $w_{H,L}$ depend on v_1

Transient simulation results





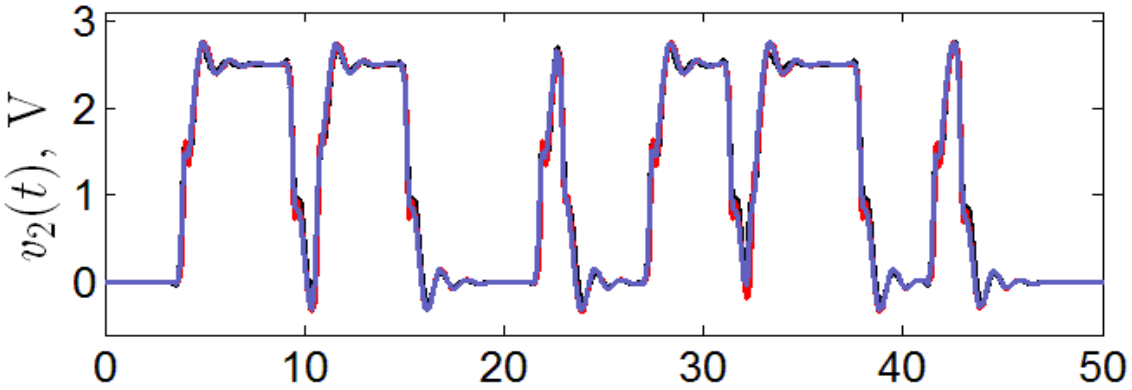
Transient simulation results



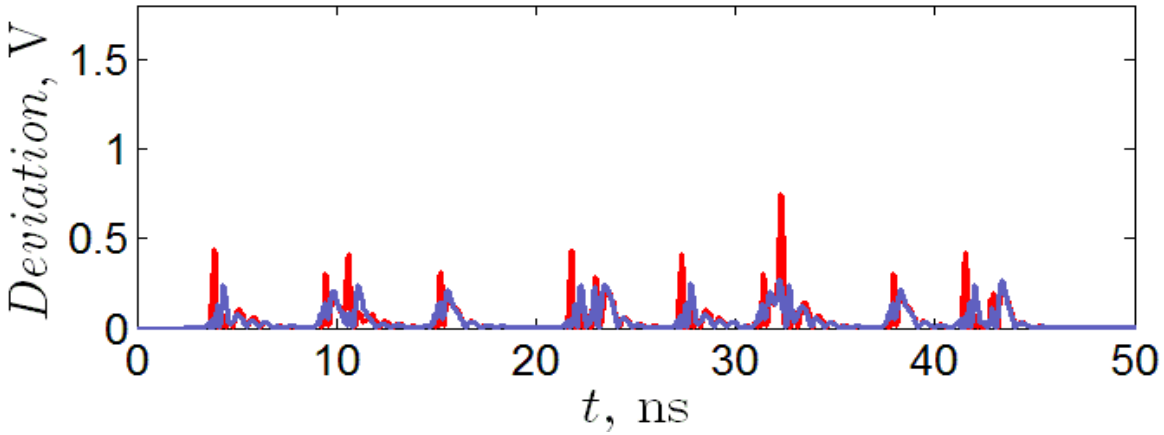
Overclocking:
solve *a* problem or
solve *the* problem ?

Thévenin model works, but why?

Transient simulation results

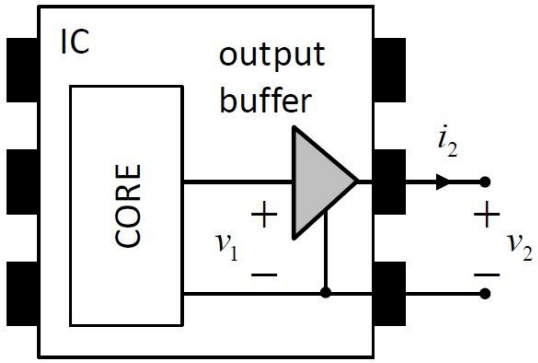


Hybrid model: IBIS weighting functions driven through Hammerstein structure.



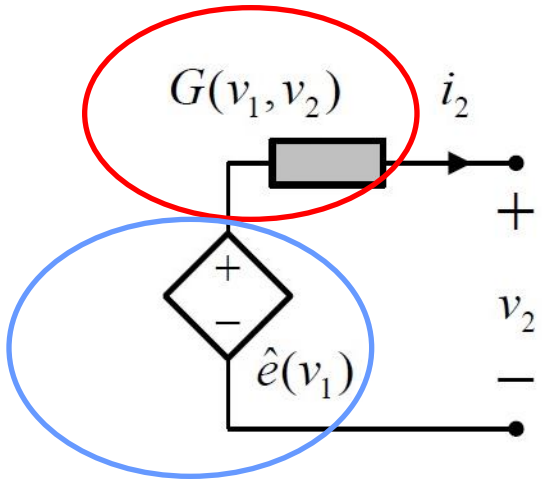
Overclock problem solved but original Thévenin model has better dynamics.

Summing things up…



Tables + Simple filter + delay

Static table-based model here → dynamic models: compensation capacitance, linear FIR, nonlinear model if needed



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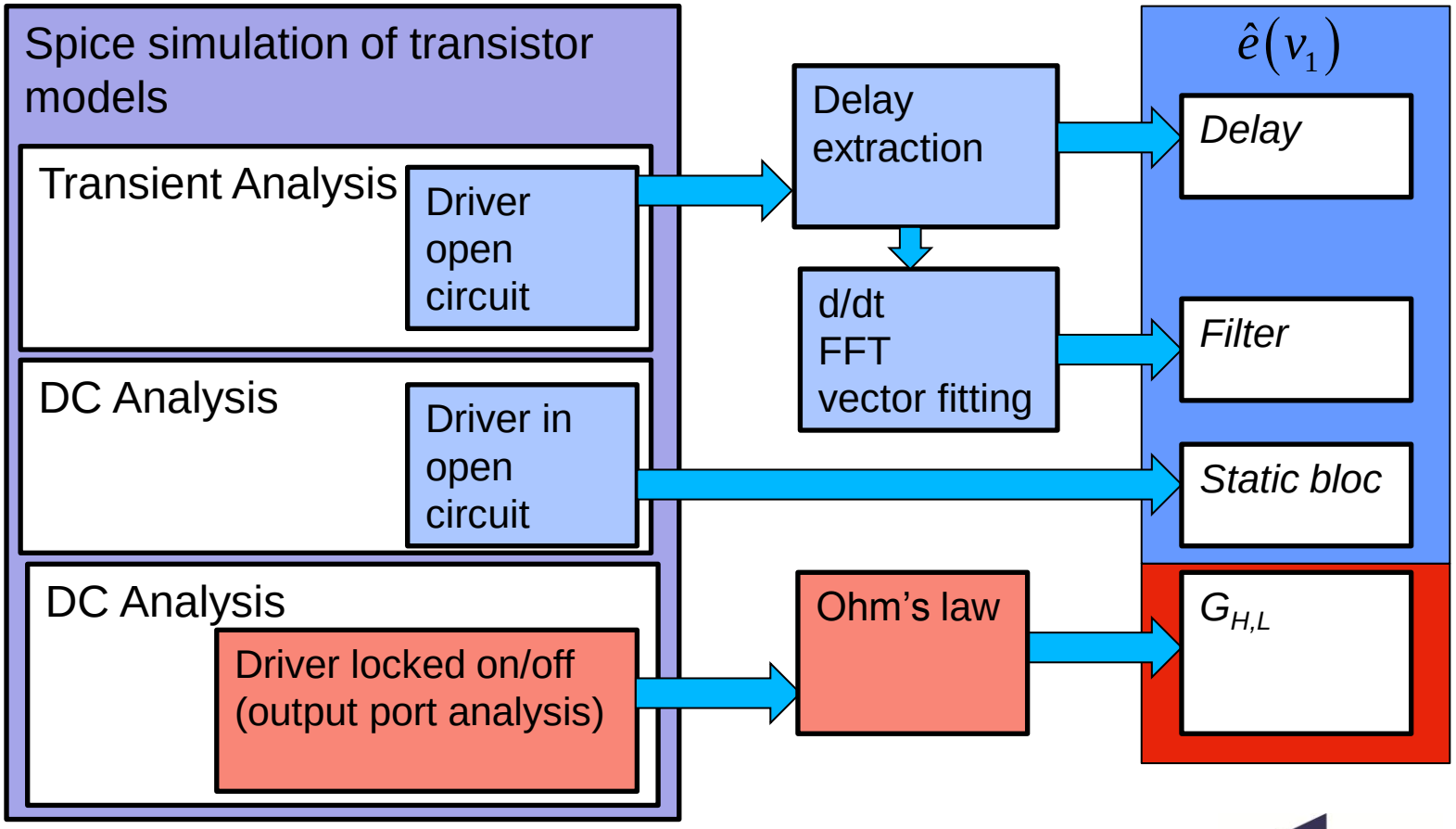
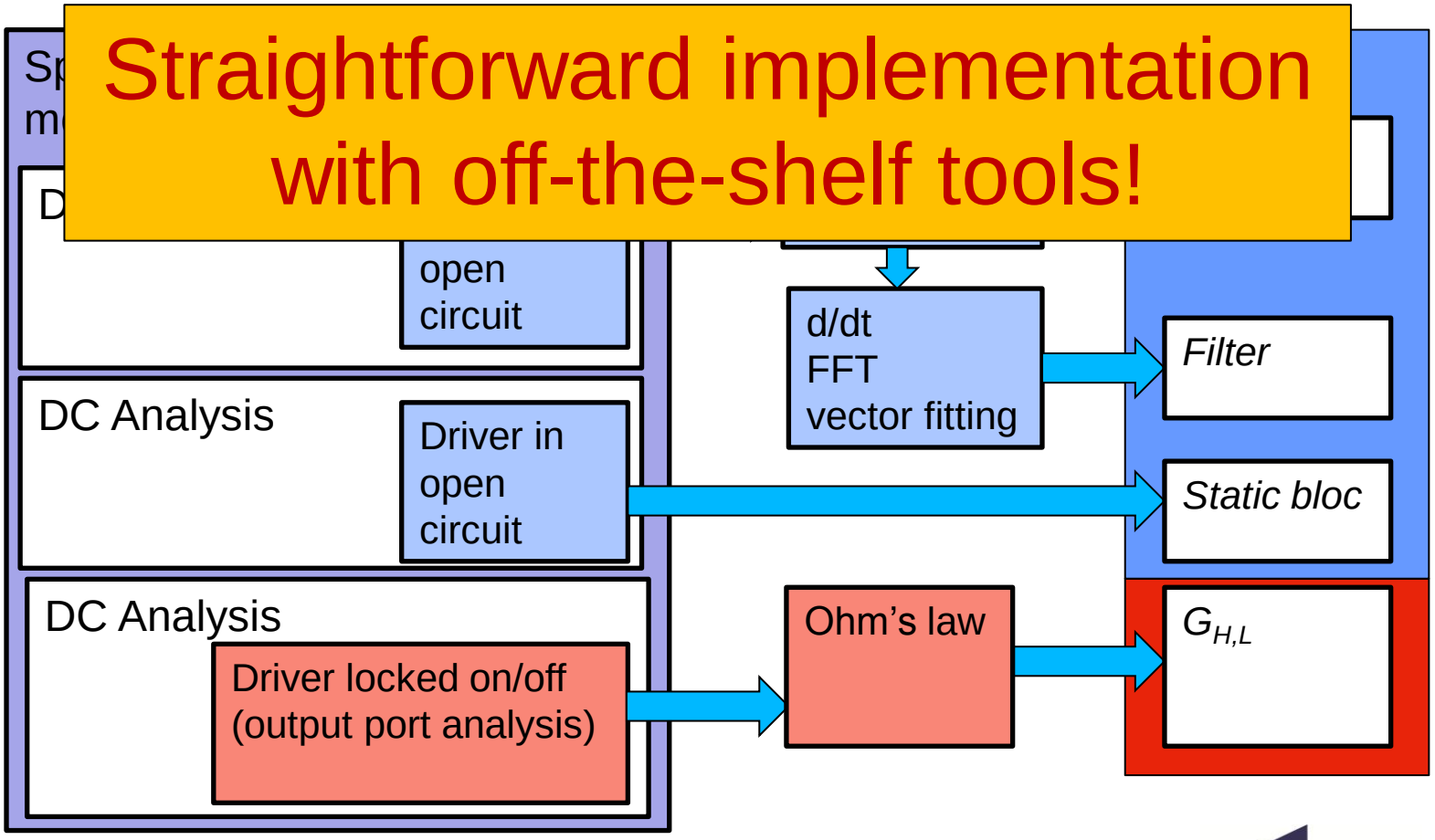
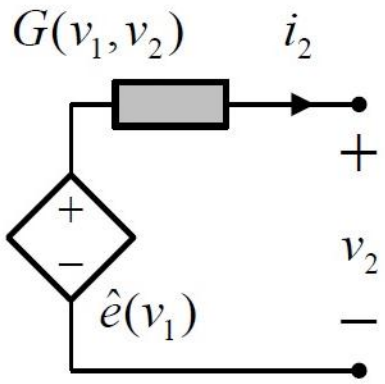


Summing things up…

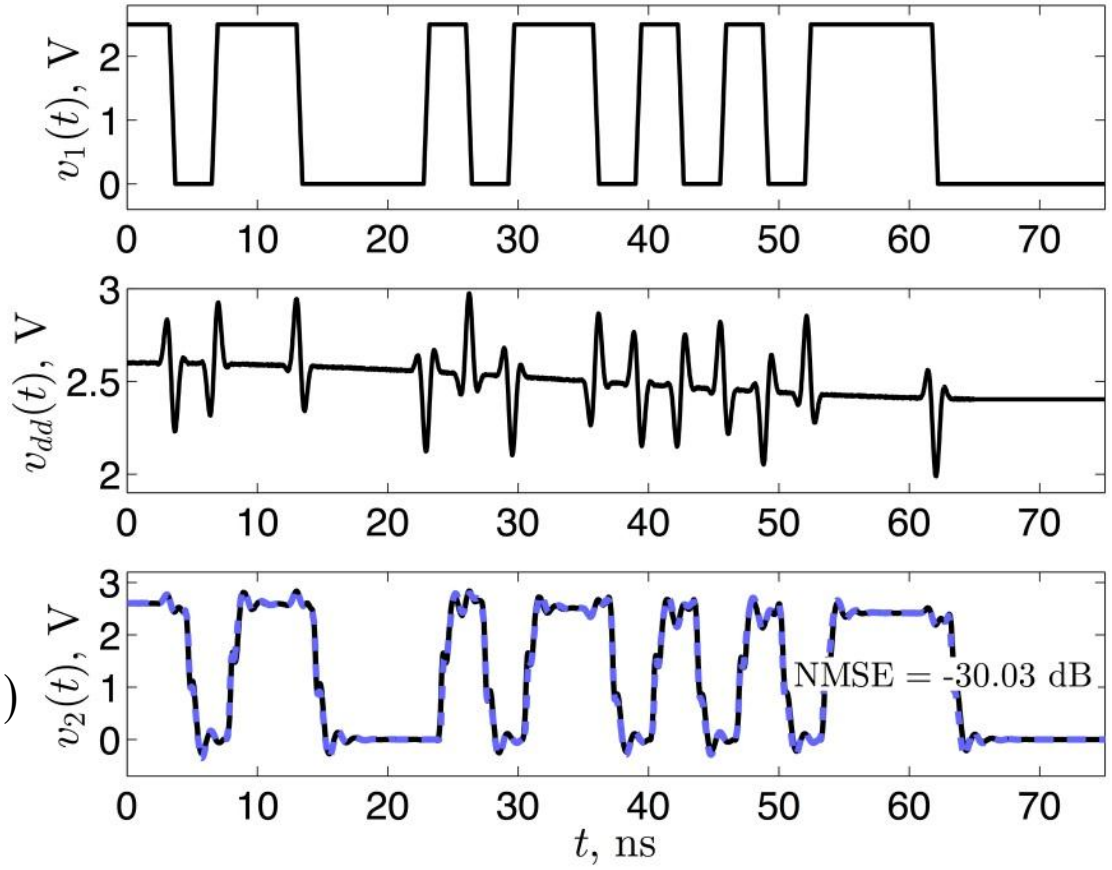


Accounting for Vdd variation



$$\hat{e}(v_1, v_{dd}) = \frac{\hat{e}(v_1, VDD)}{VDD} v_{dd}$$

$$G_H(v_2, v_{dd}) = a(v_{dd}) G_H(v_2, VDD) + b(v_{dd})$$



Conclusion

Top down approach: circuit theory → macromodel.

Easy implementation.

Basic building block for future EDA tools.

Good potential in solving inaccuracies related to jitter, overclocking, etc.

References:

Conference paper : C. Diouf, M. Telescu , N. Tanguy, I.S. Stievano, F.G. Canavero, “Robust nonlinear models for CMOS buffers”, 20th IEEE Workshop on Signal and Power Integrity, May 2016, Turin, taly
Extended paper: C. Diouf, M. Telescu, I. S. Stievano, N. Tanguy, F. G. Canavero, “Simplified topology for IC buffer behavioural models”, IET Circuits, Devices & Systems, 2016 (in press).