Multiport I/O Model Computation For Power-aware SI Simulation

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WAEL DGHAIS AND F. H. BELLAMINE

waeldghais@ua.pt/wael.dghais@hotmail.co.uk

Institut Supérieur des Sciences Appliquées et de Technologie de Sousse, Tunisia

PRESENTATION OUTLINES

1-Introductions/Motivations

2- IBIS Model for an Inverter

-Input Signal Decomposition

-Functions Decomposition

3-IBIS Hybrid Automaton Representation

4-Event-Driven IBIS Implementation

5- Multiport Power-Aware Behavioral Model

-Last Stage Extraction

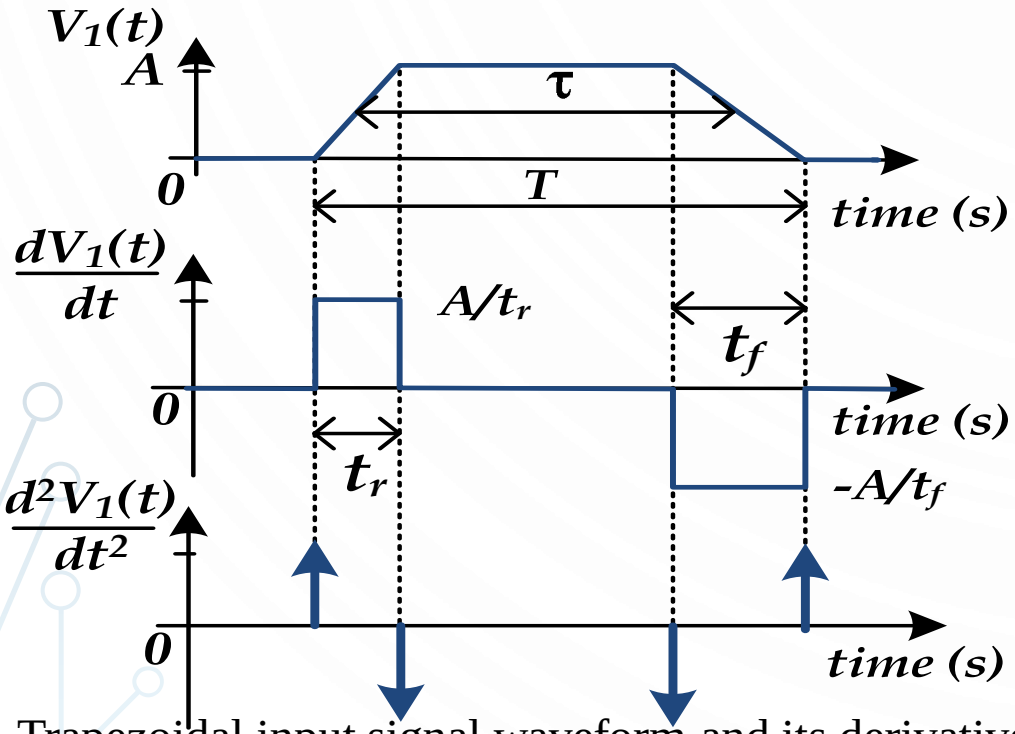
-Pre-driver Stage Extraction

6-Verification/Validation Setup and Results

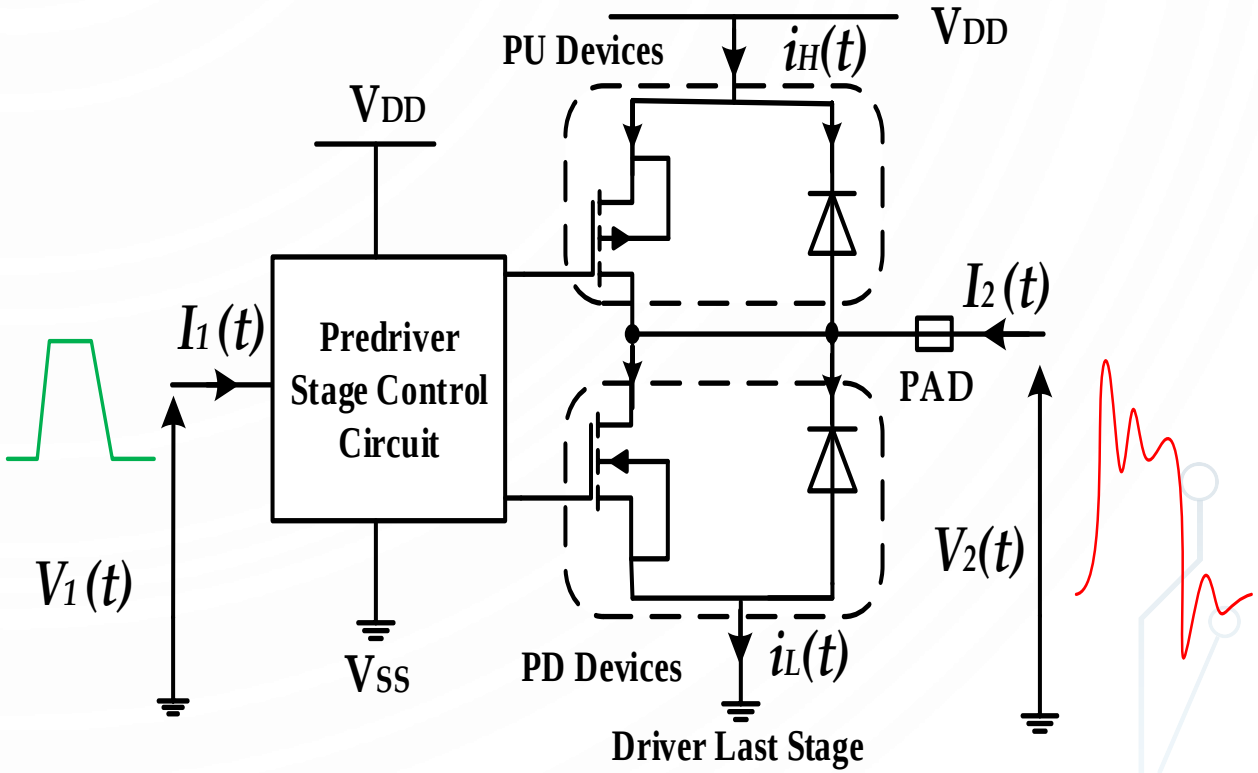
7- Conclusions

INTRODUCTION

- The driver's input signals are encoded as on-off non return to zero (NRZ) or pulse amplitude modulated (PAM) signals.
- Real digital (i.e. discrete) waveforms have a certain non-zero rise and fall times that describe the switching between these two input DC high (*H*) and low (*L*) logic levels states.



Trapezoidal input signal waveform and its derivatives



The I/O buffer's structure with its main electrical variables

MOTIVATIONS

- The adequate methodology to address the I/O modelling task is to apply hybrid modelling procedure that integrates both the continuous electrical variables and discrete-controlled signals to describe the driver's dynamics

- For instance, nonlinear-accurate "booleanization" of continuous dynamics (ABCD-NL) was proposed to capture the AMS component's analog dynamic behavior using purely Boolean models [1].

- This work will extend this approach [1] to analyze the predriver's model formulation presented by the equivalent circuit I/O buffer information specification (IBIS) model [3] and the other parametric approaches [4], [5].
- IBIS numerical model is based on a nonlinear hybrid automaton that combines the interaction between discrete-controlled models for capturing the switching behavior [2], [6] (i.e. **finite state machine (FSM)** model [7]) and the local models structure characterized by continuous evolving variables (e.g. **nonlinear differential equation (NDE) model**).

INPUT SIGNAL DECOMPOSITION

At constant power supplies V_{DD} and V_{SS}, the driver's model NDE representation is :

$$\boldsymbol{I_2(t) = \Phi\left(\vec{V}(t), \dot{\vec{V}}(t), \ldots \vec{V}^{(m)}(t)\right)}$$

- $V(t) = [V_1(t), V_2(t)]^T$ is the vector of state variables. m describes the order of the system.
- $\Phi(\cdot)$ is a multivariable nonlinear function that defines a NDE relating the observable output current $I_2(t)$ with the vector of state variables and its higher derivatives.

- The complexity of this general NDE formulation can be reduced using a discretization of the driver's continuous nonlinear dynamic trajectory based on input signal or state variables decomposition/partitioning.

- The choice of an appropriate state quantization technique must be carefully considered with this approach in order to balance the modeling accuracy and running complexity

FUNCTIONS DECOMPOSITION

The PU and PD output nonlinear admittances, are described by the $F_L(\cdot)$ and $F_H(\cdot)$ functions, respectively [5].

$$\begin{cases} I_L(t) = F_L\left(V_2(t), \dot{V}_2(t)\right) = \Phi\left(V_1 = 0, V_2(t), \dot{V}_2(t)\right) \\ I_H(t) = F_H\left(V_2(t), \dot{V}_2(t)\right) = \Phi\left(V_1 = V_{DD}, V_2(t), \dot{V}_2(t)\right) \end{cases}$$

- The $F_L(\cdot)$ and $F_H(\cdot)$ model the (I-V) and the (C-V) characteristics of the PU and PD devices while the input is kept at high and low logic levels while varying the output voltage $V_2(t)$.

- The function, $\Phi(\cdot)$, can be analytically approximated as a product of two functions, knowing its two samples at two different DC inputs values (e.g. $F_L(\cdot)$ and $F_H(\cdot)$ functions), by a linear interpolation with respect to the variable V_1:

$$I_2(t) = w_H(V_1(t)) \times F_H\left(V_2(t), \dot{V}_2(t)\right) + w_L(V_1(t)) \times F_L\left(V_2(t), \dot{V}_2(t)\right)$$

IBIS MODEL FOR AN INVERTER

$$I_2(t) = w_H(V_1(t)) \times F_H\left(V_2(t), \dot{V}_2(t)\right) + w_L(V_1(t)) \times F_L\left(V_2(t), \dot{V}_2(t)\right)$$

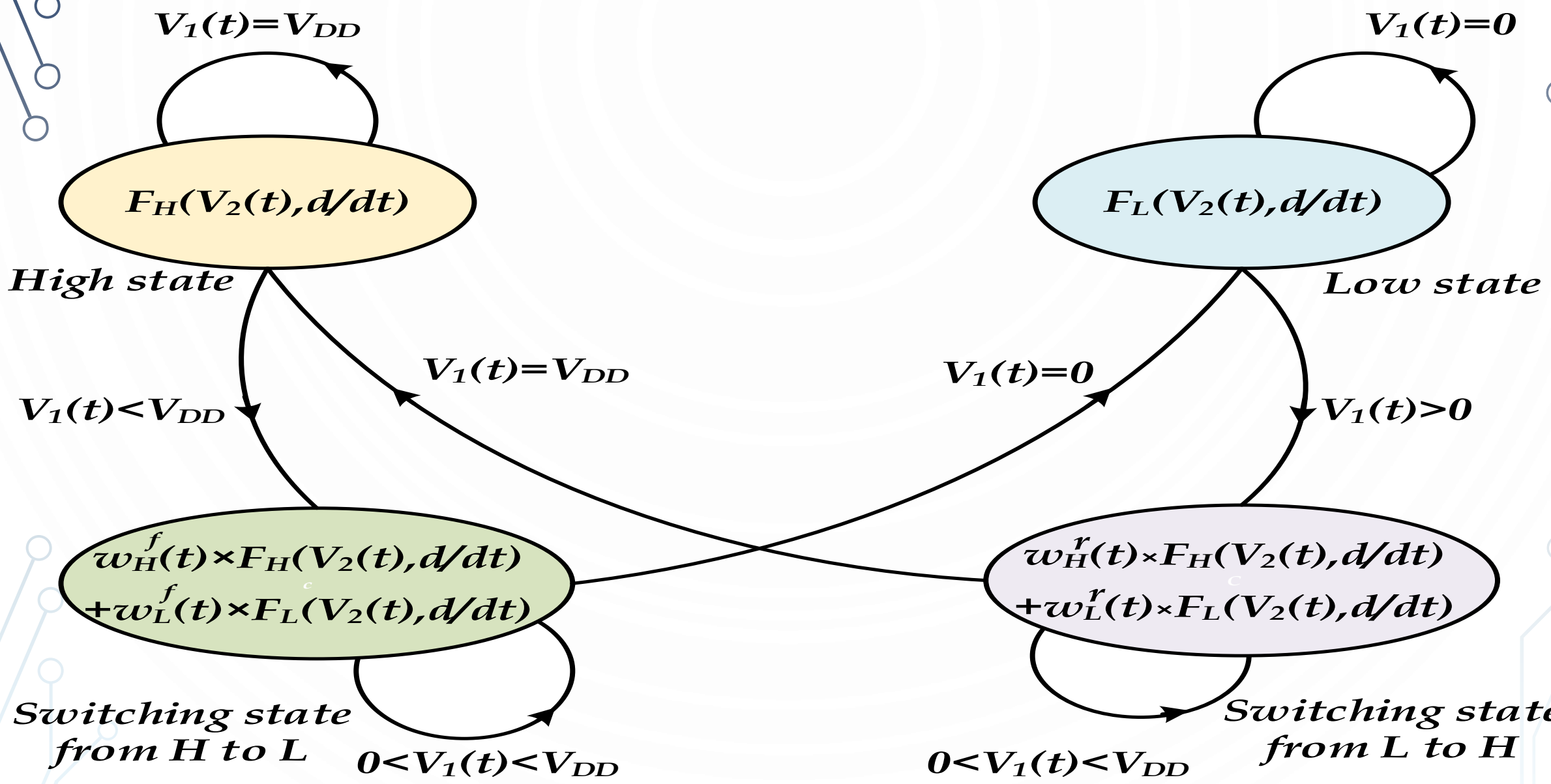
- $w_H(t) = \frac{V_1(t) - V_{SS}}{V_{DD} - V_{SS}}$ and $w_L(t) = \frac{V_{DD} - V_1(t)}{V_{DD} - V_{SS}}$ capture the input port static switching characteristics. $(w_H(t) + w_L(t) = 1)$
- This formulation represents the first IBIS version v1.0 that has no dynamics reflected in the driver's input port.
- The transitions between the local models occur instantaneously and it is valid only for predicting signal distortion of one inverter at a low data rate

IBIS Hybrid Automaton Representation

- The switching between the local models is a continuous flow that occurs with respect to time. This switching behavior has to be integrated in the model in order to reflect the real hybrid device continuous trajectories which traverse across this quantized continuous state space [2].
- The pre-driver's nonlinear dynamic manifest itself by asymmetry distortion of the input rising, (r), and falling, (f), edges.
- IBIS specifications introduce the four voltage-time (V-t) tables that are used to compute the scaling timing signals $w_L^n(t)$ and $w_H^n(t)$ in order to improve the switching accuracy [3]. The event-driven IBIS model formulation is [5]:

$$\boldsymbol{I_2(t) = w_L^n(t) \times F_L\left(V_2(t), \dot{V}_2(t)\right)}$$
$$\boldsymbol{+w_H^n(t) \times F_H\left(V_2(t), \dot{V}_2(t)\right); n = r, f}$$

Hybrid automaton representation of the IBIS computational process in predicting the output current $I_2(t)$.



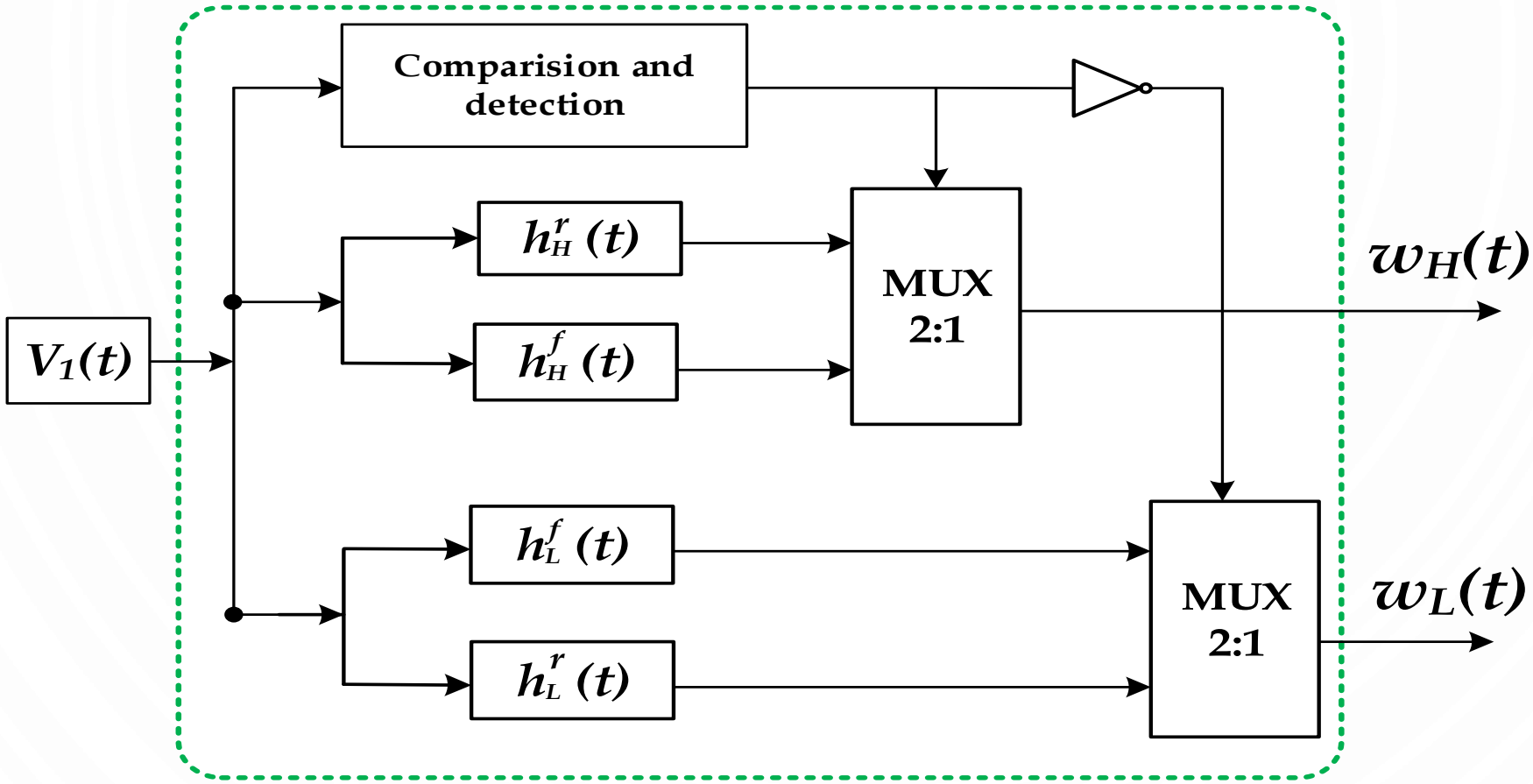
EVENT-DRIVEN IBIS IMPLEMENTATION (1)

- Instead of using a fixed timing V-t table stored in the EDA model library that will be time-driven controlled, event-driven linear filter will be developed in order to assure the mapping from the NRZ input signal and the four timing signals, $w(t)$.

- An extraction of the impulse response, $h(t)$, from the observable trapezoidal input response was carried out by computing the derivative of the $w(t)$ signals providing the input-output V-t time series data according to the IBIS specifications

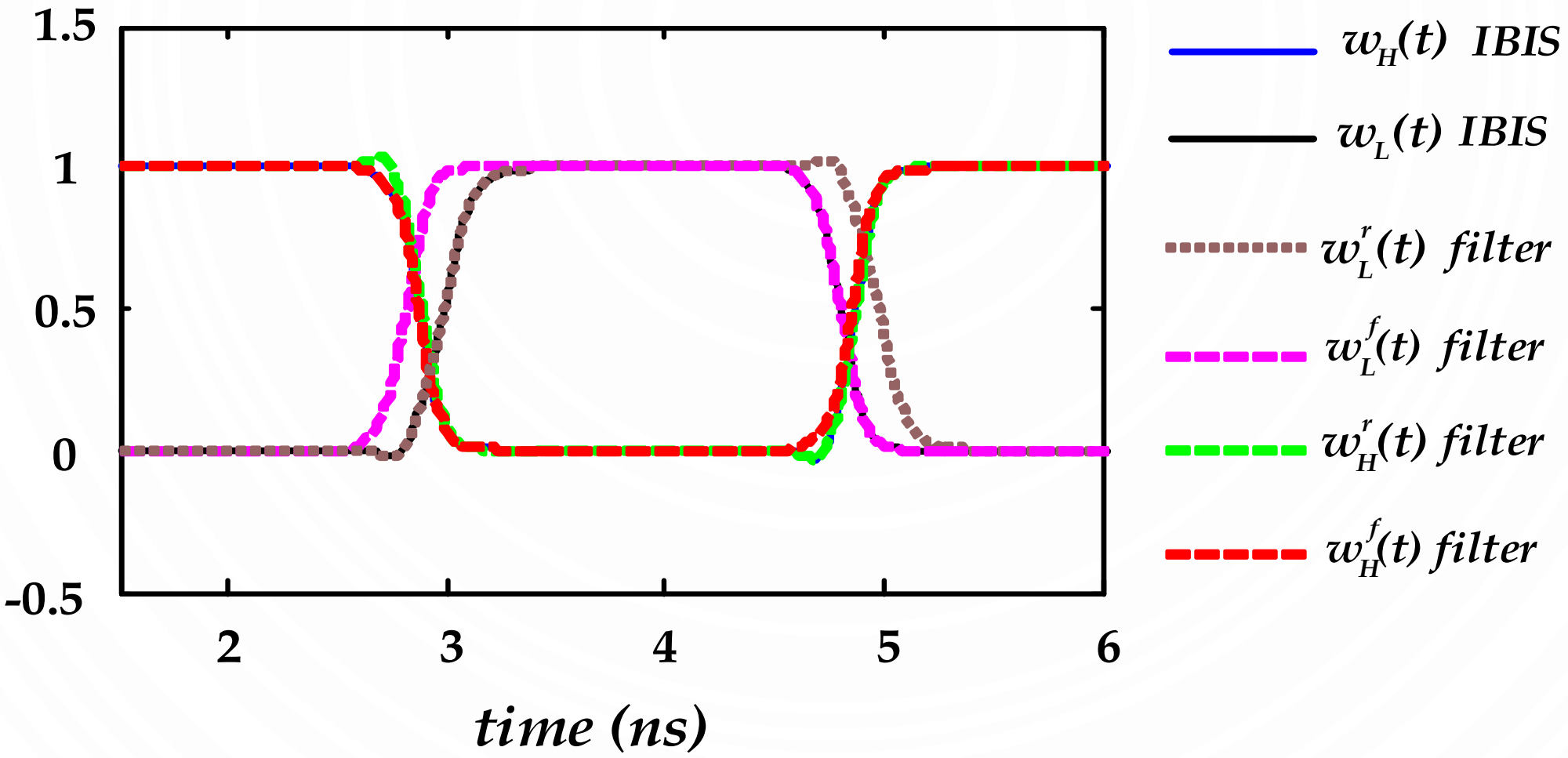
$$\begin{cases} h_L^n(t) = \dfrac{dw_L^n(t)}{dt} \\ h_H^n(t) = \dfrac{dw_H^n(t)}{dt} \end{cases} ; n = r, f$$

EVENT-DRIVEN IBIS IMPLEMENTATION (2)



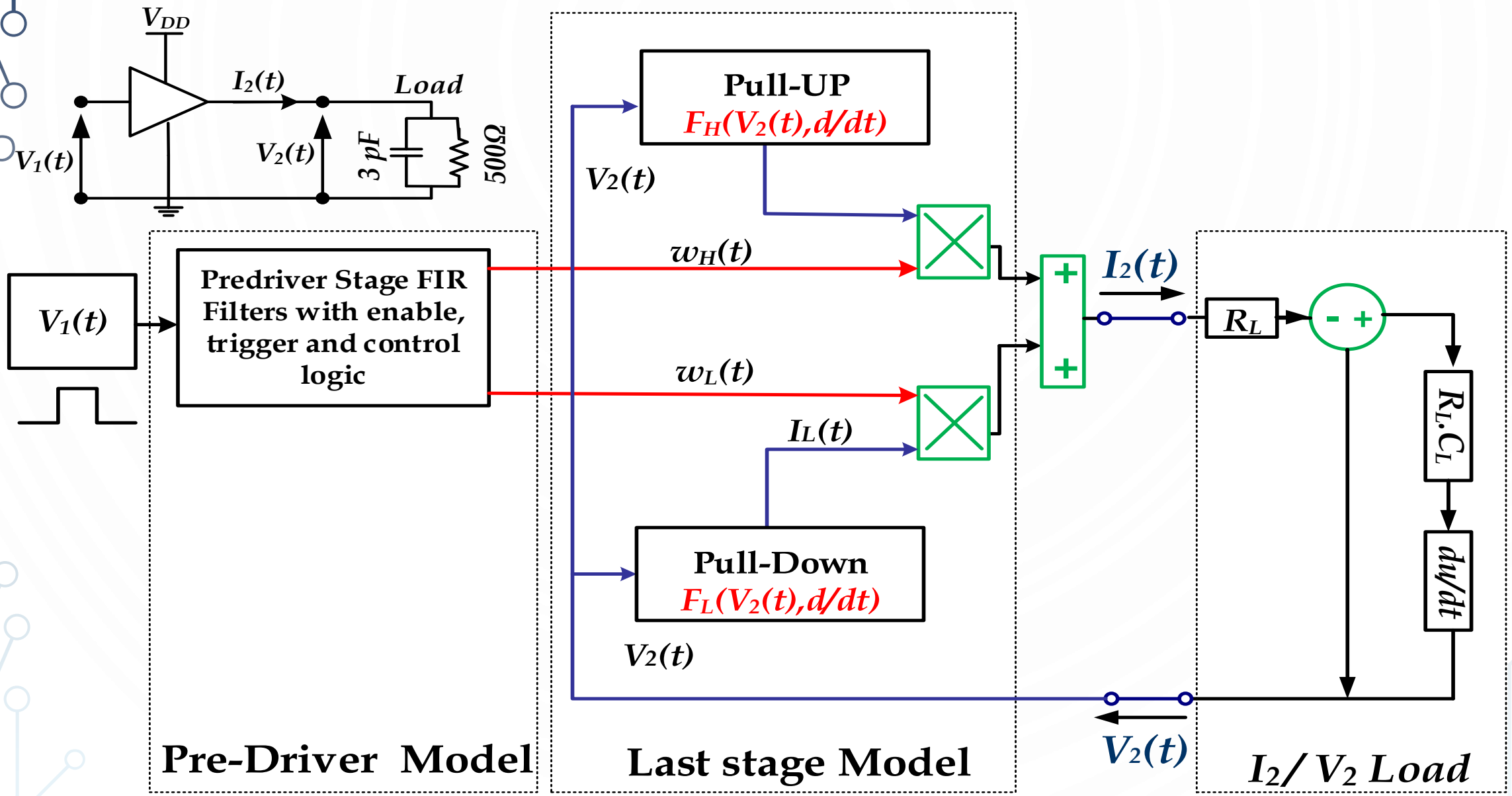
- The synthesis of the adequate discrete signal controlling the multiplexing of the filters output according to the duration of the high and low levels and the event occurring with rising and falling transition of the input signal is performed by the detection/comparison block

VERIFICATION RESULTS

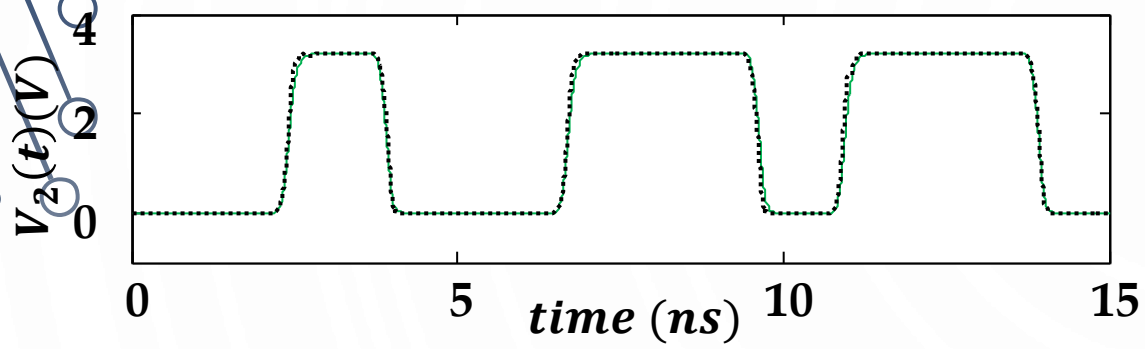


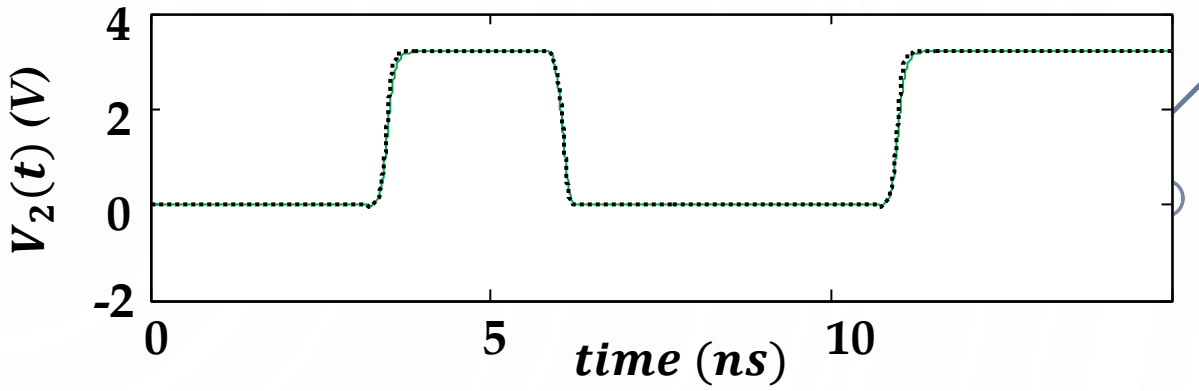
Predicted timing signals by the filter bank of the predriver's event-driven model implementation,

VALIDATION SETUP

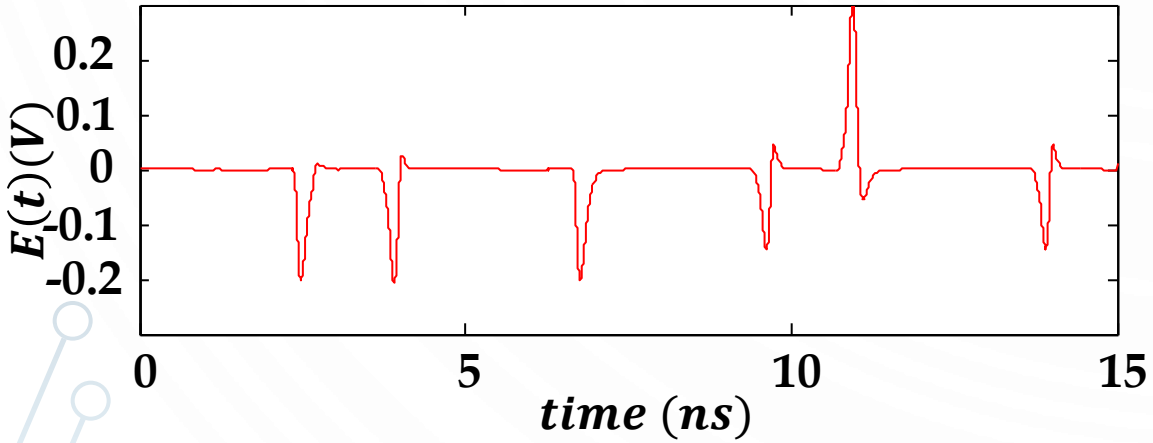


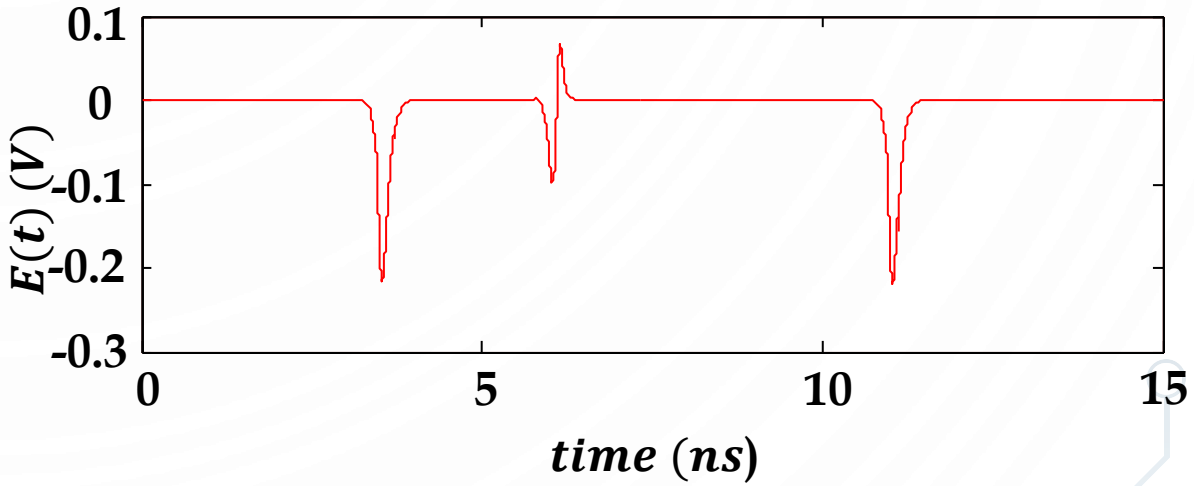
VALIDATION RESULTS





Behavioral Model ..... Physical TL Model





•Comparision between the predicted output voltage waveform, $V_2(t)$ for input data rate of 700Mbps and *tr=tf=500 ps*.

•Comparision between the predicted output voltage waveform, $V_2(t)$ for input data rate of 400Mbps and *tr=tf=500 ps*.

MULTIPORT POWER-AWARE BEHAVIORAL MODEL

- The SSO causes PG voltage fluctuations that affect the transistors bias points and their driving capabilities. The output current is expressed as a first order dynamic as follows:

$$I_2(t) = P_H\left(X_u(t), \frac{dX_u(t)}{dt}\right) + P_L\left(X_d(t), \frac{dX_d(t)}{dt}\right)$$

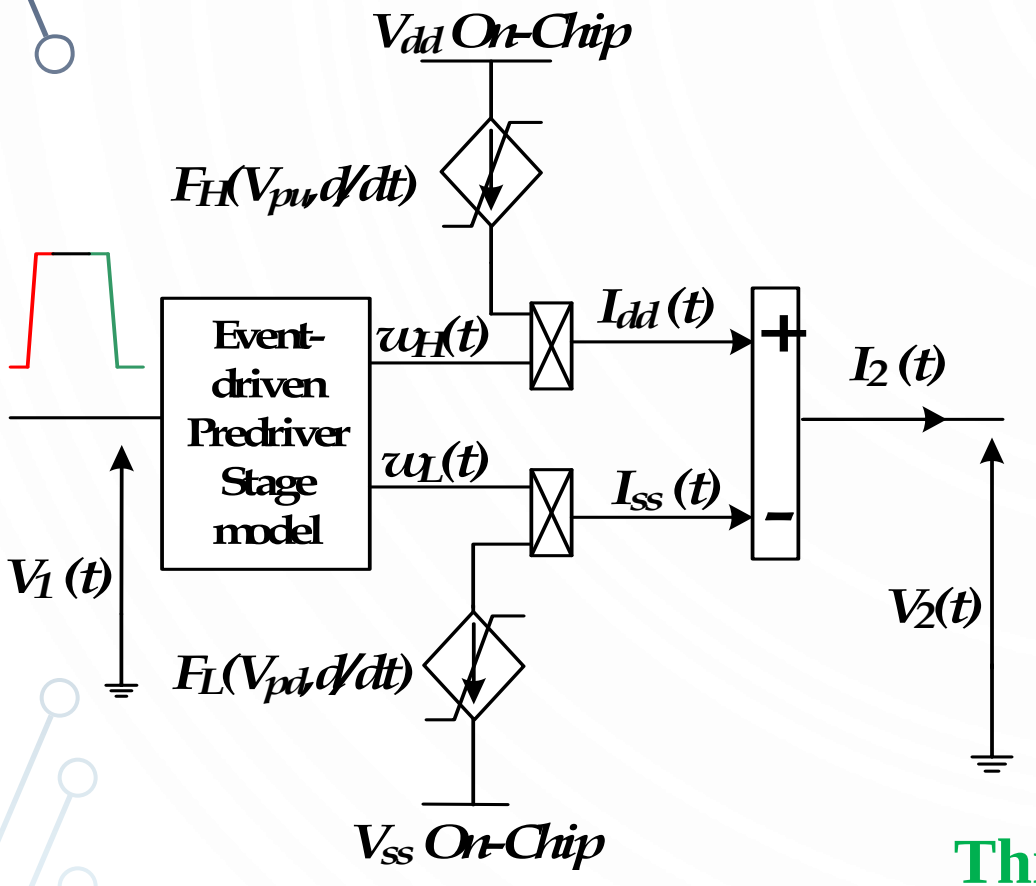
$X_u(t) = [V_{zu}(t), V_{pu}(t)]^T$ and $X_d(t) = [V_{zd}(t), V_{pd}(t)]^T$. The $P_u(\cdot)$ and $P_d(\cdot)$ are nonlinear multivariate dynamic functions.

- The function $P_H(\cdot)$ can be decomposed as the product of two nonlinear multivariate functions $T_H(\cdot)$ and $F_H(\cdot)$

$$I_{dd}(t) = P_H\left(X_u(t), \frac{dX_u(t)}{dt}\right) \Rightarrow I_{dd}(t) \cong T_H\left(V_{zu}(t), \frac{dV_{zu}(t)}{dt}\right) \cdot F_H\left(V_{pu}(t), \frac{dV_{pu}(t)}{dt}\right)$$

STATIC GATE MODULATION EFFECT

- Driver's 2-port IBIS model for the PU and PD network



BIRD-98.3 : The normalized nonlinear functions $G_H(V_{dd}(t))$, and $G_L(V_{ss}(t))$, accounting for the PG voltage variations were extracted through a voltage dc sweep while recording the respective current in saturation mode.

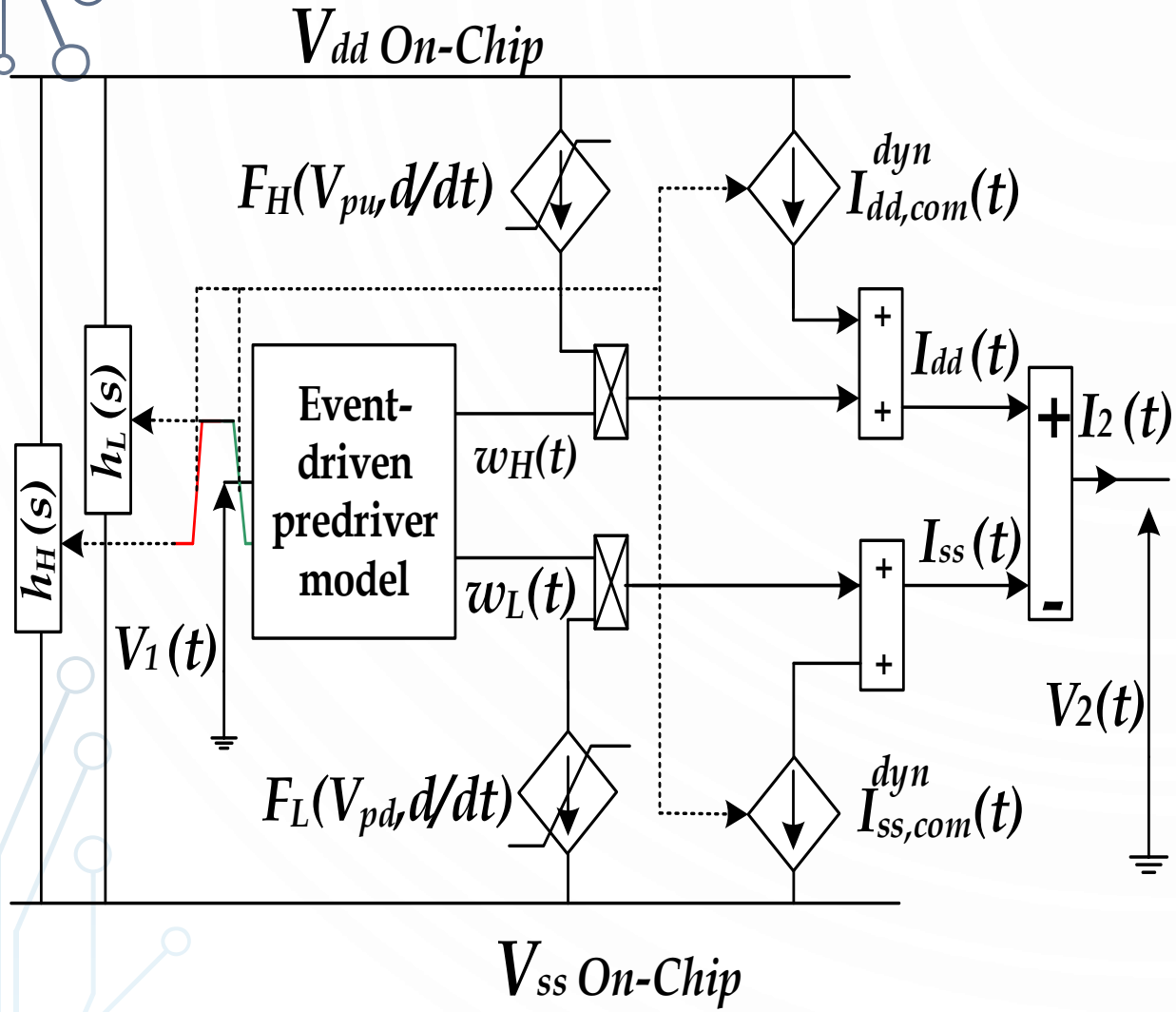
$$I_2(t) = w_H^n(t) \cdot G_H(V_{dd}(t)) \cdot F_H\left(V_{pu}(t), d/dt\right) + w_L^n(t) \cdot G_L(V_{ss}(t)) \cdot F_L\left(V_{pd}(t), d/dt\right)$$

$$I_2(t) = w_H^n(t) \cdot F_H\left(V_{pu}(t), d/dt\right) + w_L^n(t) \cdot F_L\left(V_{pd}(t), d/dt\right); n = \{r, f\}$$

This formulation is inaccurate a because $G_H(V_{zu}(t)) \neq G_H(V_{dd}(t)) - G_H(V_z(t))$ and $G_L(V_{zd}(t)) \neq G_L(V_z(t)) - G_L(V_{ss}(t))$ [12].

SWITCHING COMPOSITE CURRENT

The BIRD 95.6 models the dynamic contribution of the power supply fluctuation by adding a timing current (I-t) to capture the missing current predicted by IBIS at the power supply port



$$\begin{cases} I^{dyn,n}_{dd,com}(t) = I^{TL,n}_{dd}(t) - I^{IBIS,n}_{dd}(t) \\ I^{dyn,n}_{ss,com}(t) = I^{TL,n}_{ss}(t) - I^{IBIS,n}_{ss}(t) \end{cases}$$

where $I^{TL,n}_{dd}(t)$ and $I^{IBIS,n}_{dd}(t)$ represent the PG currents predicted by the transistor level (TL) and the IBIS models, respectively.

$$I_2(t) = w^n_H(t) \cdot G_H(V_{dd}(t)) \cdot F_H(V_{pu}(t), d/dt) + w^n_L(t) \cdot G_L(V_{ss}(t)) \cdot F_L(V_{pd}(t), d/dt) + \int_0^{+\infty} h_H(t-\tau) \cdot p(\tau) d\tau + \int_0^{+\infty} h_L(t-\tau) p(\tau) d\tau + I^{dyn,n}_{dd,com}(t) + I^{dyn,n}_{ss,com}(t);\ n = \{r, f\}$$

LAST STAGE EXTRACTION

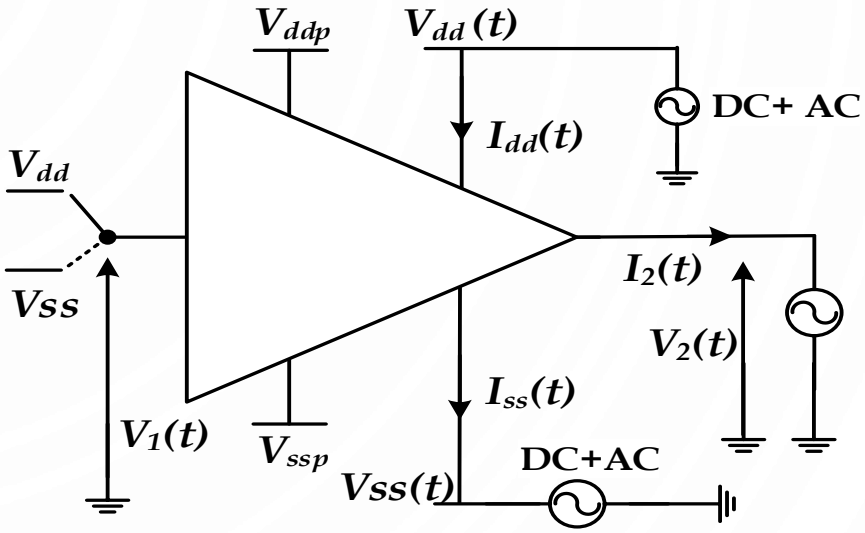
- The $F_u(\cdot)$ and $F_d(\cdot)$ are expanded as a summation of weighted hyperbolic tangent (i.e. tanh(·)) functions

$$\begin{cases} F_H(t) = \sum_{j=1}^{L_u} B_u + Q_{u,j} \cdot tan\,h(A_{u,j} \cdot R_u(t) + C_{u,j}) \\ F_L(t) = \sum_{j=1}^{L_d} B_d + Q_{d,j} \cdot tan\,h(A_{d,j} \cdot R_d(t) + C_{d,j} \end{cases}$$

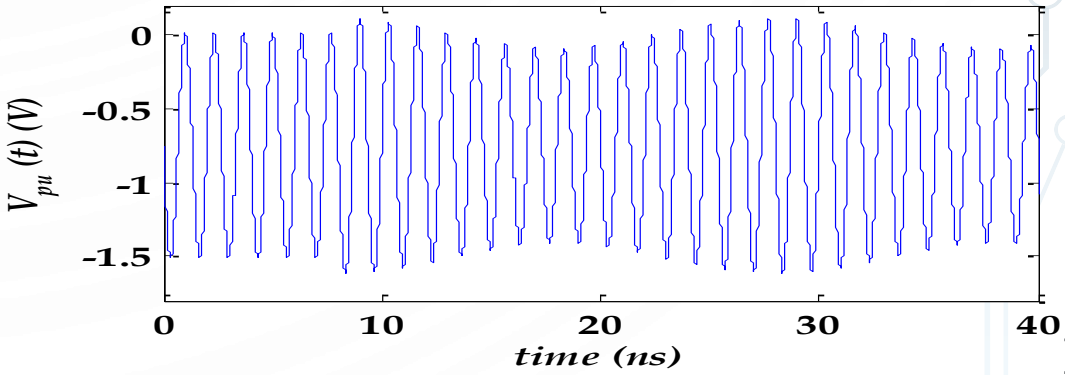
- Multiple high-frequency sinusoidal signals are used at the PG and the output ports

$$\begin{cases} V_2(t) = a_2 + a_{20} sin(2\pi f_2 t + \varphi_2) \\ V_{dd}(t) = a_3 + a_{30} sin(2\pi f_3 t + \varphi_3) \\ V_{ss}(t) = a_4 + a_{40} sin(2\pi f_4 t + \varphi_4) \end{cases}$$

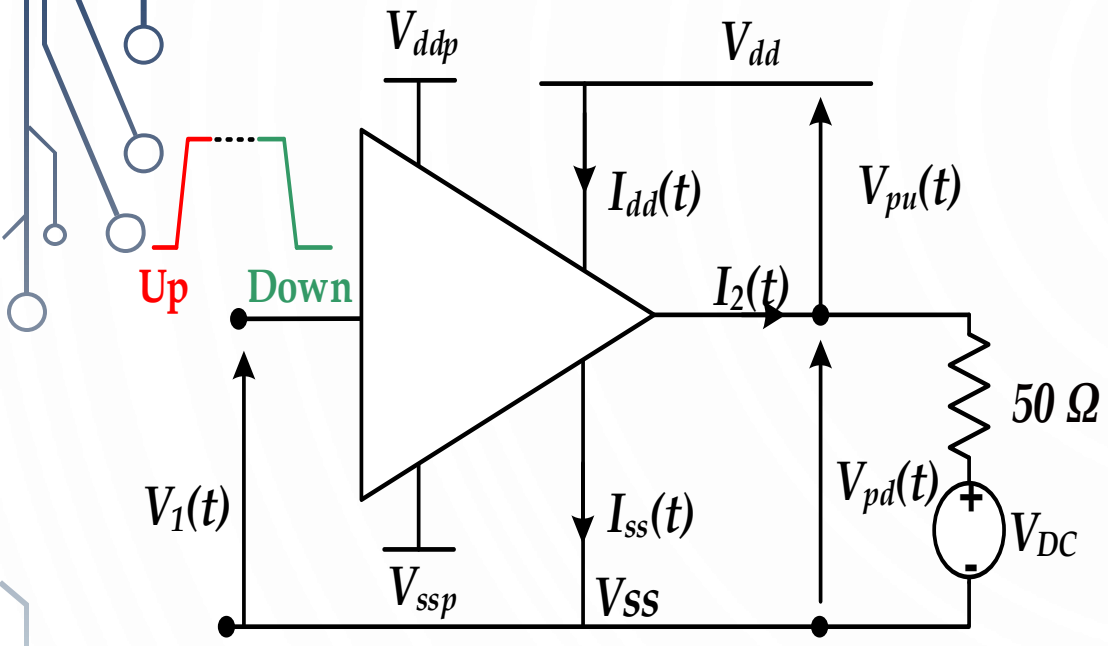
- Large-signal characterization setup.

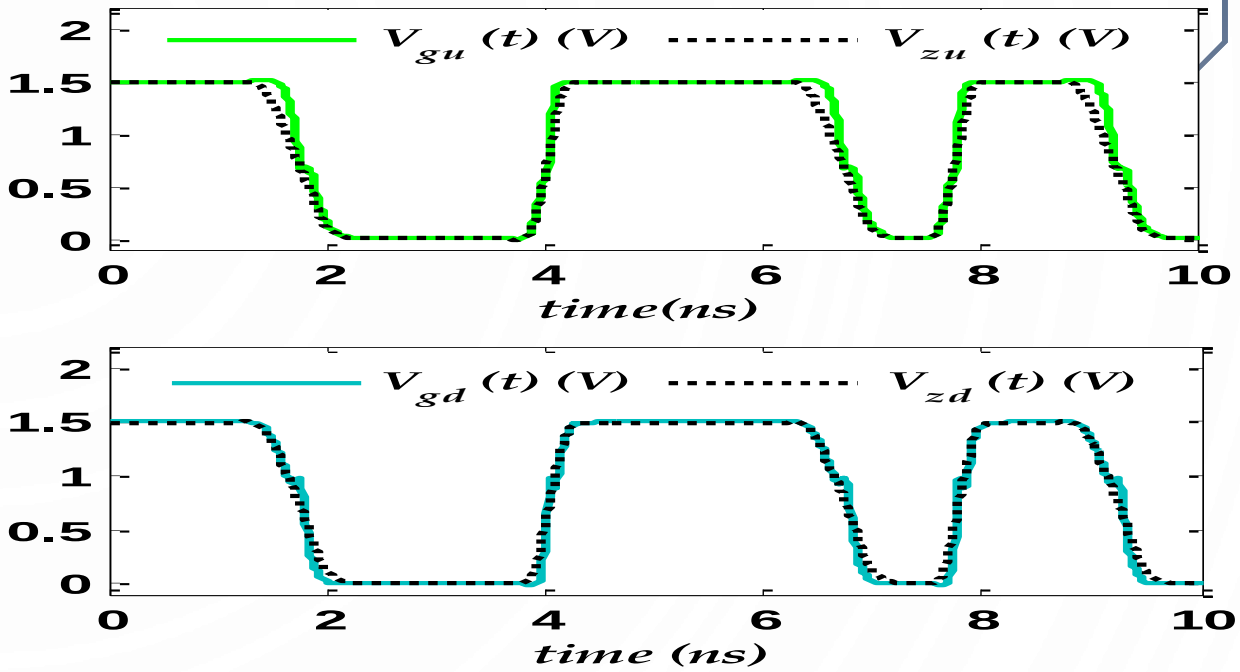


- AM-like $V_{pu}(t)$



PREDRIVER STAGE MODELS





- The time series $\{I_{dd}^{TL,n}(t), I_{ss}^{TL,n}(t), V_2^{TL,n}(t)\}$ and the voltages $V_{2,a}^{TL,n}(t)$ and $V_{2,b}^{TL,n}(t)$ are subjected to the identified model $F_H(V_{pu}, dV_{pu}/dt)$ and $F_L(V_{pd}, dV_{pd}/dt)$ functions to obtain the PG currents $\{I_{dd,a}^n, I_{dd,b}^n, I_{ss,a}^n, I_{ss,b}^n\}$.

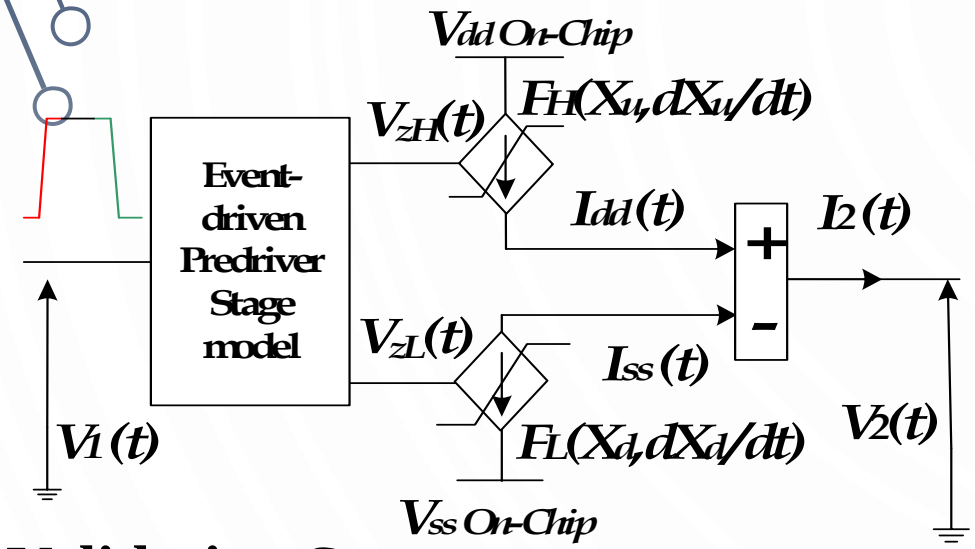
$$\begin{bmatrix} w_H^n(t) \\ w_L^n(t) \end{bmatrix} = \begin{bmatrix} I_{dd,a}^n(t) & I_{dd,b}^n(t) \\ I_{ss,a}^n(t) & I_{ss,b}^n(t) \end{bmatrix}^{-1} \cdot \begin{bmatrix} I_{dd}^{TL,n}(t) \\ I_{ss}^{TL,n}(t) \end{bmatrix}$$

- A linear transformation is applied to retrieve the timing behavior of the pre-driver gate voltage $V_z(t)$.

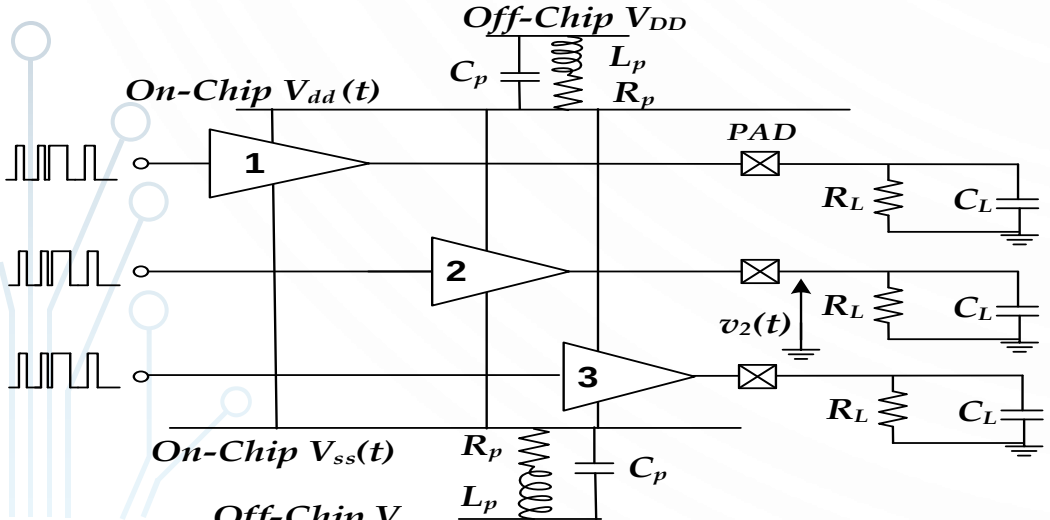
$$\begin{cases} V_{zH}^n(t) = V_{dd}(t) - V_{DD} \times w_H^n(t) \\ V_{zL}^n(t) = V_{DD} \times \left(1 - w_L^n(t)\right) - V_{ss}(t) \end{cases}$$

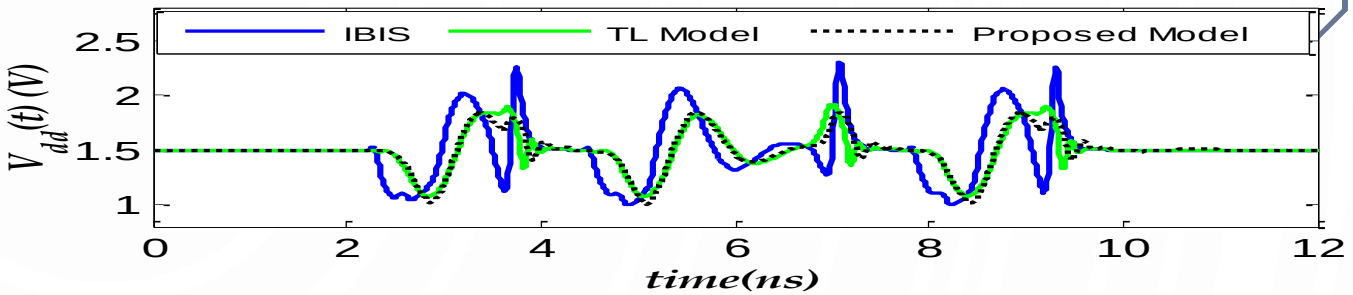
MULTIPORT MODEL'S IMPLEMENTATION

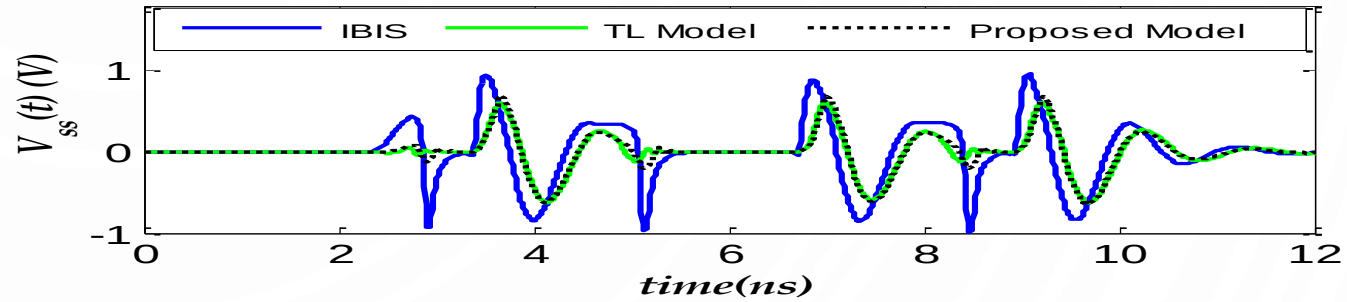
Implemented driver's model

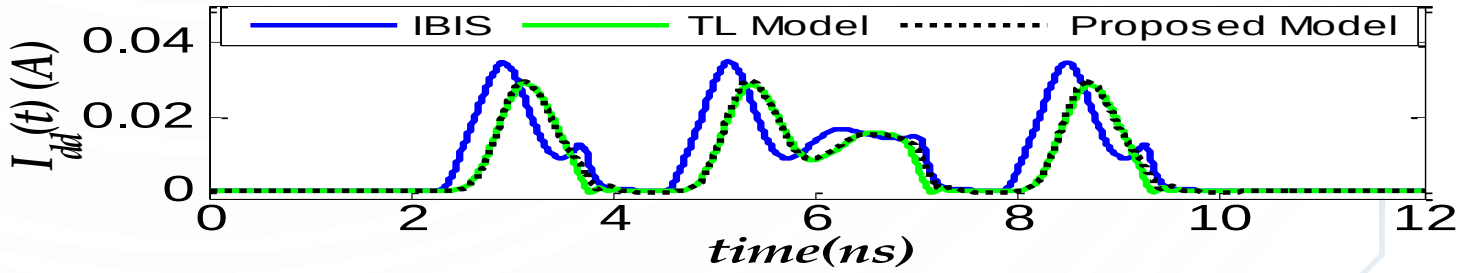


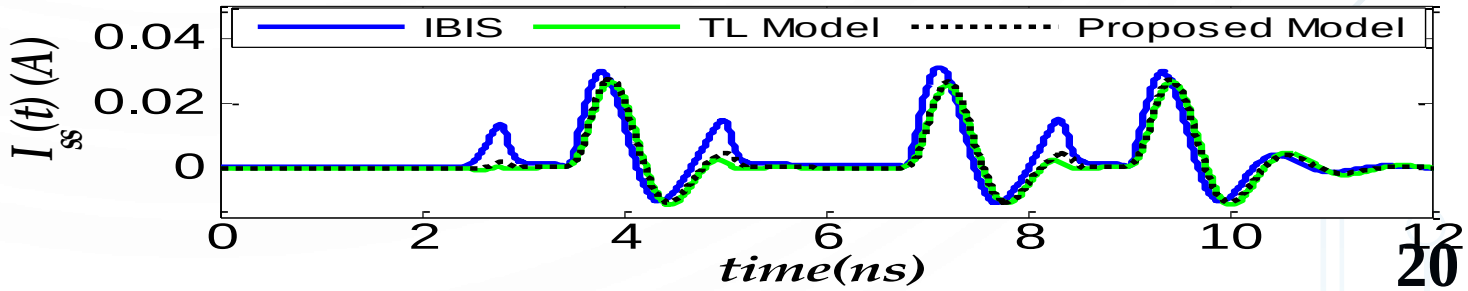
Validation Setup











MULTIPORT MODEL VALIDATION RESULTS

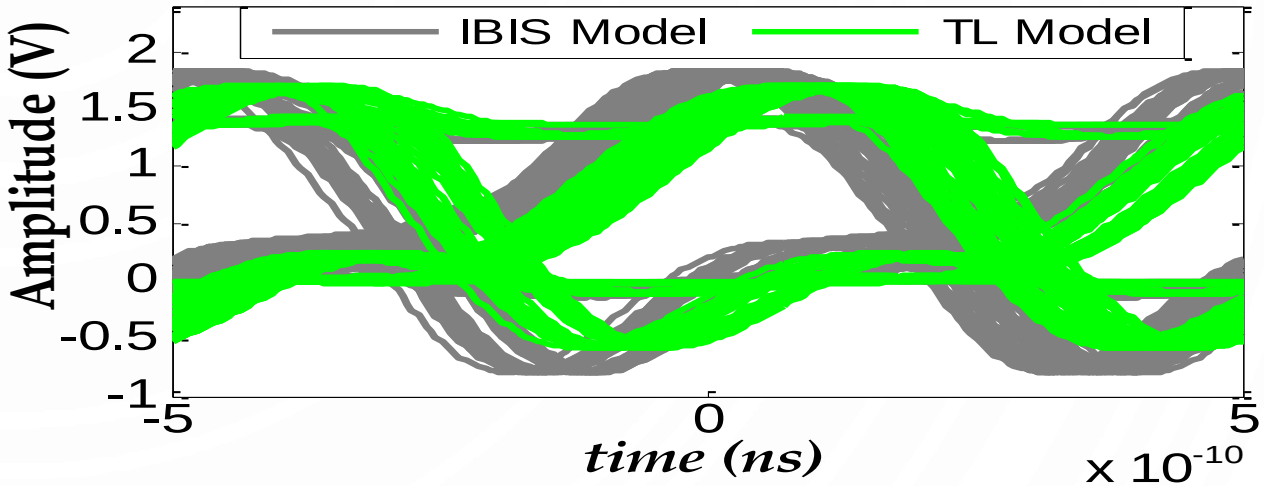
- The normalized mean square error (NMSE) is used to quantify the model's accuracy

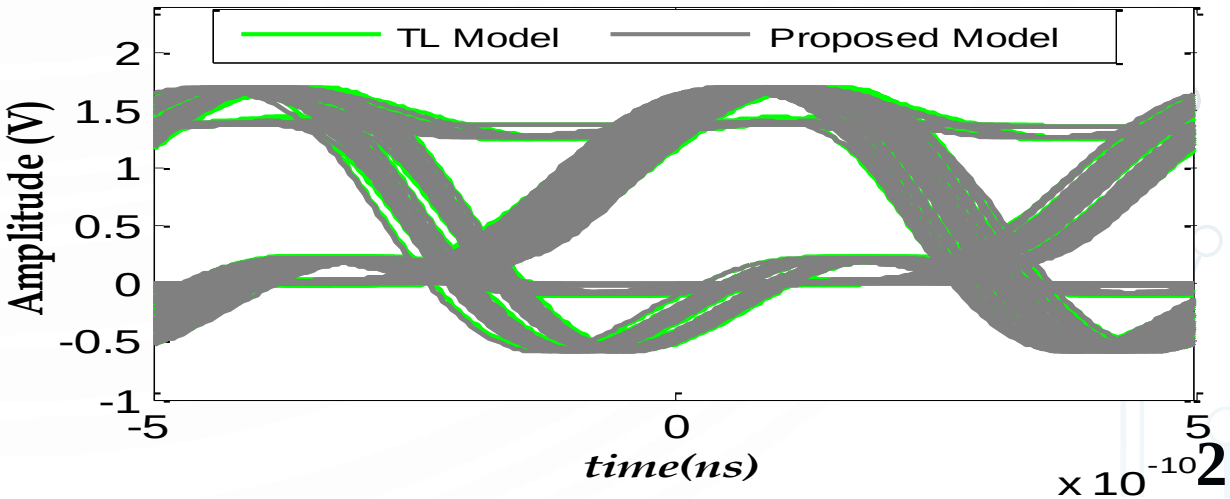
$$NMSE_y = 10log_{10}\left[\frac{\sum_{k=1}^{K}(y(k)-\hat{y}(k))^2}{\sum_{k=1}^{K}(y(k))^2}\right]$$

Simulation's Performance of the Proposed Model in the Validation setup

Model	$NMSE_{V_{ss}}$	$NMSE_{V_{dd}}$	$NMSE_{V_2}$	CPU time (s)
TL	-	-	-	107.29 s
Proposed	-25. 46 dB	-24.87 dB	-30.60 dB	28.92 s
IBIS	-10.50 dB	-11.41 dB	-11.31 dB	22.13 s

- Eye diagram comparison between the TL and the IBIS , and the proposed model..





CONCLUSIONS (1)

- ✓ This work has presented the derivation of the hybrid automaton IBIS driver's model that manifests switching continuous behavior since it mixes the event-triggered predriver's switching dynamics with nonlinear continuous steady state dynamics of the PU and PD models of the driver's last stage,

- ✓ The extracted predriver's model is implemented as a discrete/Boolean controlled bank of a finite impulse response (FIR) filters approximating its circuit's nonlinear dynamics based on quantized states of the input signal,

- ✓ The developed nonlinear hybrid automaton is a well suited modelling approach for capturing highly nonlinear AMS devices by defining the transient evolution of the hybrid AMS DC state under two-level NRZ or PAM multilevel signals excitation.

CONCLUSIONS (2)

- ✓ The static gate modulation does not cover all the static operation two dimensional I-V plane (e.g. $I_{ds} = H(V_{gs}, V_{ds})$) which is highly required for modelling the SSN mechanisms and to cope with I-V plane of short-channel transistors

- ✓ There is some inconsistency between the static and dynamic extension of the 2-piece and IBIS model which should be complementary by removing the static distortions from the I-t dynamic contribution in order to derive a correct model generation.

- ✓ The proposed multiport power-aware I/O buffers model includes the coupling between the input-output signal paths and the power/ground planes. The behavioral model generation procedure is based on the large signal time-domain characterization and formulation and parametric identification for Power-Aware Signal Integrity Analysis.

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