

AGENDA - EUROPEAN IBIS SUMMIT AT SPI 2016

Wednesday, May 11, 2016

**Starhotel Majestic
Corso Vittorio Emanuele II, 54
Turin, Italy**

Room: Vittoria A/B (main SPI conference room)

Sponsors: ANSYS
CST
Keysight Technologies
Synopsys
Zuken

Online Presentations: <http://www.ibis.org/summits/may16/>
(Order and times subject to change)

13:45 REFRESHMENTS AND SIGN IN

14:00 WELCOME AND INTRODUCTOINS

14:10 IBIS Update
Mike LABONTE*, Lance WANG**
*Signal Integrity Software (SiSoft); USA,
**IO Methodology; USA

14:20 Understanding IBIS-AMI Simulations
Richard ALLRED
Signal Integrity Software (SiSoft); USA

14:50 Using IBIS-AMI Models to Maximize Data Rate Given SerDes EQ and Channel ISI/Loss
Donald TELIAN
SiGuys; USA

15:20 Initial Delay Issues in Analog IBIS Buffers
Michael SCHAEDEr, Mariusz FAFERKO, Amir WALLRABENSTEIN
Zuken; Germany

15:40 IBIS + Mpiilog: Current and Future Developments on I/O-Buffer Modeling
Gianni SIGNORINI*#, Claudio SIVIERO**###, Igor Simone STIEVANO**###,
Stefano GRIVET-TALOCIA**###, Michael MIRMAK*###
*Intel Corporation, **Politecnico di Torino;
#Germany, ##Italy, ###USA

16:10 BREAK AND REFRESHMENTS (15 Minutes)
- Reconvene at 16:25

16:25 Models for IC Buffers: A Top-down Approach

Cherif DIOUF*#, **Mihai TELESU****#, N. TANGUY**#,
Igor Simone STIEVANO***##, Flavio G. CANAVERO***#
*Ecole Nationale d'Ingenieurs de Brest,
**Universite de Bretagne Occidentale,
***Politecnico di Torino;
#France, ##Italy

16:55 Multiport I/O Model Computation for Power-Aware SI Simulation

Wael DGHAI*, Fethi BALLAMINE**
*University of Soursse, **Universite de Carthage; Tunisia

17:35 On-Die Decoupling Model Improvements for IBIS Power Aware Models

Randy WOLFF#, Aniello VISCARDI##
Micron Technology; #USA, ##Italy

17:55 CLOSING REMARKS

Lance WANG, IO Methodology, IBIS Vice-chair, USA

18:00 END OF MEETING