Interconnect Task Group Update – Package Modeling

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2015 European IBIS Summit

May 13, 2015 Berlin, Germany

IBIS Interconnect Task Group

Meets Wednesdays at 8:00 a.m. Pacific Time

http://www.eda.org/ibis/interconnect_wip/

Major Contributors

▪ Cadence Design Systems	Brad Brim
▪ Intel Corporation	Michael Mirmak
▪ Keysight Technologies	Radek Biernacki
▪ Mentor Graphics	Arpad Muranyi
▪ Micron Technology	Justin Butterfield, Randy Wolff
▪ Signal Integrity Software	Walter Katz
▪ Teraspeed Labs	Bob Ross

Advanced Package Modeling BIRD Overview

A BIRD is close to complete to add advanced package and on-die interconnect modeling capabilities to IBIS

The BIRD adds support for:

- Broadband and coupled models using IBIS-ISS (standardized SPICE) and Touchstone data
- Separate on-die and package interconnect models and combined on-die and package interconnect models
- Independent or coupled supply and signal interconnect models
- Singled-ended and differential interconnect models
- Single pin to single buffer signal connections
  - Branched signal paths such as stacked die to be supported in future Electrical Module Description (EMD) syntax

Advanced Package Modeling BIRD Overview

Hierarchy:

- New package models and legacy package models can co-exist in IBIS
  - Simulators can choose to use either one if both exist for a given set of signals
  - Assumes a simulator will not try to combine new and legacy package models in the same simulation (models are uncoupled with no interactions)

Pre-layout Support:

- Signal model Terminals referenced by a Pin's Model_name (DQ, etc.)
- Supply model Terminals referenced by a Pin's Signal_name (i.e. VDDQ)

Post-layout Support:

- Signal model Terminals can connect to Pins, Die Pads and Buffer Terminals referenced by a Pin's Pin_name (1, A1, etc.)
- Supply model Terminals can connect to Pins, Die Pads and Buffer Terminals with 'bussing' options to short at each level

BIRD Syntax

[Interconnect Model Selector]/[End Interconnect Model Selector]

- Used to list available interconnect models for a [Component]

[Begin Interconnect Model]/[End Interconnect Model]

- Mark the start and end of an interconnect model description

Subparameters:

- Manufacturer
- Description
- Param – parameters passed into an IBIS-ISS subcircuit (single value)
- File_TS – external Touchstone file reference
- File_IBIS-ISS – external IBIS-ISS file reference
- Unused_Terminal_Termination – unconnected terminal terminations
- Number_of_Terminals – total number of model terminals
- Terminal – defines unique characteristics of each model terminal

Terminals

Terminals of the interconnect model can be located at many package or die locations

- Pins
- Die Pads
  - Signal (I/O)
  - Supply (POWER and GND)
- Buffers
  - Signal (I/O)
  - Supply
    - Pullup Reference
    - Pulldown Reference
    - Power Clamp Reference
    - Ground Clamp Reference
    - External Reference

Signal Model Terminals

Terminal <terminal number> <At Pin|DiePad|Buffer> <ID> <What ID means>

One line per terminal

Example Signal (I/O) Terminal records

- Post-layout
  - Terminal 1 Pin_A_signal M8
  - Terminal 2 Pad_A_signal M8
  - Terminal 3 A_signal M8
- Pre-layout
  - Terminal 1 Pin_A_signal DQ Model_name
  - Terminal 2 Pad_A_signal DQ Model_name
  - Terminal 3 A_signal DQ Model_name

Differential Signal Model Terminals

Example Differential Signal (I/O) Terminal records

- Post-layout
  - Terminal 1 Pin_A_signal M8
  - Terminal 2 Pin_A_signal M7
  - Terminal 3 Pad_A_signal M8
  - Terminal 4 Pad_A_signal M7
  - Terminal 5 A_signal M8
  - Terminal 6 A_signal M7
- Pre-layout
  - Terminal 1 Pin_A_signal_pos DQS Model_name
  - Terminal 2 Pin_A_signal_neg DQS Model_name
  - Terminal 3 Pad_A_signal_pos DQS Model_name
  - Terminal 4 Pad_A_signal_neg DQS Model_name
  - Terminal 5 A_signal_pos DQS Model_name
  - Terminal 6 A_signal_neg DQS Model_name

Supply Model Terminals

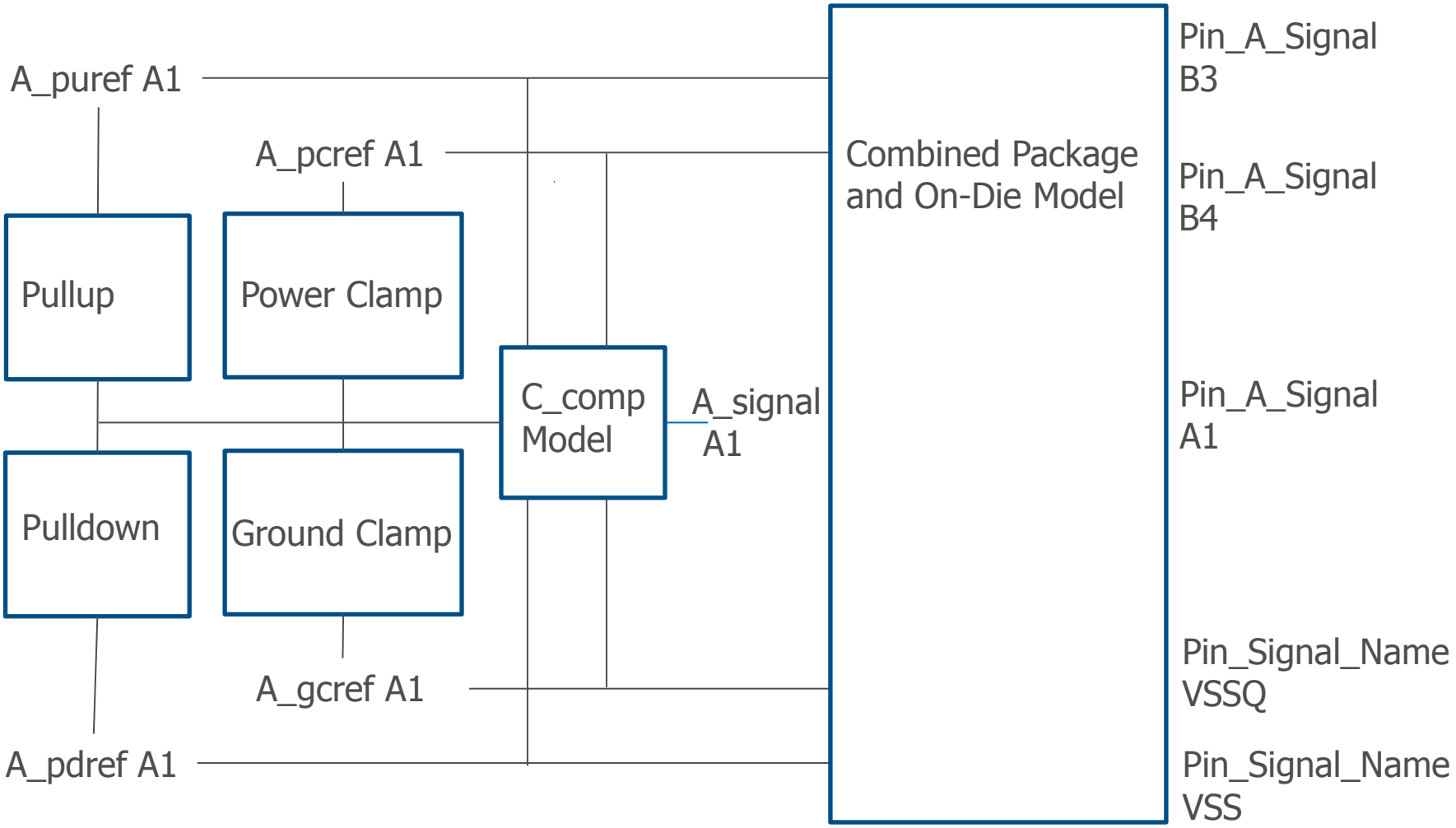
Post-layout

- Using Pins, Pads and Buffers
  - Terminal 1 Pin_A_Signal B1
  - Terminal 2 Pin_A_Signal B2
  - Terminal 3 A_puref M3
- Using Signal_name and Buffers
  - Terminal 1 Pin_A_Signal VDD Signal_name
  - Terminal 2 A_puref M3

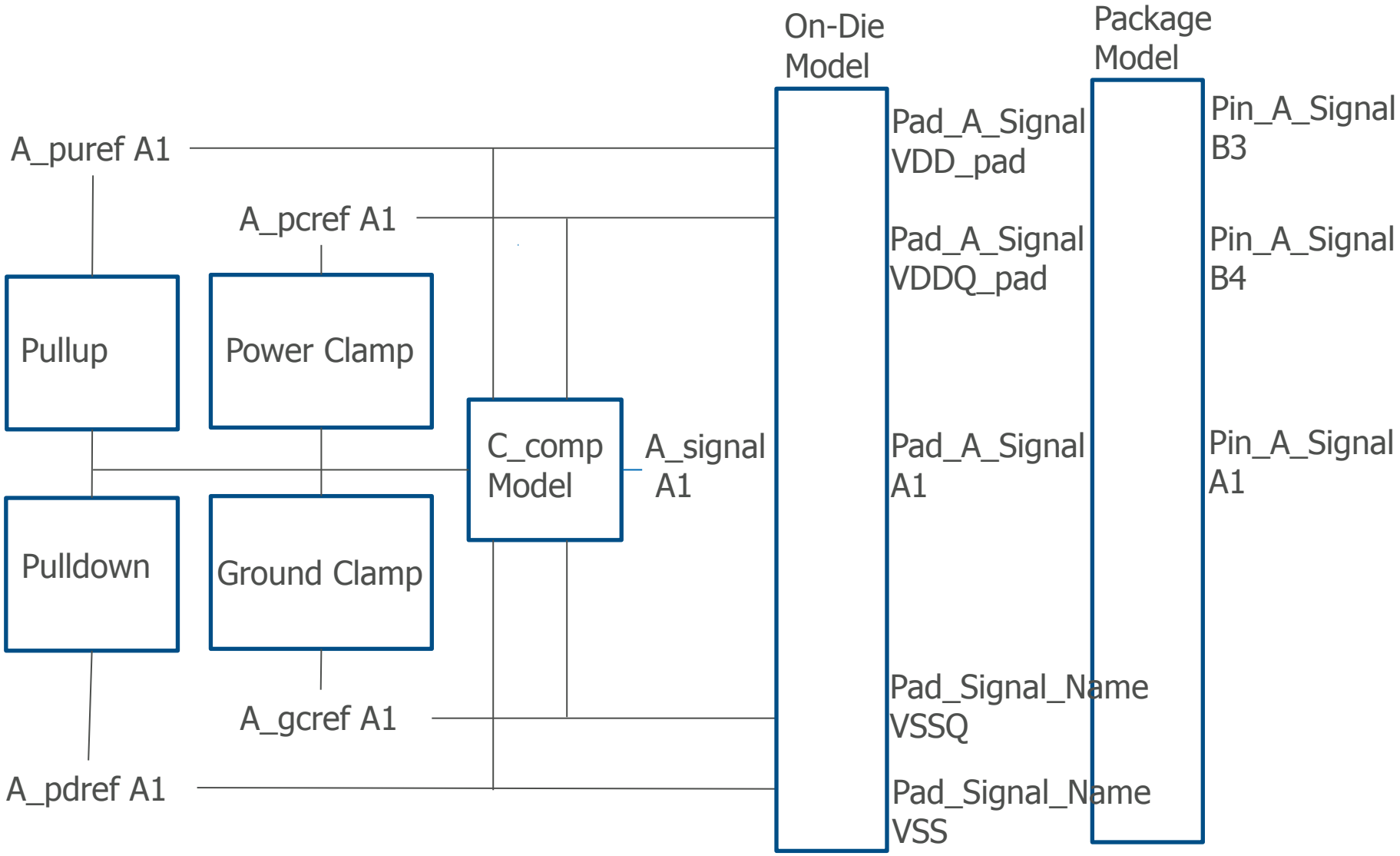
Pre and Post-layout

- Using Signal_name and “Pin mapping”
  - Terminal 1 Pin_A_Signal VDD Signal_name
  - Terminal 2 A_Signal VDD Signal_name
- Using Signal_name and “Model_name”
  - Terminal 1 Pin_A_Signal VDD Signal_name
  - Terminal 3 A_puref DQ Model_name

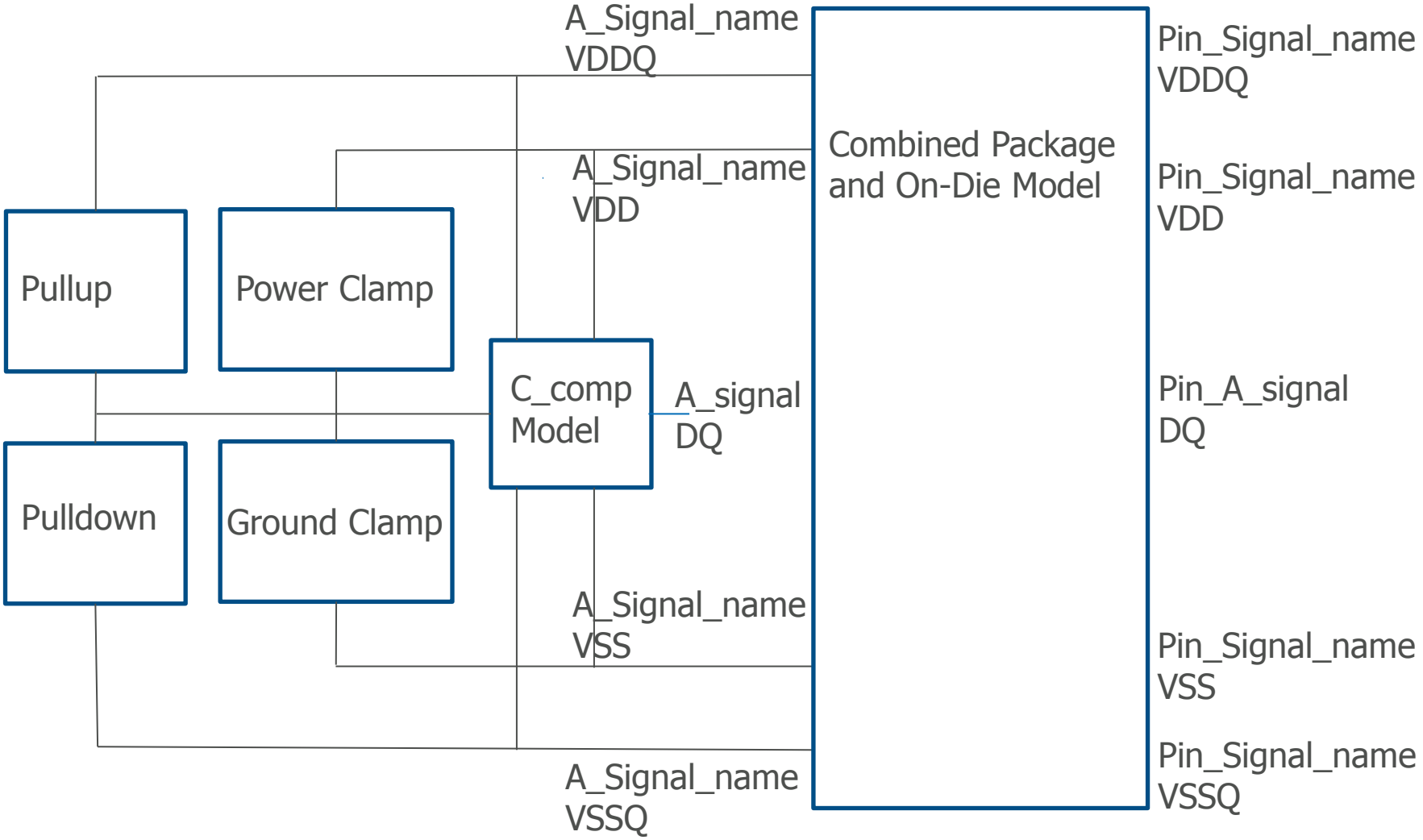
Post-Layout Package Terminals



Post-Layout Package Terminals



Pre-Layout Package Terminals



Interconnect Model Examples

[Begin Interconnect Model] A1 | Post Layout Interconnect Model
File_TS A1.s2p
Number_of_Terminals 3
Terminal 1 Pin_A_signal A1
Terminal 2 A_signal A1
Terminal 3 Pin_Signal_name VSS
[End Interconnect Model]

[Begin Interconnect Model] DQ | Pre Layout Interconnect Model
File_IBIS-ISS DQ.iss DQ
Param Length Value 0.1
Number_of_Terminals 3
Terminal 1 Pin_A_signal DQ Model_name
Terminal 2 A_signal DQ Model_name
Terminal 3 Pin_Signal_name VSS
[End Interconnect Model]

BIRD Syntax – Mapping Supply Connections

[Die Supply Pads]/[End Die Supply Pads]

- Scoped under [Component]
- Lists the supply die pad node names and corresponding Signal_names
- Used to mate package and on-die PDN networks

[Buffer Rail Mapping]

- Used with the new interconnect modeling syntax instead of [Pin Mapping]
- Defines the connections between POWER and/or GND pins and buffer and/or terminator voltage supply references using Signal_name.
- When present, then the Signal_name field (second column of [Pin] records) shall indicate that all POWER or GND pins with the same Signal_name are connected.

Corners

Interconnect model corners do not easily fit definitions of Typ, Min and Max

- Too many variables such as high/low impedance, high/low loss, min/max length
- Parameters will only be allowed a single value
- Corner cases will have to be handled through selections from multiple [Interconnect Model Selector]s

Interconnect Task Group Work in Progress

1. Interconnect Modeling for Packages
2. EMD
3. Touchstone Specification updates
4. Expansions of parameters to support statistical Design of Experiment (DOE) simulations

Are we covering your interconnect modeling needs?

- If not, let us know.
- Join the task group or send an email to ibis-interconn@freelists.org

References

Draft 19 of the Interconnect Modeling Using IBIS-ISS BIRD

- http://www.eda.org/ibis/interconnect_wip/InterconnectBIRD_19.docx

2015 DesignCon IBIS Summit presentation by Walter Katz of SiSoft "IBIS Interconnect BIRD"

- http://www.eda.org/ibis/summits/jan15/katz.pdf

Freelists email archive for IBIS Interconnect task group

- http://www.freelists.org/archive/ibis-interconn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