[Define Package Model] Proposed Extension

Randy Wolff, Micron Technology
Radek Biernacki, Keysight Technologies
Bob Ross, Teraspeed Labs

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[Define Package Model] POWER & GND Pin Connection Additions

- **Allows option for combining POWER or GND pin package models within existing IBIS specification for Power Integrity analysis**
  - **E.g., multi-pin GND plane coupled model based on one pin**
  - **Supports how some existing package models have been developed using [Component]/[Pin Mapping] keyword**
  - **Pins without model data due to merging are connected with implicit shorts**
- **Introduces new [Merged Pins] keyword for explicit connections**
  - **After [Define Package Model]/[Pin Numbers] and before [Model Data]**
  - **Works with [Component]/[Pin Mapping] keyword**

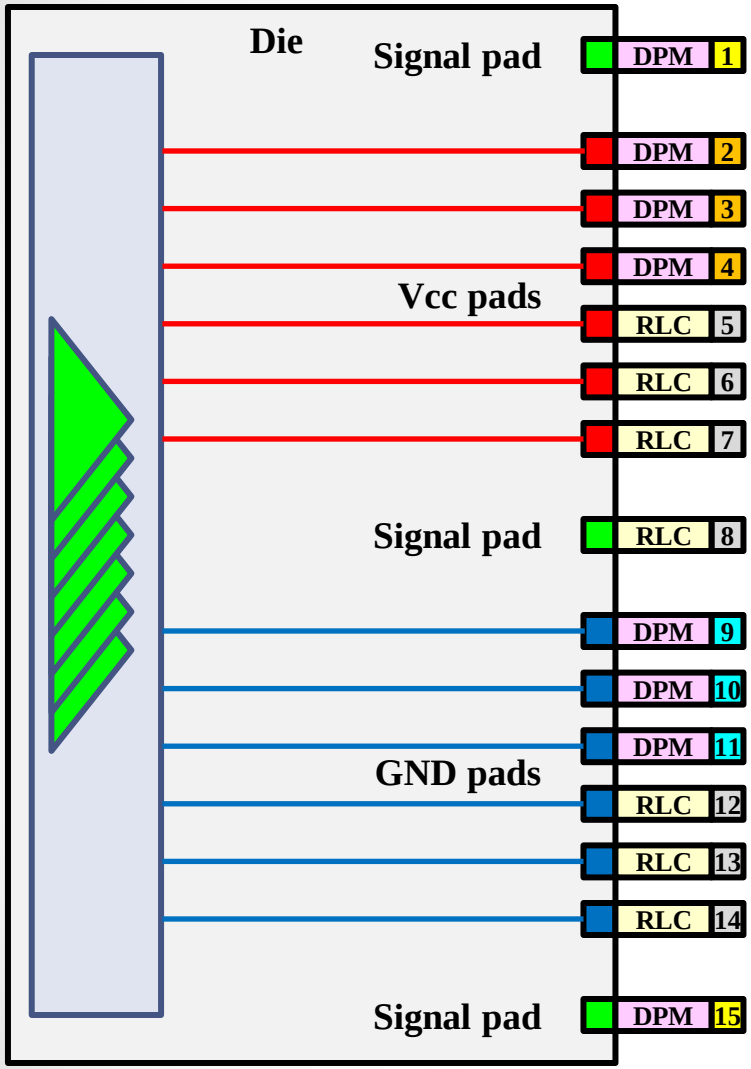
[Merged Pins] Syntax Example

```
[Manufacturer]  ACME, Inc.
[OEM]  ACME, Inc.
[Description]  FBGA Package Model for x4 Data Pins and POWER/GND
[Number of Pins]  13
[Pin Numbers]
A1 |VDD
A2 |VSSQ
A8 |VSSQ
A9 |VSS
B2 |VDDQ
B3 |DQS_c
B7 |DQ1
C2 |DQ0
C3 |DQS_t
C7 |VDD
D3 |DQ2
D7 |DQ3
D9 |VSSQ

[Merged Pins] A1
H1 M1 | Merged VDD

[Merged Pins] C7
F9 J9 N9 | Merged VDD (electrically in parallel with A1, shorted at the die)

[Merged Pins] A9
C8 E9 G1 H9 K1 K9 N1 | Merged VSS

[Merged Pins] A2
D1 | Merged VSSQ (electrically in parallel with A8 and D9, shorted at the die)

[Merged Pins] B2
B8 C1 C9 E2 E8 | Merged VDDQ
```

Legend for Pending BIRD Cases

- **Without [Merged Pins]**
  - **Implicit Short:** -------
- **DPM: [Define Package Model]/[Pin Numbers] coupled [Model Data] used**
- **RLC: Default [Pin] R_pin, L_pin, C_pin or [Package] R_pkg, L_pkg, C_pkg value under [Component]**
- **Grey Pin: Not listed in [Pin Numbers]**

[Pin Numbers], no [Pin Mapping], no [Merged Pins]



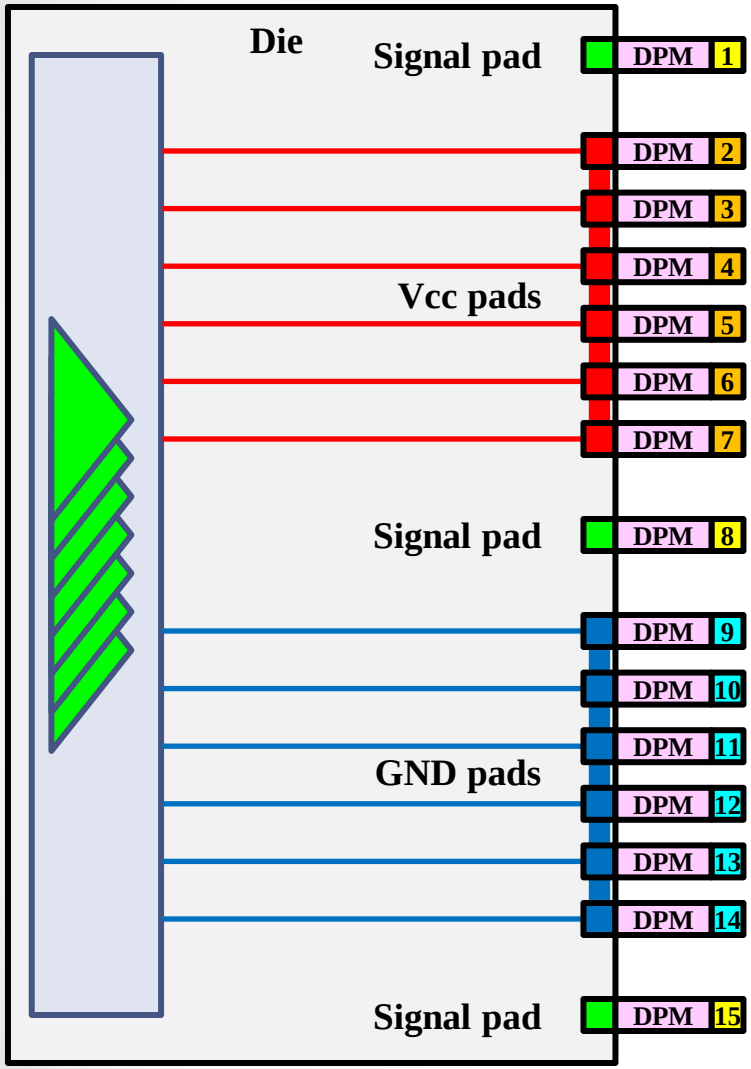
For pins listed under [Pin Numbers] (in color)

- **Package model comes from [Define Package Model]**

For pins NOT listed under [Pin Numbers] (in gray)

- **Package RLC comes from [Pin]/[Package]**

[Pin Numbers], [Pin Mapping], no [Merged Pins]

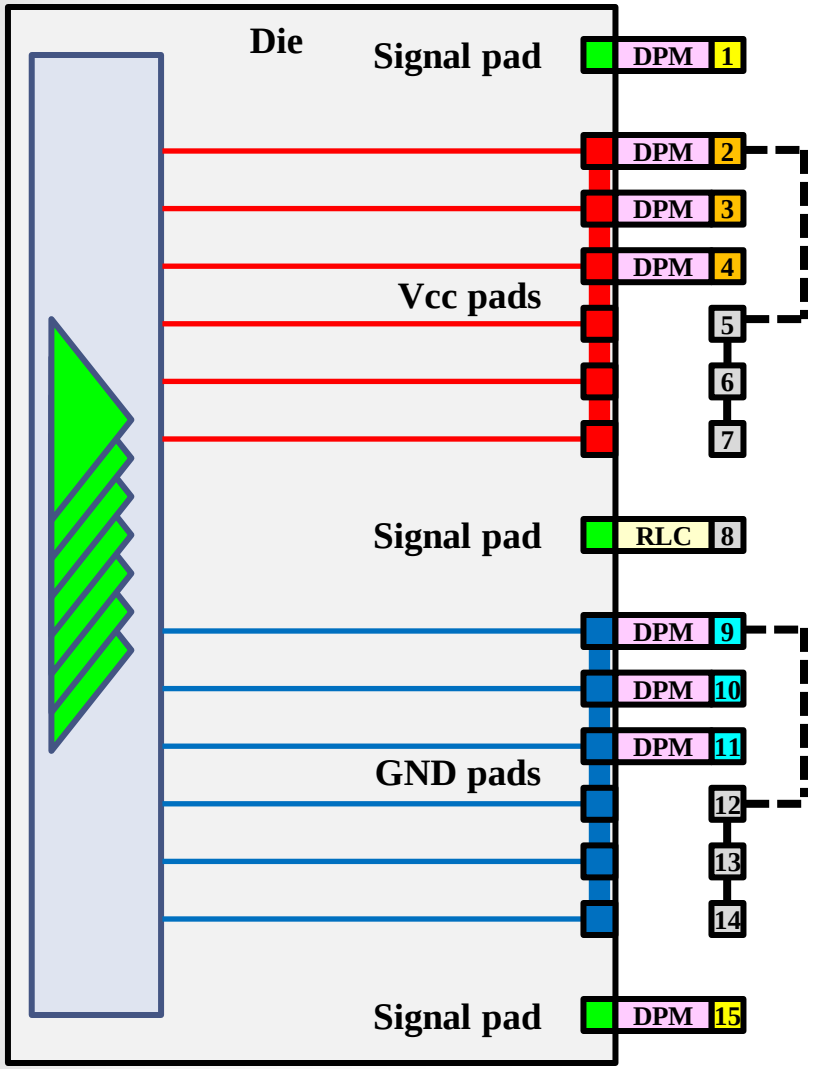


All pins are listed under [Pin Numbers]

- **Package model comes from [Define Package Model]**

Rule applies to both signal and power/ground pins

[Pin Numbers], [Pin Mapping], no [Merged Pins]



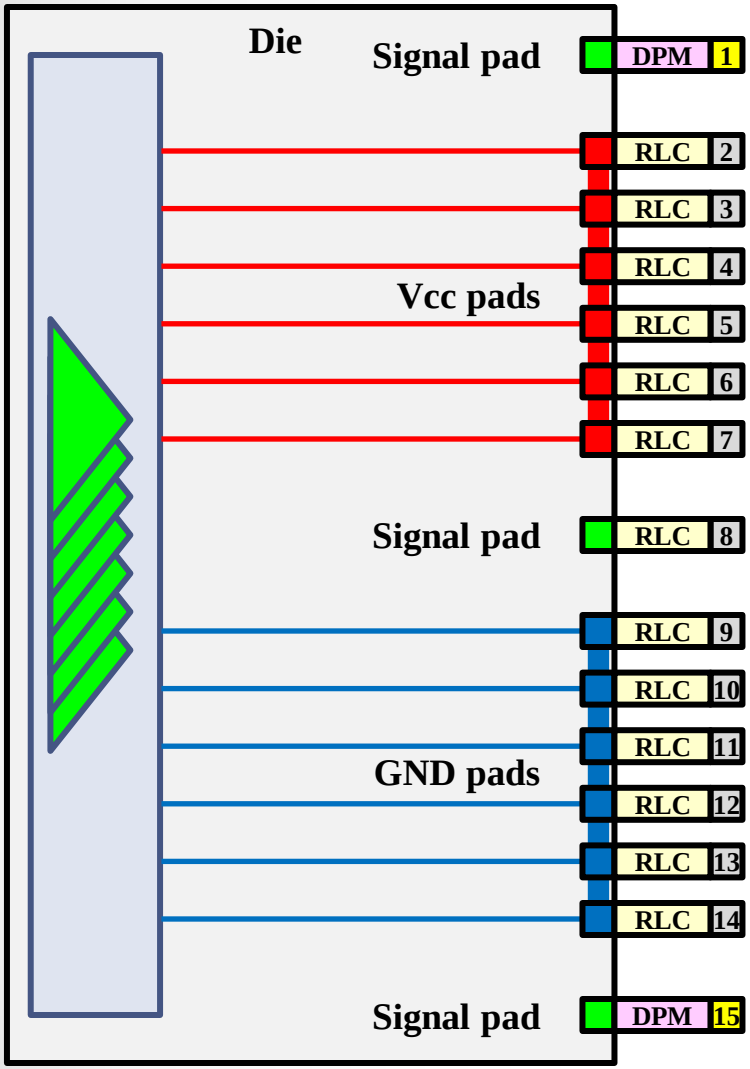
For pins listed under [Pin Numbers] (in color)

- **Package model comes from [Define Package Model]**

For pins NOT listed under [Pin Numbers] (in gray)

- **Signal pins: package RLC comes from [Pin]/[Package]**
- **Power/ground pins: NO package RLC should be used**
- **Implicit connection to first pin listed in [Pin Numbers]**
- **EDA tools now expected to support this option**
- **EDA tools may provide interface to select where unlisted pins are attached to pins listed under [Pin Numbers]**

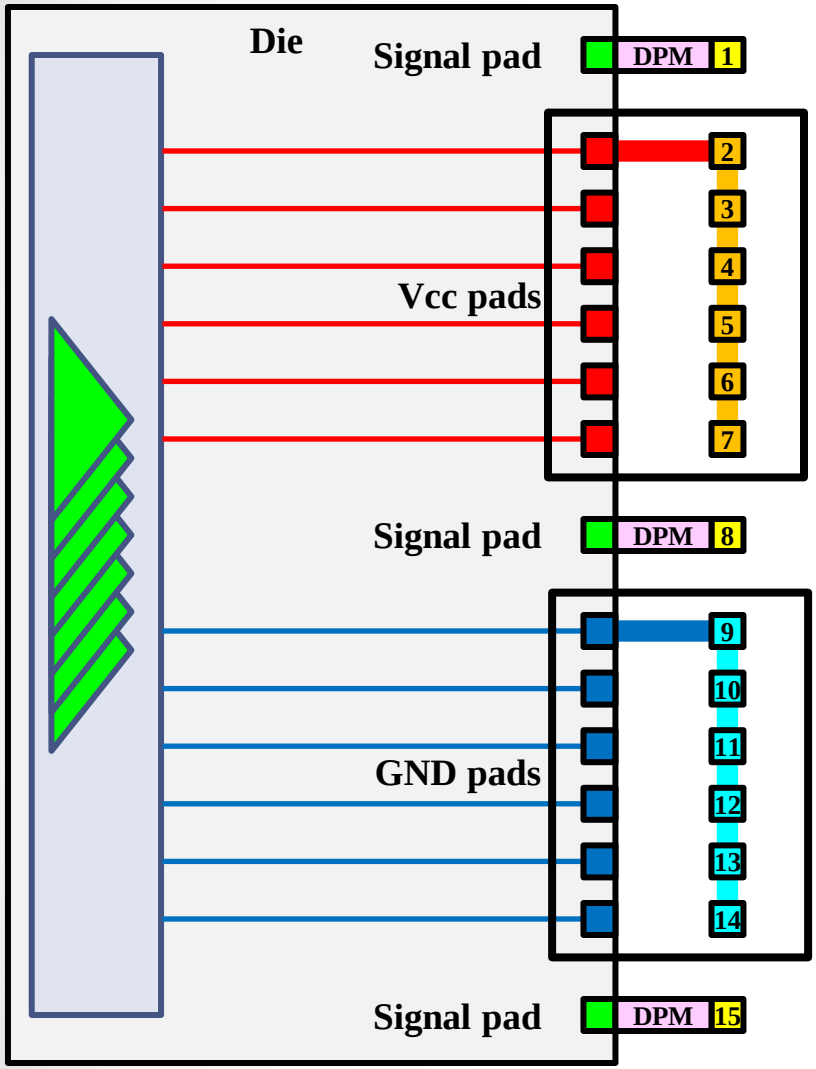
[Pin Numbers], [Pin Mapping], no [Merged Pins]



No bussed pins are listed under [Pin Numbers] (in gray)

- **Package RLC should be used**

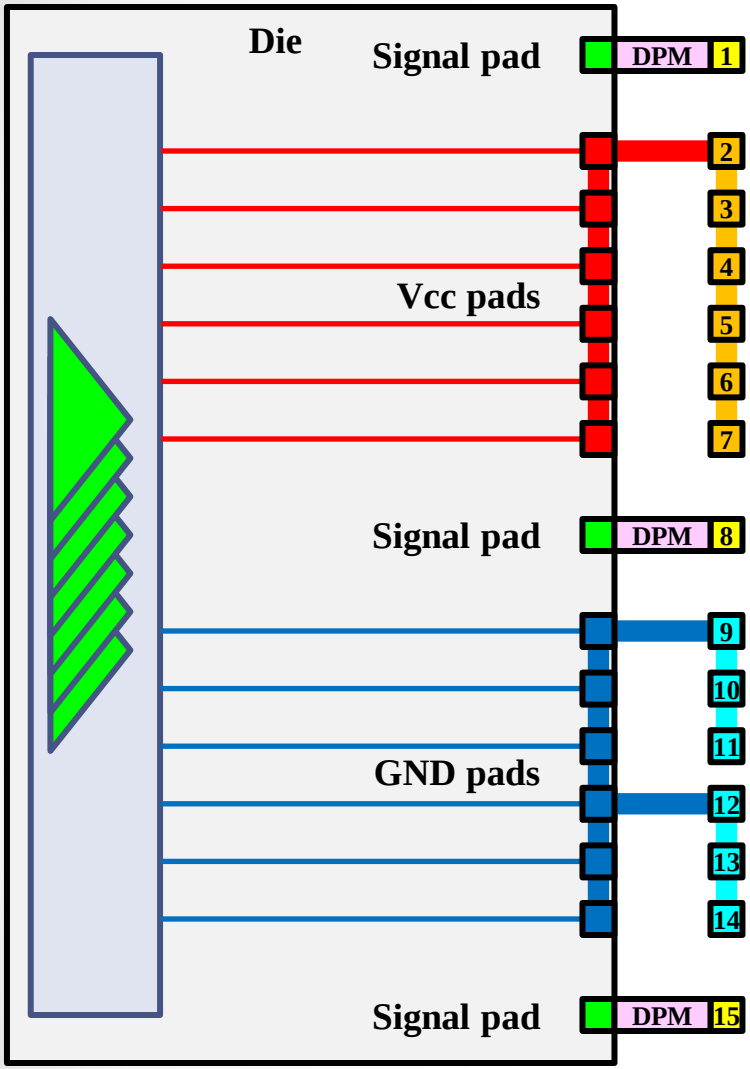
[Pin Numbers], no [Pin Mapping], with [Merged Pins]



Illegal

[Pin Mapping] bus is required to align with [Merged Pins] connections

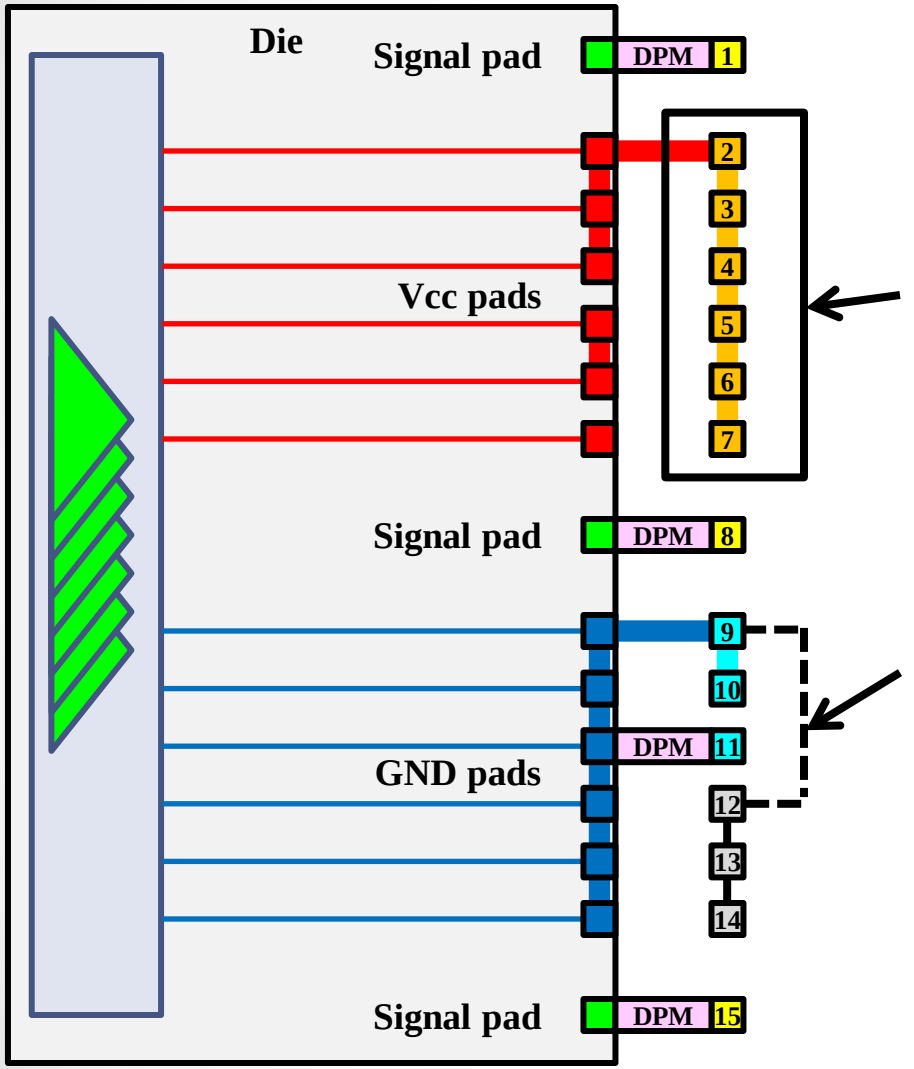
[Pin Numbers], [Pin Mapping], with [Merged Pins]



All pins are listed under [Pin Numbers]

- **Package model comes from [Define Package Model]**
- **[Merged Pins] keyword defines connection to [Pin Numbers] entries**
- **Pins 3-7, 10-11, and 13-14 are NOT in [Pin Numbers] list, but in [Merged Pins] list**
- **[Pin Mapping] busses can be associated with several [Merged Pins] groups**

[Pin Numbers], [Pin Mapping], with [Merged Pins]

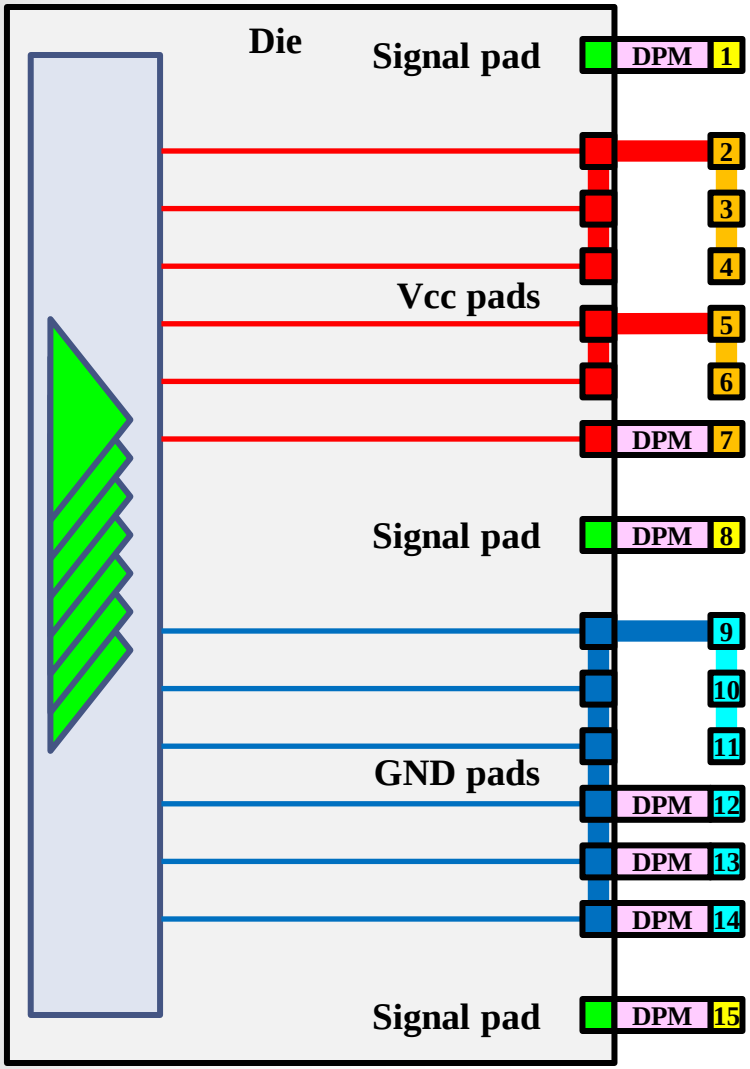


Illegal

Pins outside of a [Pin Mapping] bus not allowed in a [Merged Pins] group (pins 5, 6, and 7)

Unlisted pins for same [Pin Mapping] bus are implicitly merged, by default, to the first pin listed under [Pin Numbers]

[Pin Numbers], [Pin Mapping], with [Merged Pins]



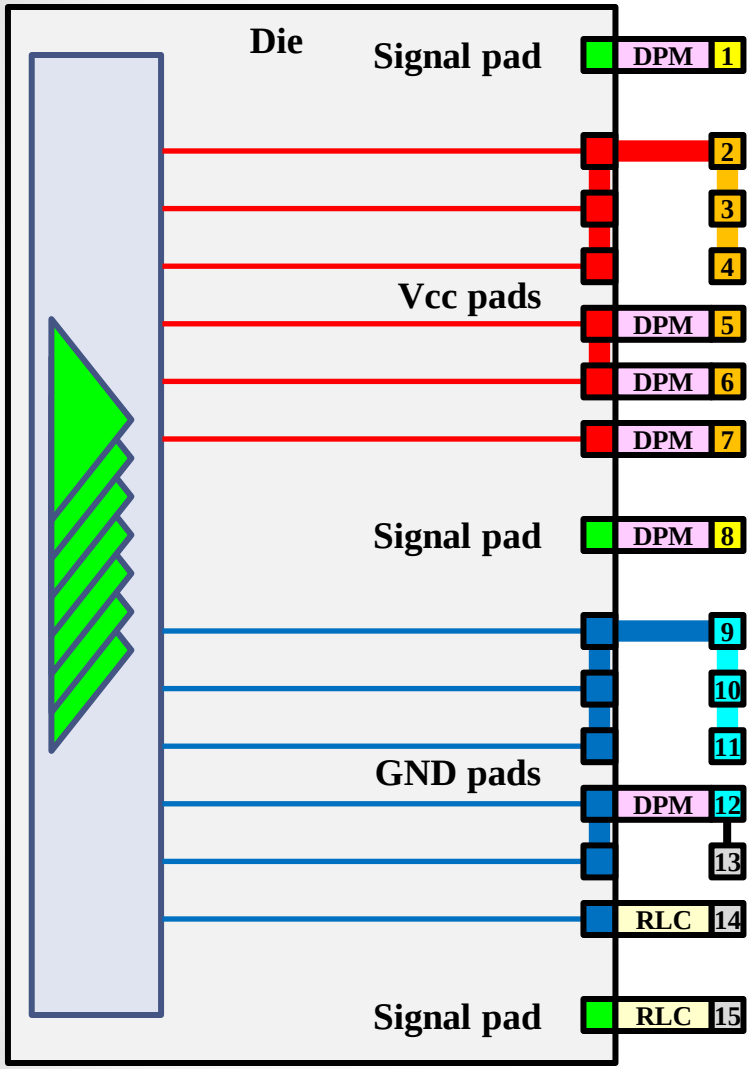
Legal Cases

[Pin Mapping] busses and [Merged Pins] listings are aligned

Pin 7 is on a separate [Pin Mapping] bus

Pins 12-14 listed under [Pin Numbers] and these pins should use the [Define Package Model] data

[Pin Numbers], [Pin Mapping], with [Merged Pins]



Legal Cases

[Merged Pins] used for pins 3, 4 to 2 and for pins 10, 11 to 9

For pins NOT listed under [Pin Numbers] (in gray)

- **Pin 13: NO package RLC should be used**
- **Pin 13 is on same [Pin Mapping] bus as pin 12 and is implicitly merged to pin 12**

Unlisted pin 14 is on separate bus and connected by RLC model (as is the signal pin 15)

Conclusion

- **BIRD176 being prepared for Version 6.1**
- **POWER/GND connection option available within existing IBIS for unlisted pins in [Pin Numbers]**
- **New [Merged Pins] keyword gives explicit connections**
- **Questions, comments?**