Physics and Modeling of Vias in Printed Circuit Boards

Jan Birger Preibisch & Christian Schuster

Institute of Electromagnetic Theory
Hamburg University of Technology (TUHH)

18th European IBIS Summit Meeting

May 13th, 2015 Berlin, Germay

TUHH
Technische Universität Hamburg-Harburg

Outline

(1) The Problem with Vias

(2) Physics of Vias

(3) Models for Vias

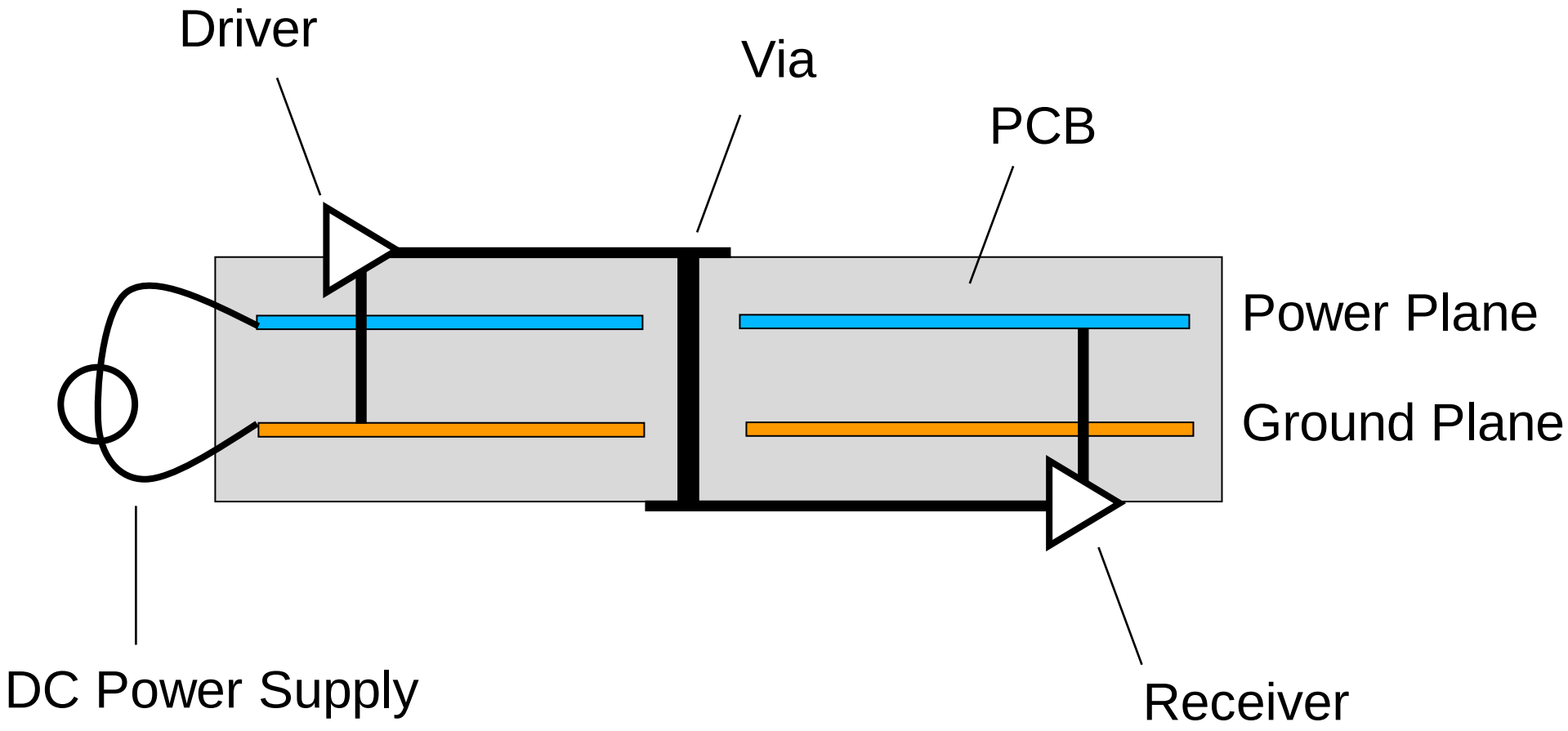
(4) Application Example

(5) Conclusions

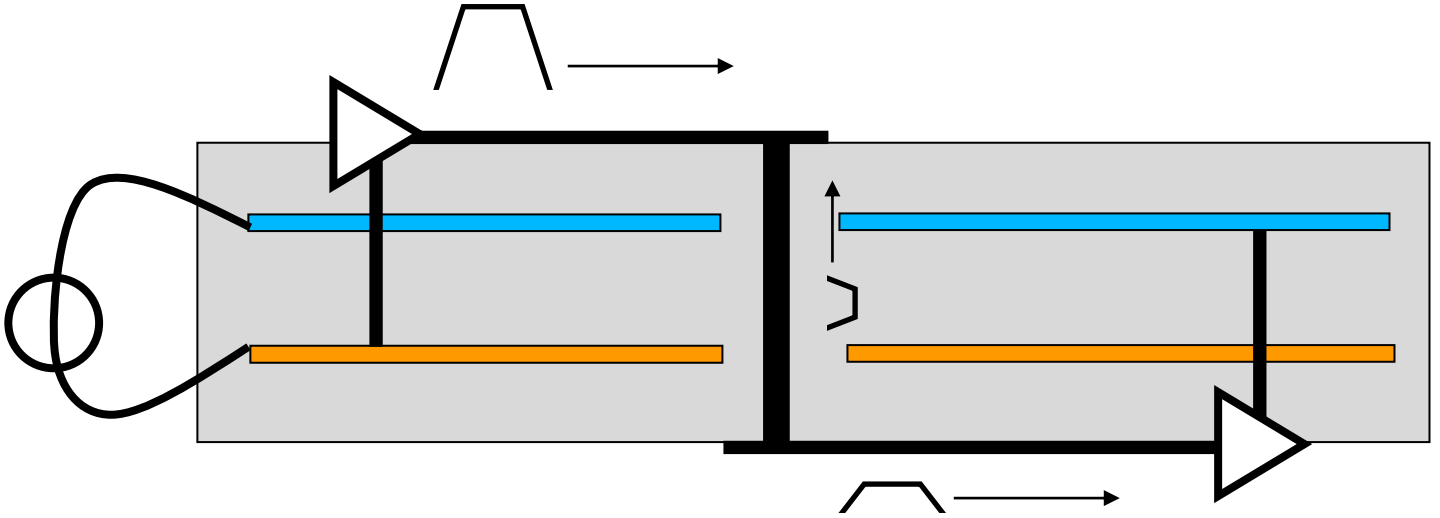
(2)

The Problem with Vias

The Problem with Vias …



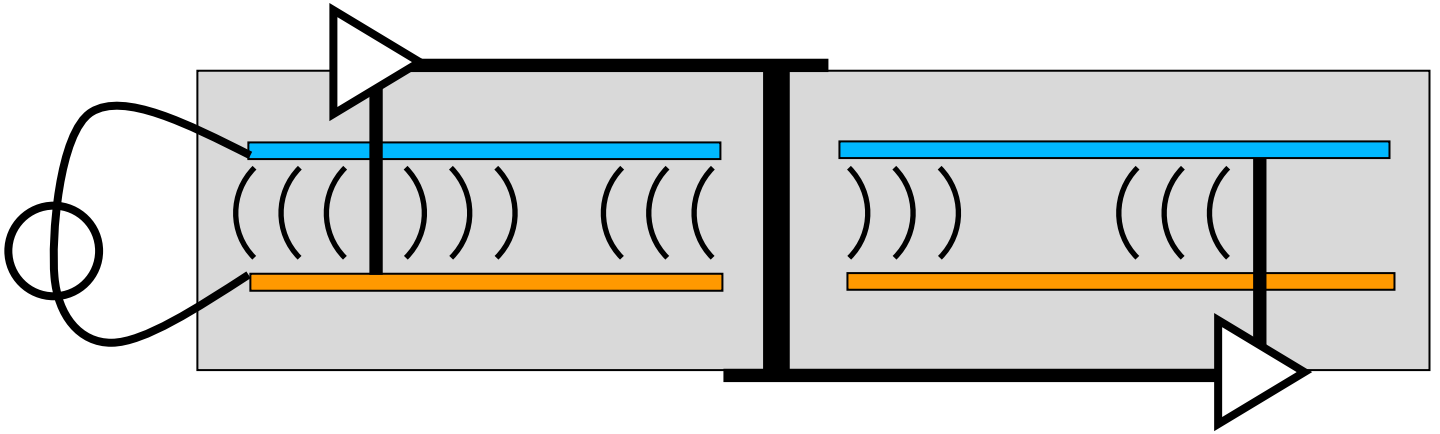
The Problem with Vias …



Signal Integrity Problems:

Attenuation, Reflection, Dispersion, Interference, Crosstalk

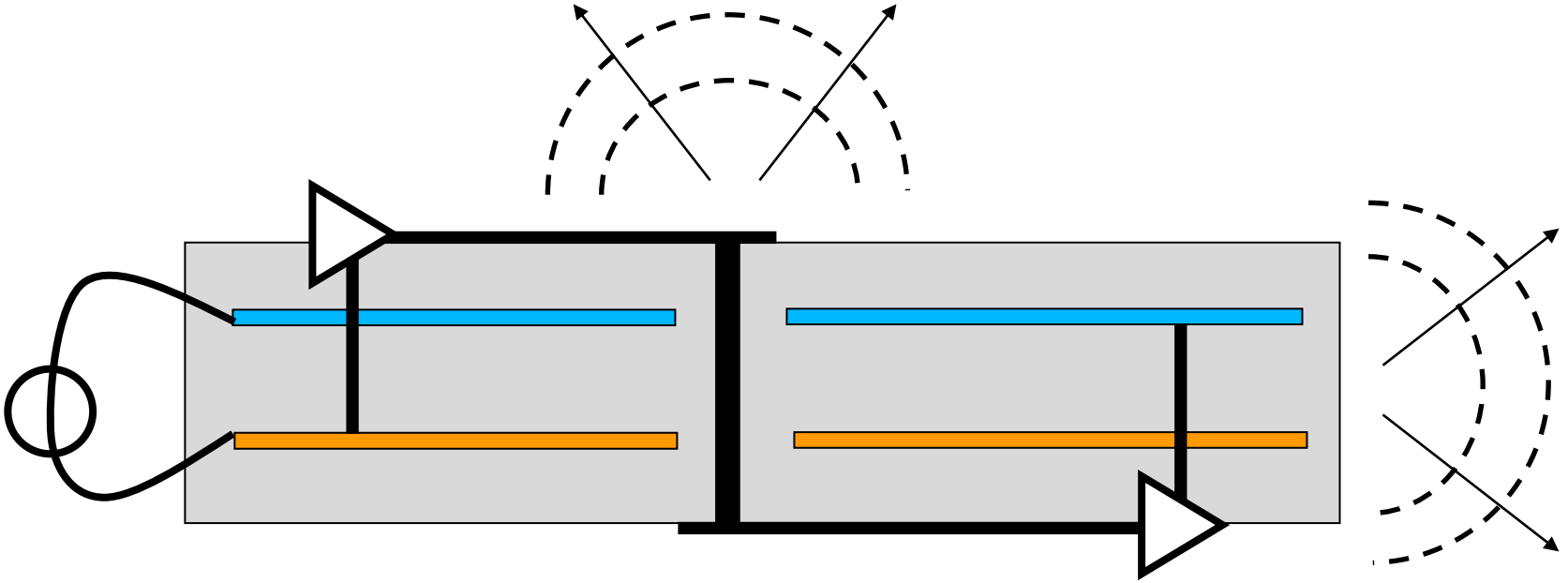
The Problem with Vias …



Power Integrity Problems:

Voltage Drop, Switching Noise, Crosstalk

The Problem with Vias …



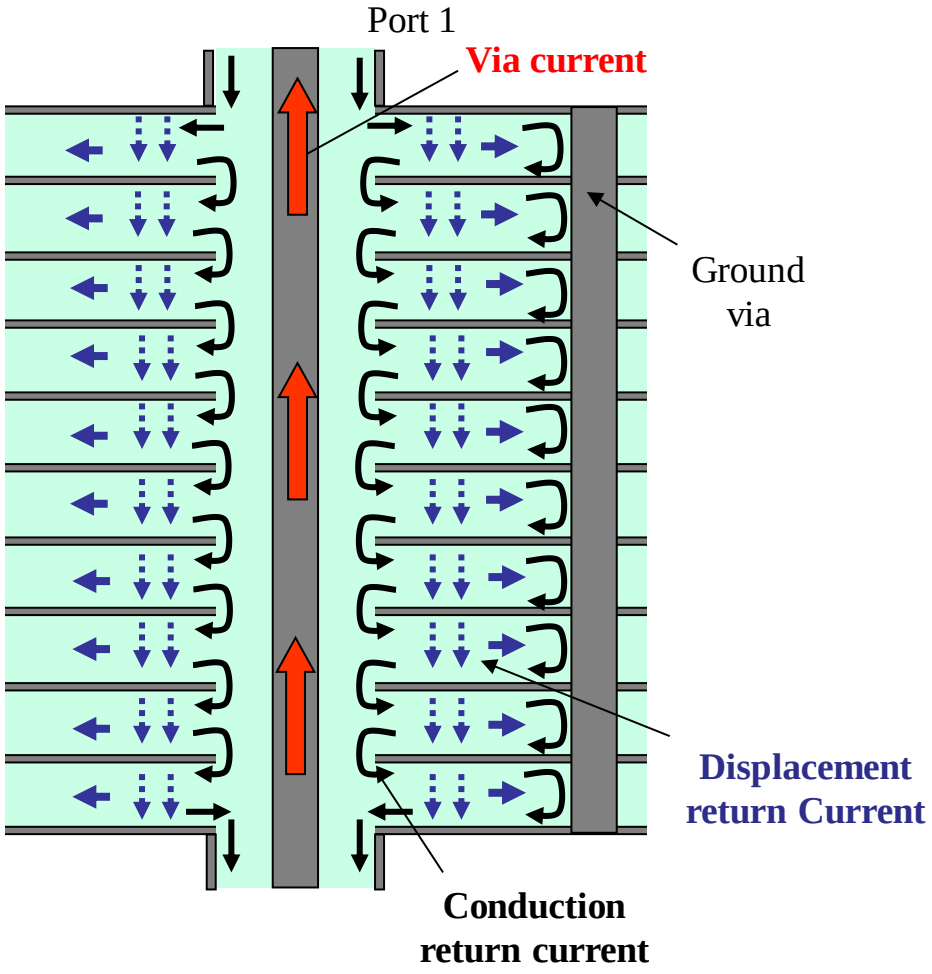
Electromagnetic Compatibility Problems:

Near Field Coupling, Radiated Emissions

(2)

Physics of Vias

Currents on Via Structures



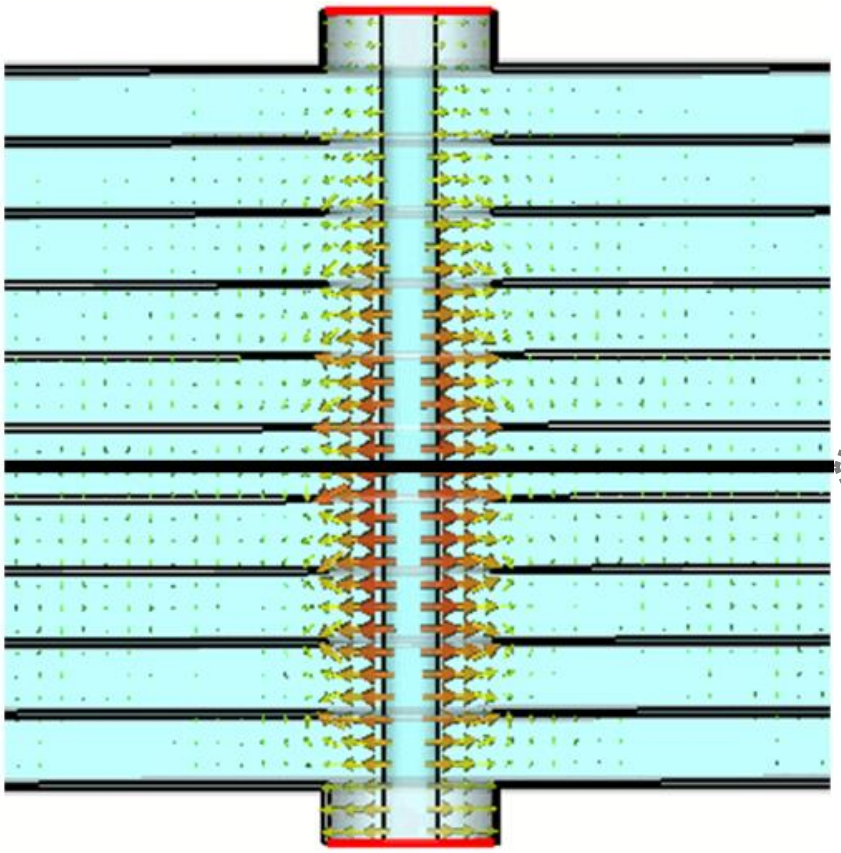
Via (Signal) Current

Conduction Return Current

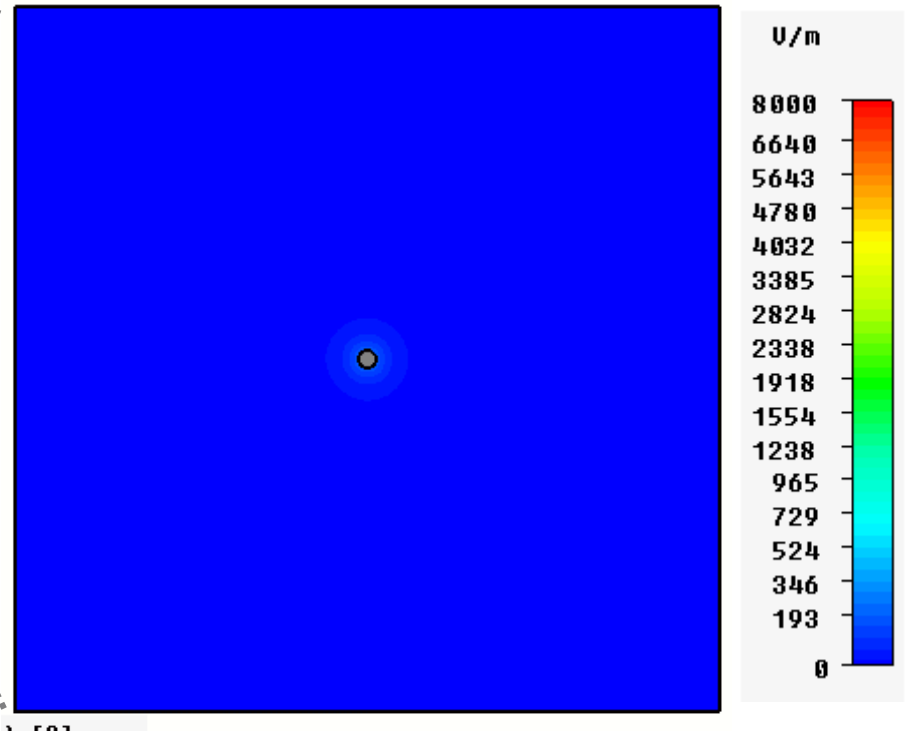
Displacement Return Current

Figures by R. Rimolo-Donadio

Electric Fields Between Plates



Top View, 5th Cavity

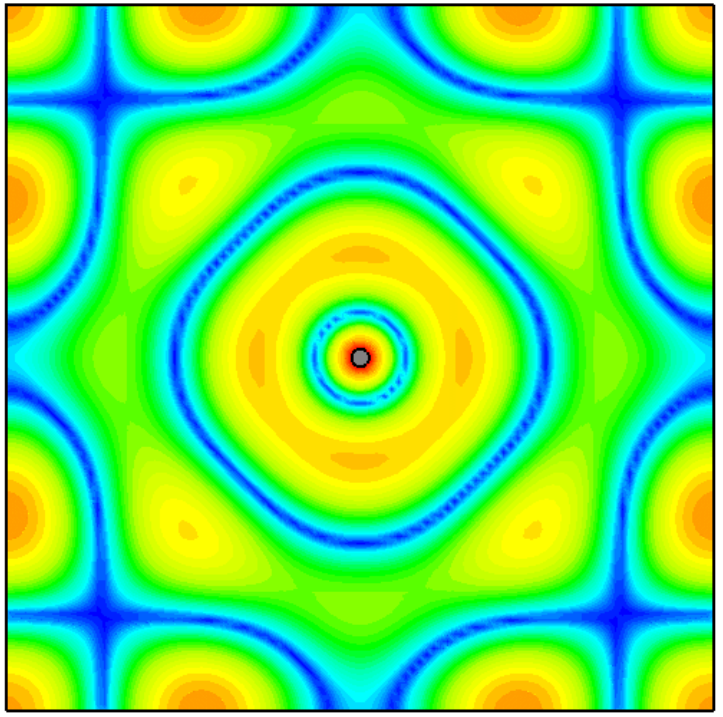


Excitation: Gaussian pulse (f_{max} = 40 GHz)

Figures by R. Rimolo-Donadio

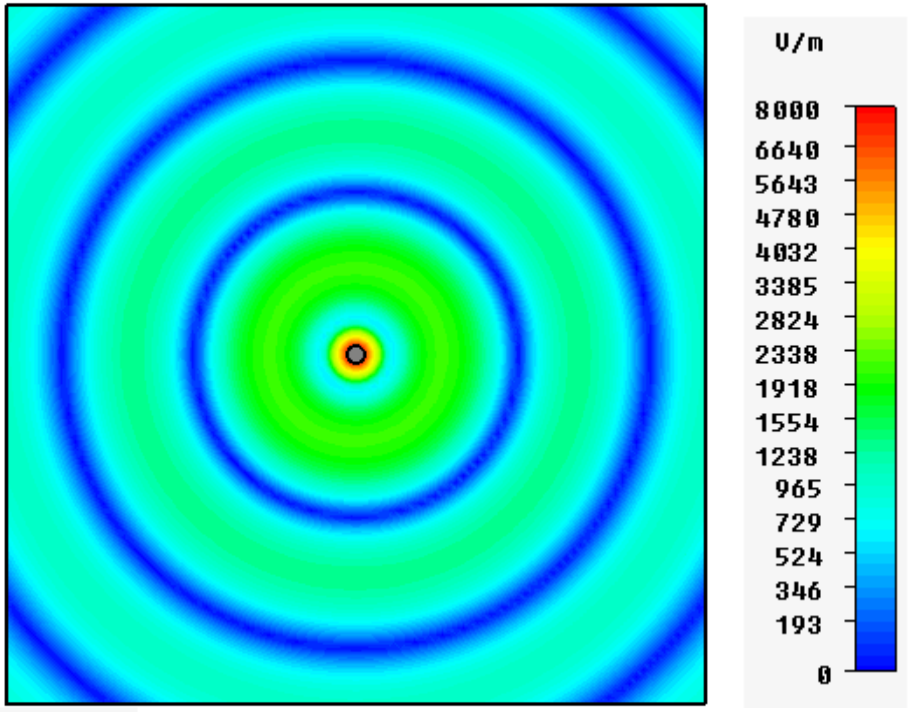
Electric Fields Between Plates

Top View, 5th cavity



Finite Planes

Top View, 5th Cavity

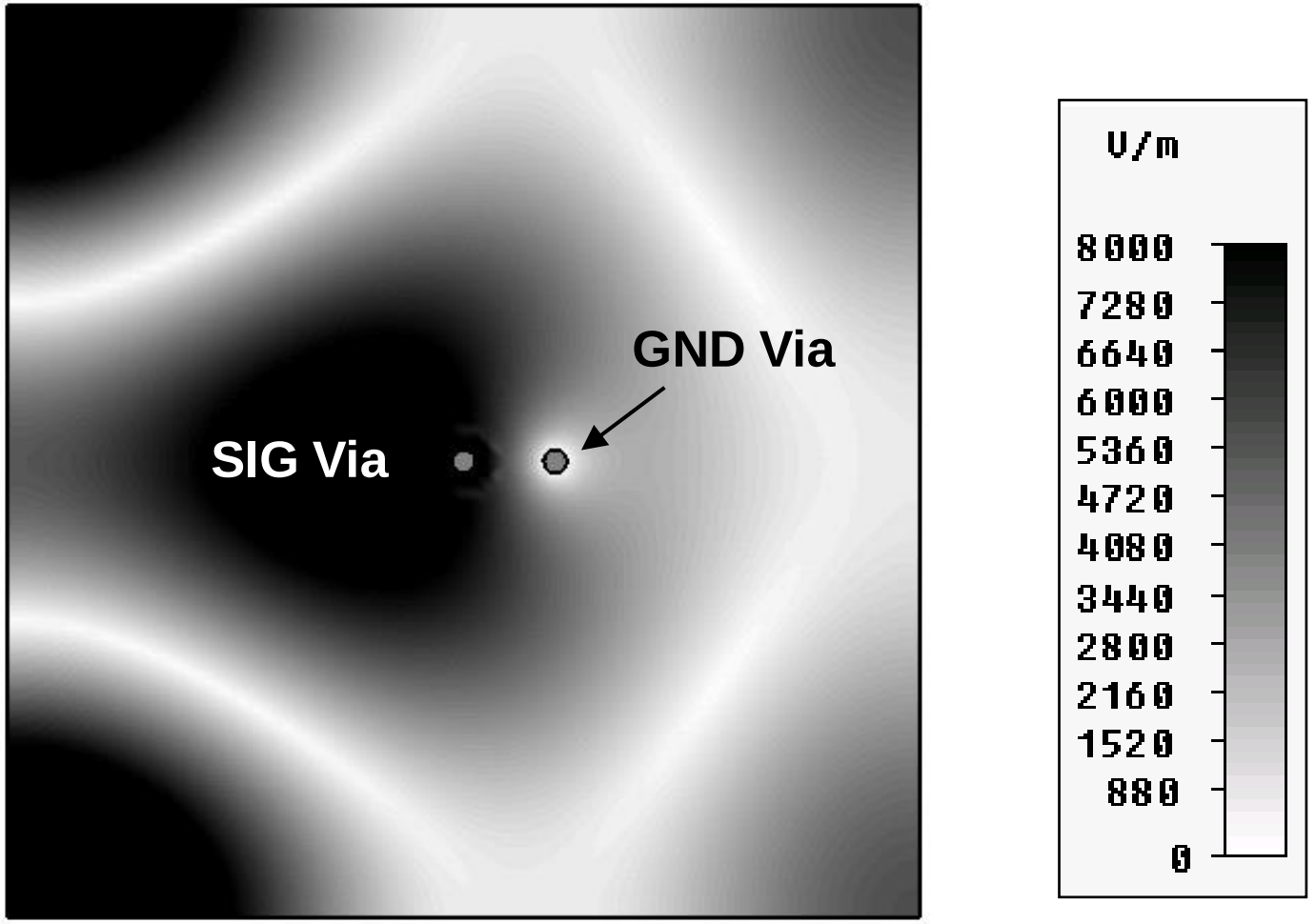


Infinite Planes

Figures by R. Rimolo-Donadio

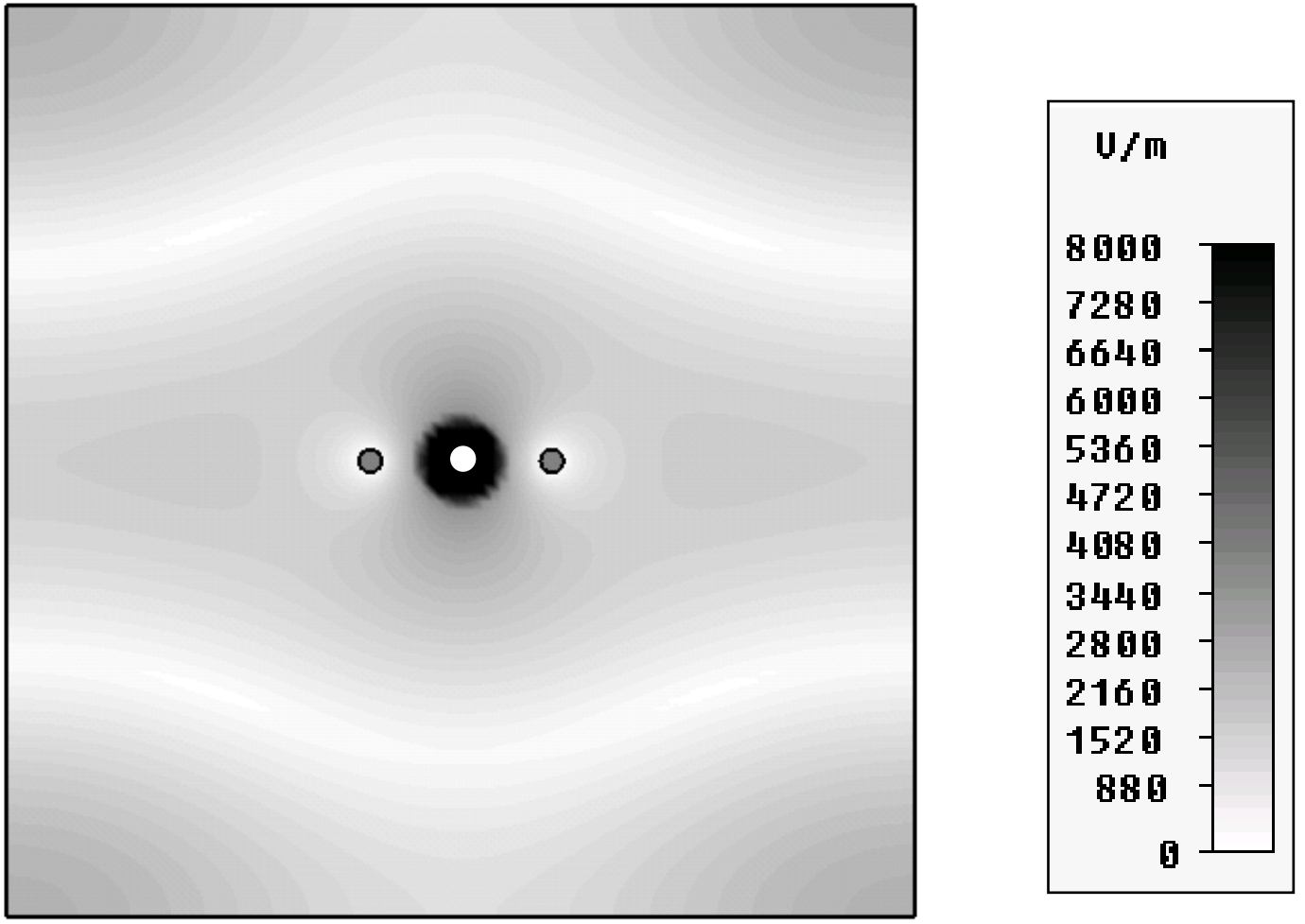
Influence of Ground Vias

1 Ground Via:



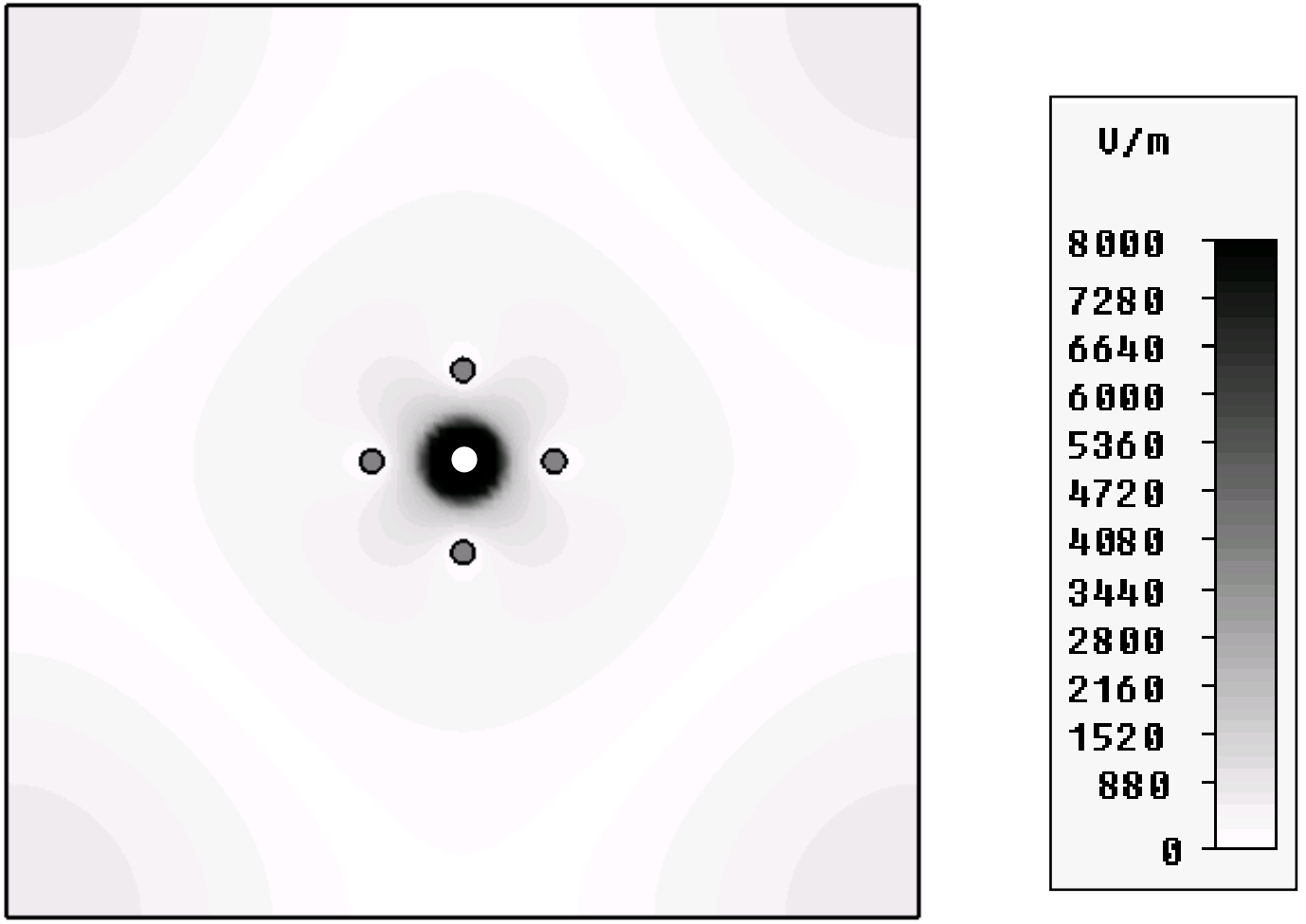
Influence of Ground Vias

2 Ground Vias:



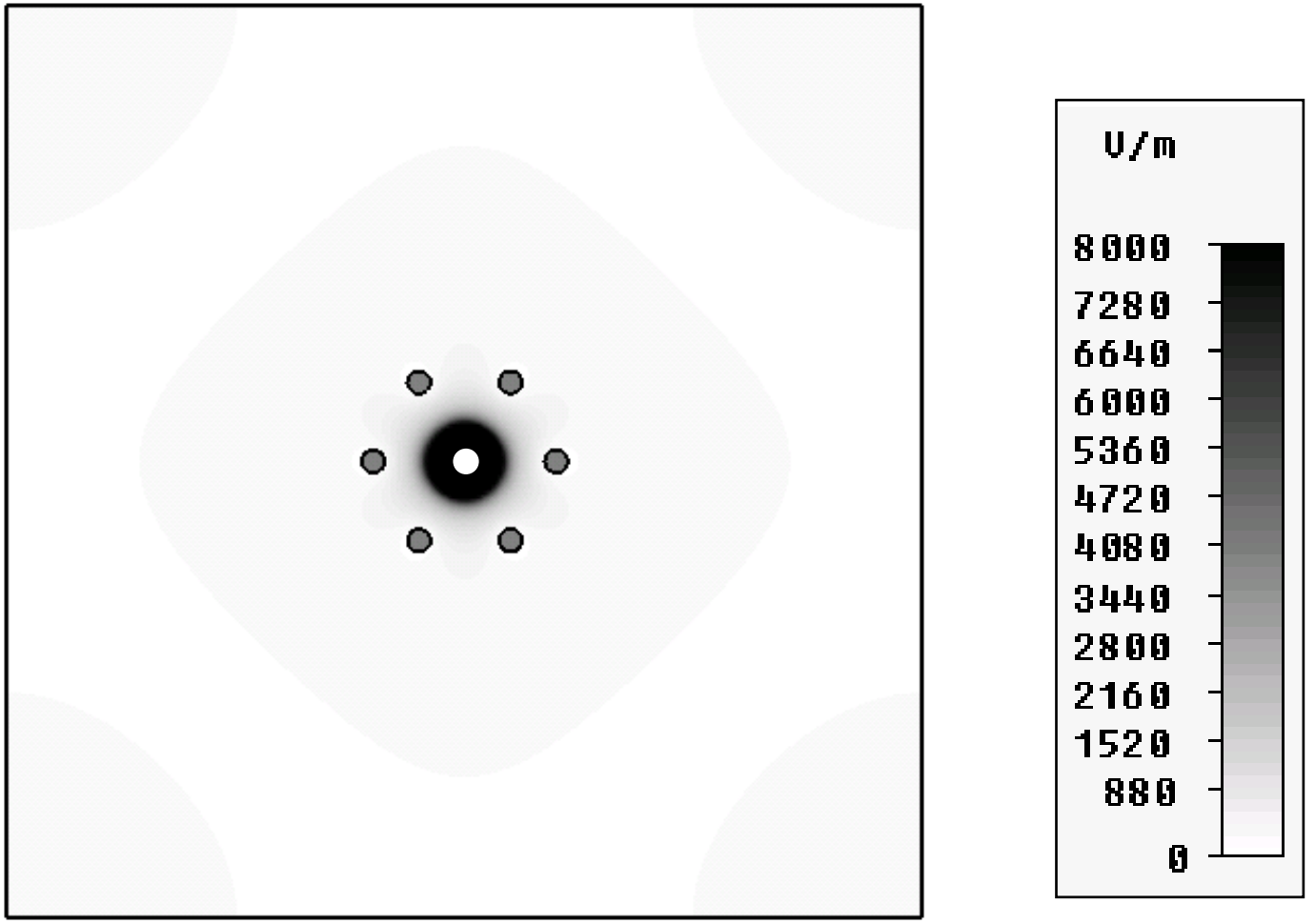
Influence of Ground Vias

4 Ground Vias:

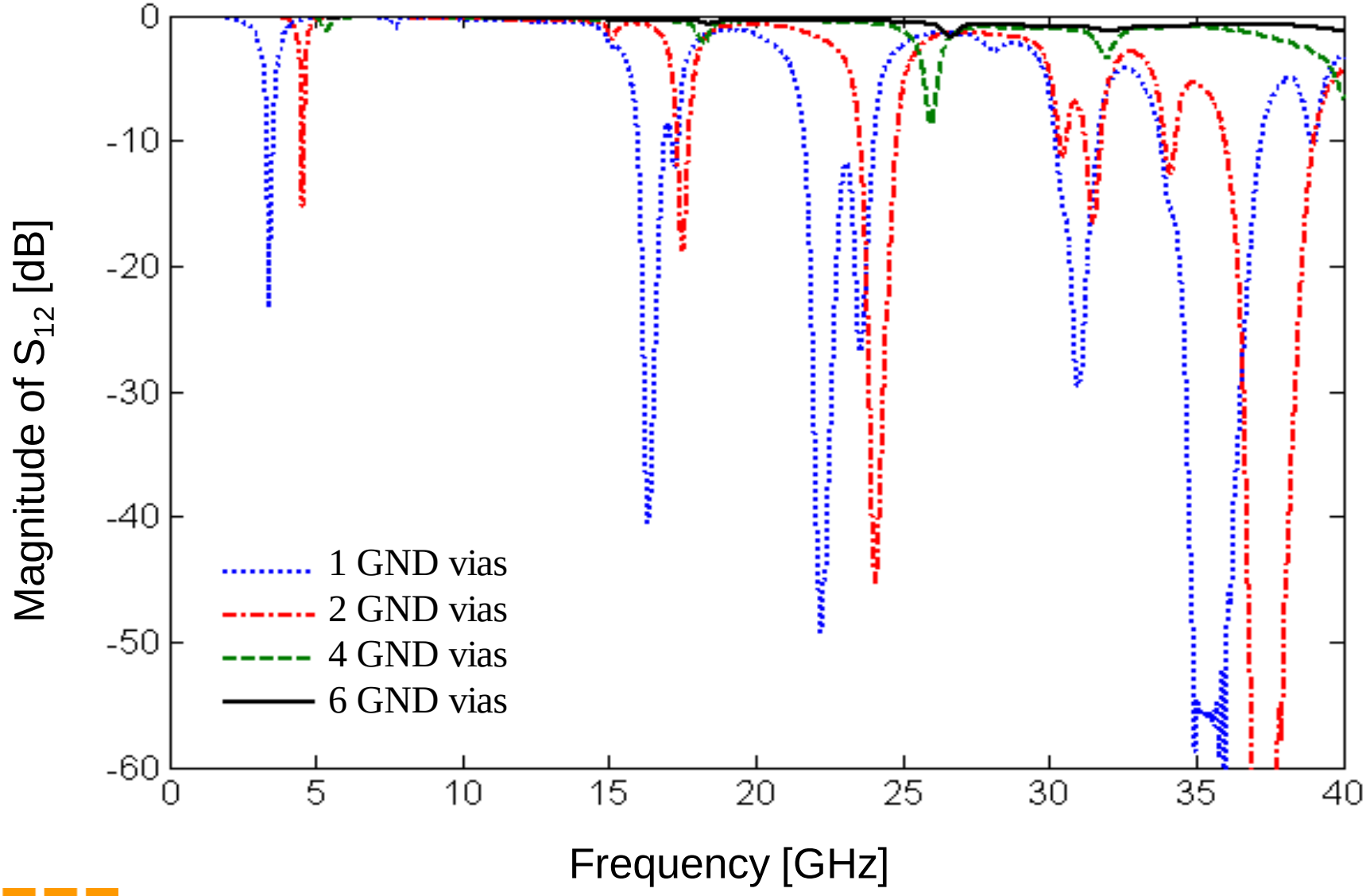


Influence of Ground Vias

6 Ground Vias:

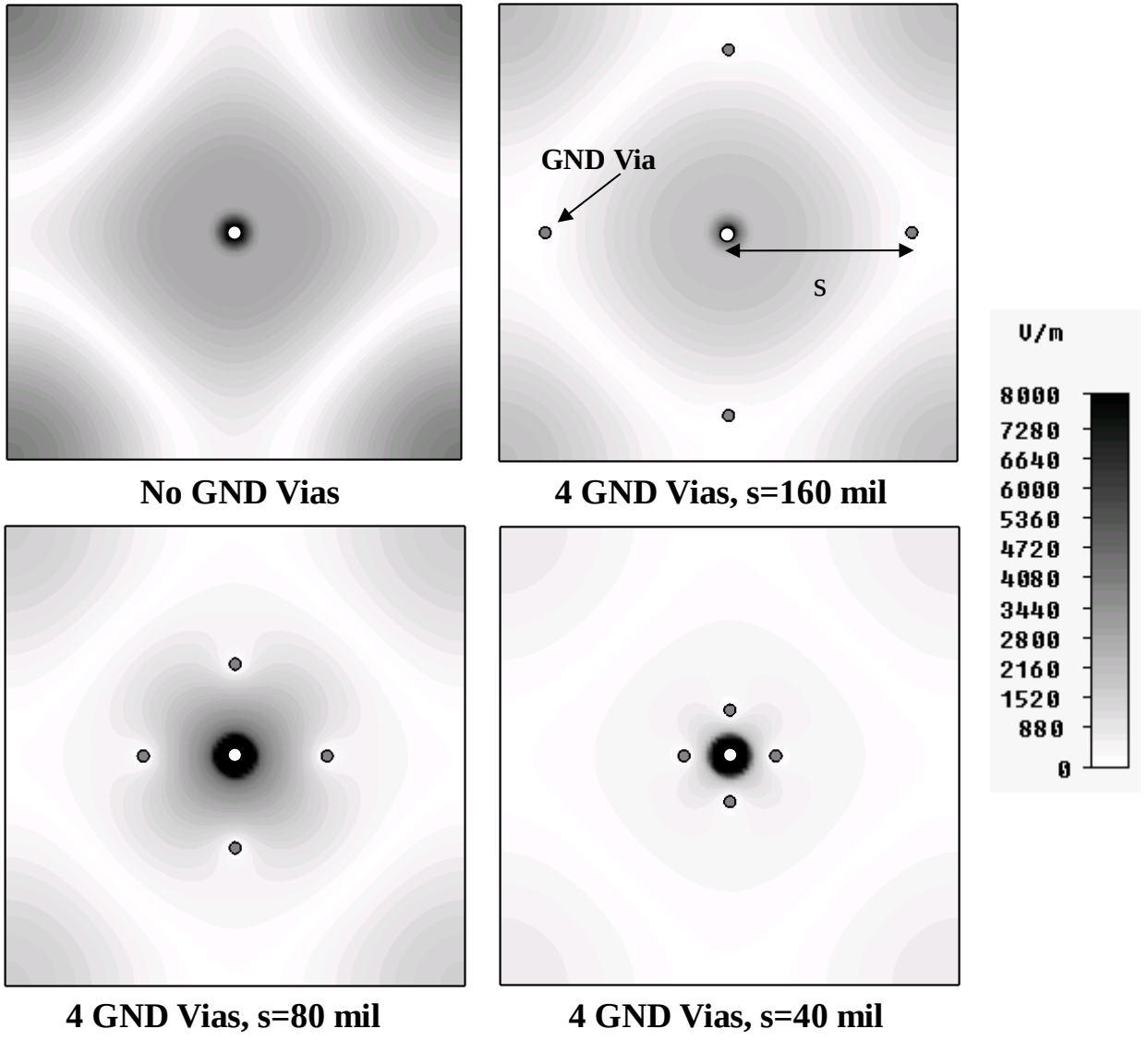


Influence of Ground Vias



Influence of Ground Vias

Effect of location of ground vias:



No GND Vias

4 GND Vias, s=160 mil

4 GND Vias, s=80 mil

4 GND Vias, s=40 mil

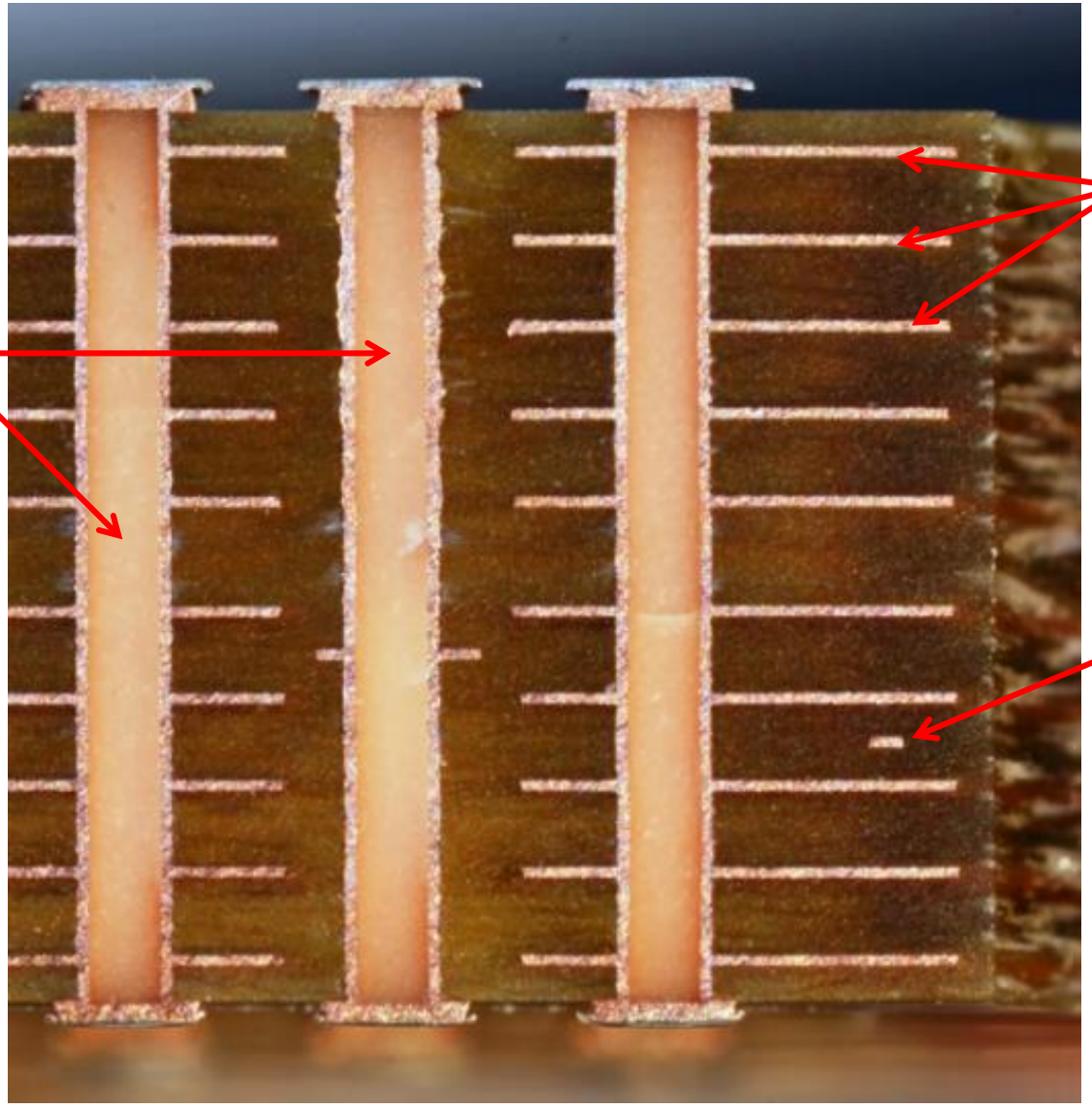
Physics of Vias – Summary

- ➔ Vias „live“ within a parallel plate environment
- ➔ Shape and size of the plates have an impact
- ➔ Ground vias can be used to control that impact
- ➔ Return currents are a mixture of displacement and conduction currents

(3)

Models for Vias

PCB Teardown



Signal and Power Vias

Via Models

Power Planes

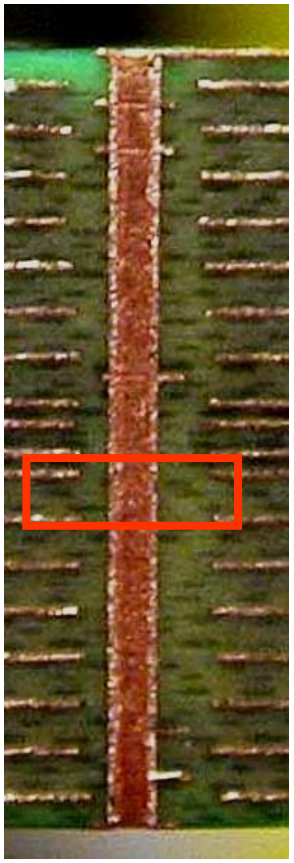
Planar Circuit Models

Stripline

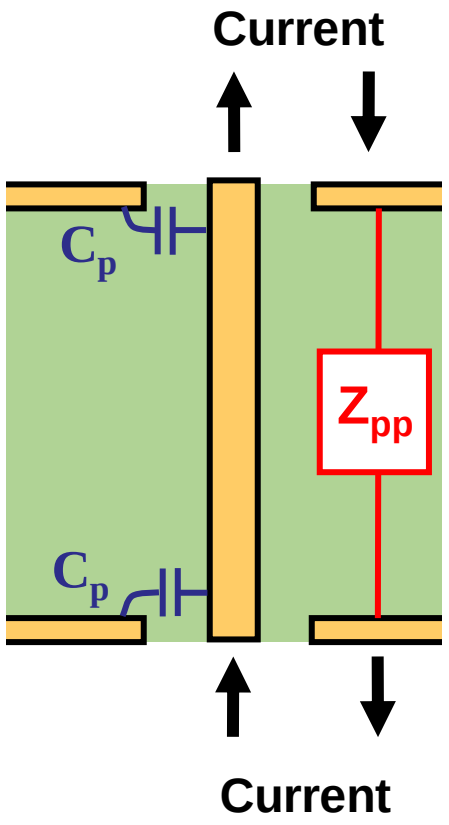
Transmission Line Models

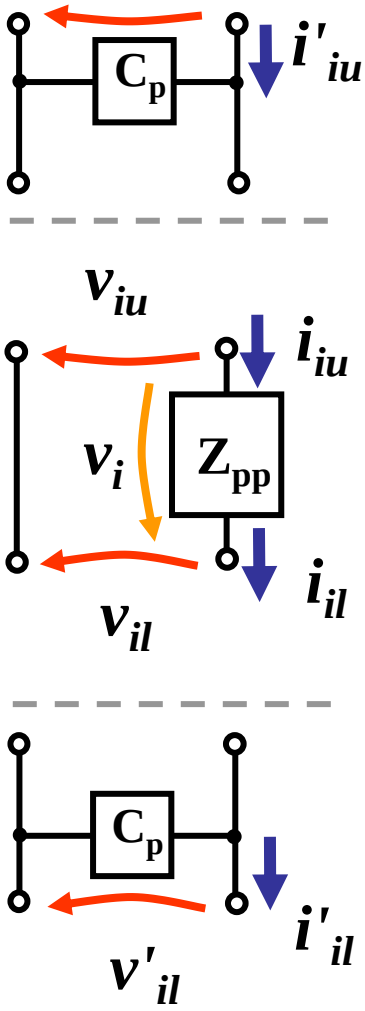
Picture courtesy IBM Yorktown (Y. Kwark)

A “Physics-Based” Model for Vias



Via Cross Section





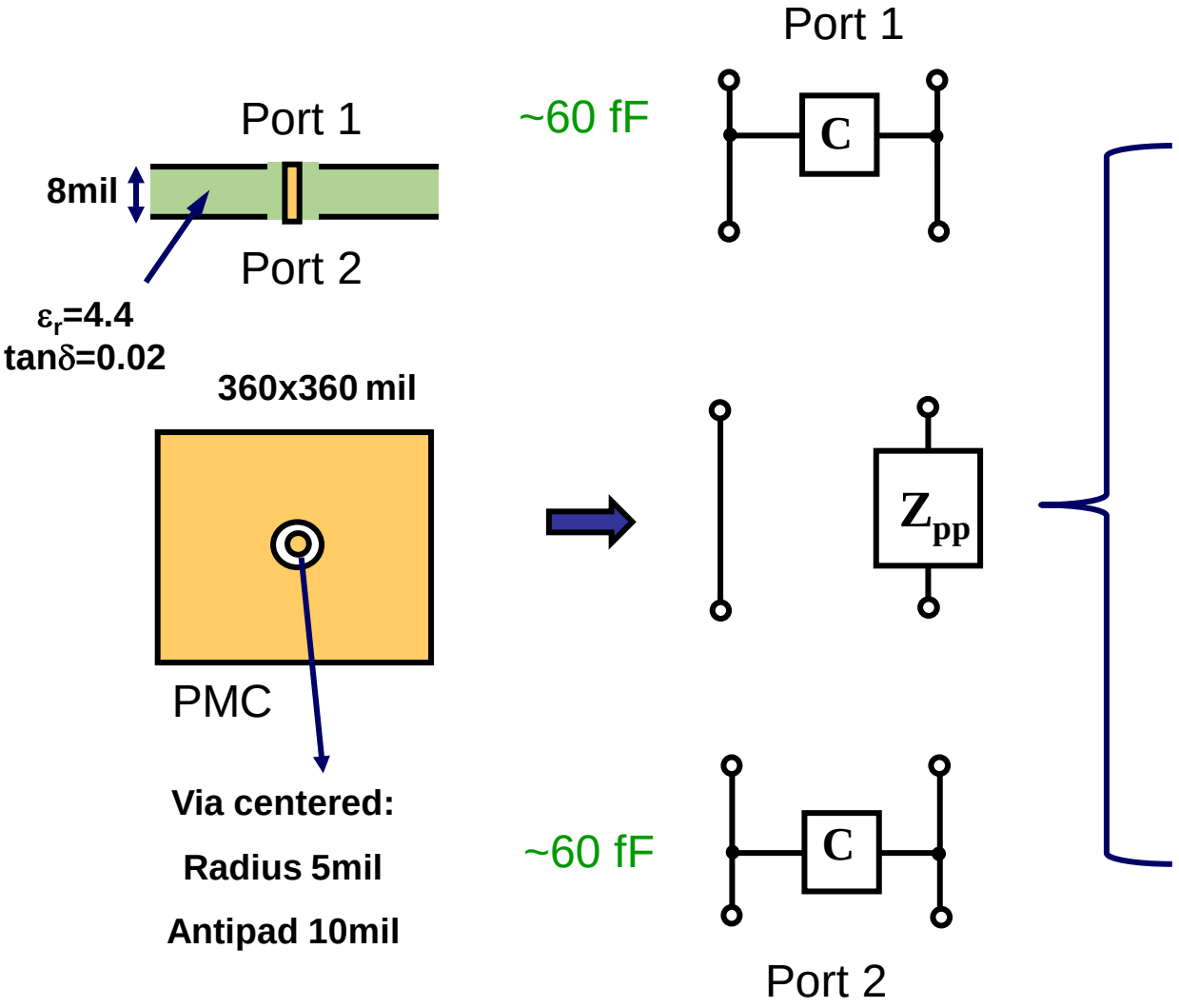
$$\begin{bmatrix} v'_{i_u} \\ i'_{i_u} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 1/Z_{p_u} & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{i_u} \\ i_{i_u} \end{bmatrix}$$

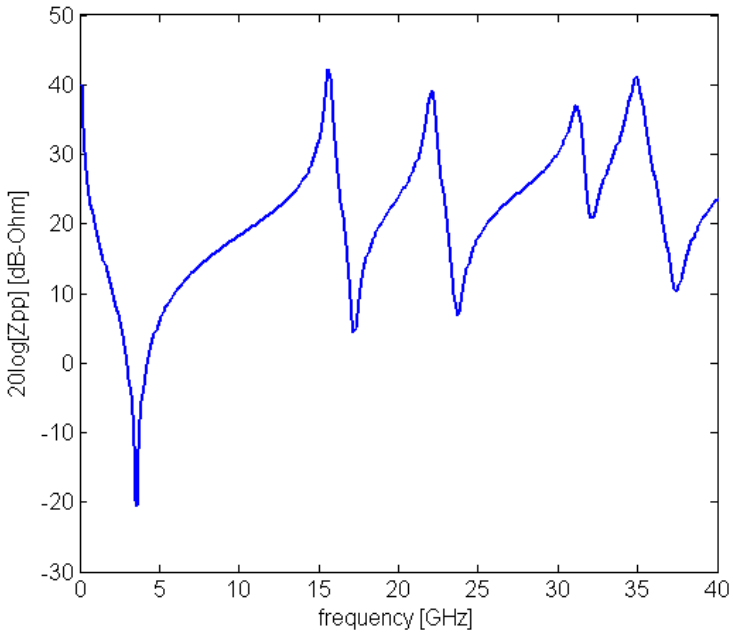
$$\begin{bmatrix} v_{i_u} \\ i_{i_u} \end{bmatrix} = \begin{bmatrix} 1 & Z_{pp} \\ 0 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{i_l} \\ i_{i_l} \end{bmatrix}$$

$$\begin{bmatrix} v_{i_l} \\ i_{i_l} \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ 1/Z_{p_l} & 1 \end{bmatrix} \cdot \begin{bmatrix} v'_{i_l} \\ i'_{i_l} \end{bmatrix}$$

A “Physics-Based” Model for Vias

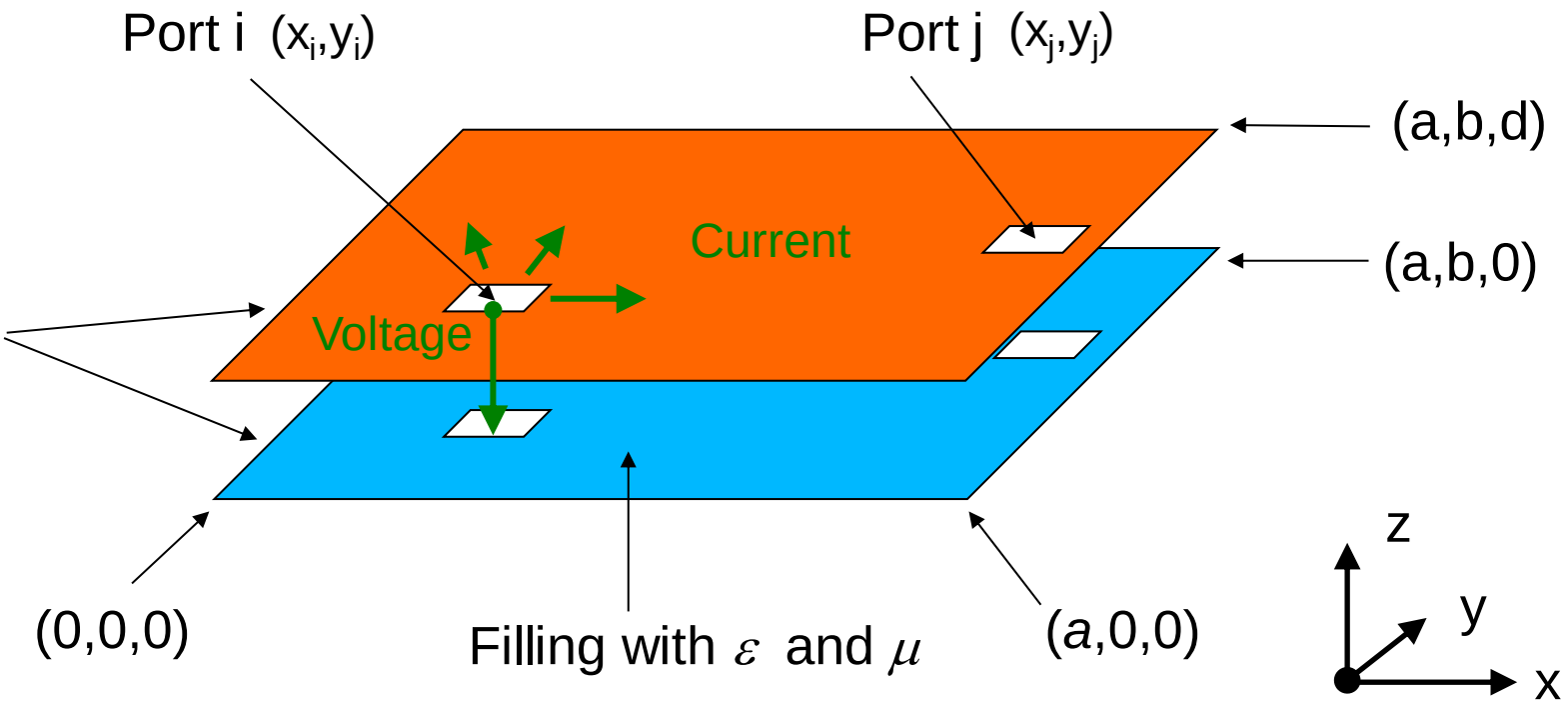
Simple example:





Planar Circuit Model I

CRM



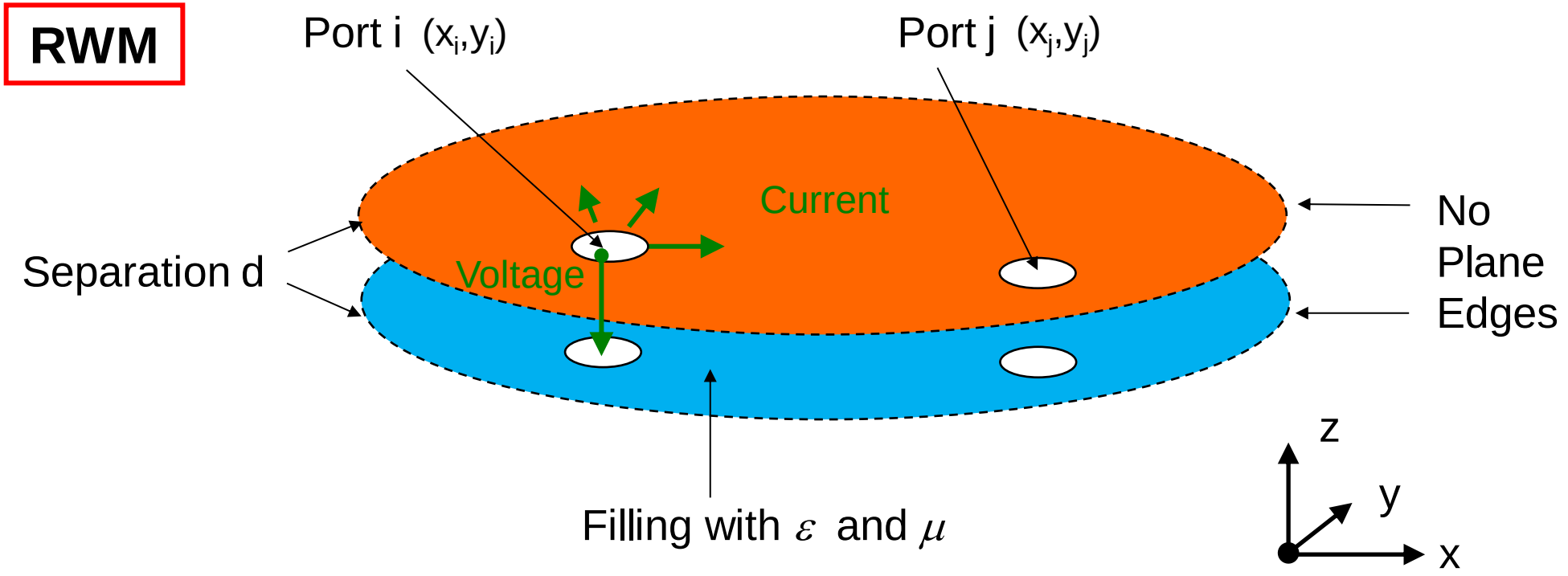
$$\underline{Z}_{ij}^{pp}(\omega) \approx \frac{j\omega\mu d}{ab} \cdot \sum_{m=0}^{\infty}\sum_{n=0}^{\infty} \left[C_m^2 C_n^2 \cdot \frac{\cos(k_{xm} x_i) \cdot \cos(k_{yn} y_i) \cdot \cos(k_{xm} x_j) \cdot \cos(k_{yn} y_j)}{k_{xm}^2 + k_{yn}^2 - k^2} \right]$$

$$k_{xm} = \frac{m\pi}{a}, \quad k_{yn} = \frac{n\pi}{b}, \quad k = \omega \cdot \sqrt{\mu\varepsilon}$$

$$C_m, C_n = 1 \text{ for } m, n = 0 \text{ and } \sqrt{2} \text{ otherwise}$$

Planar Circuit Model II

RWM

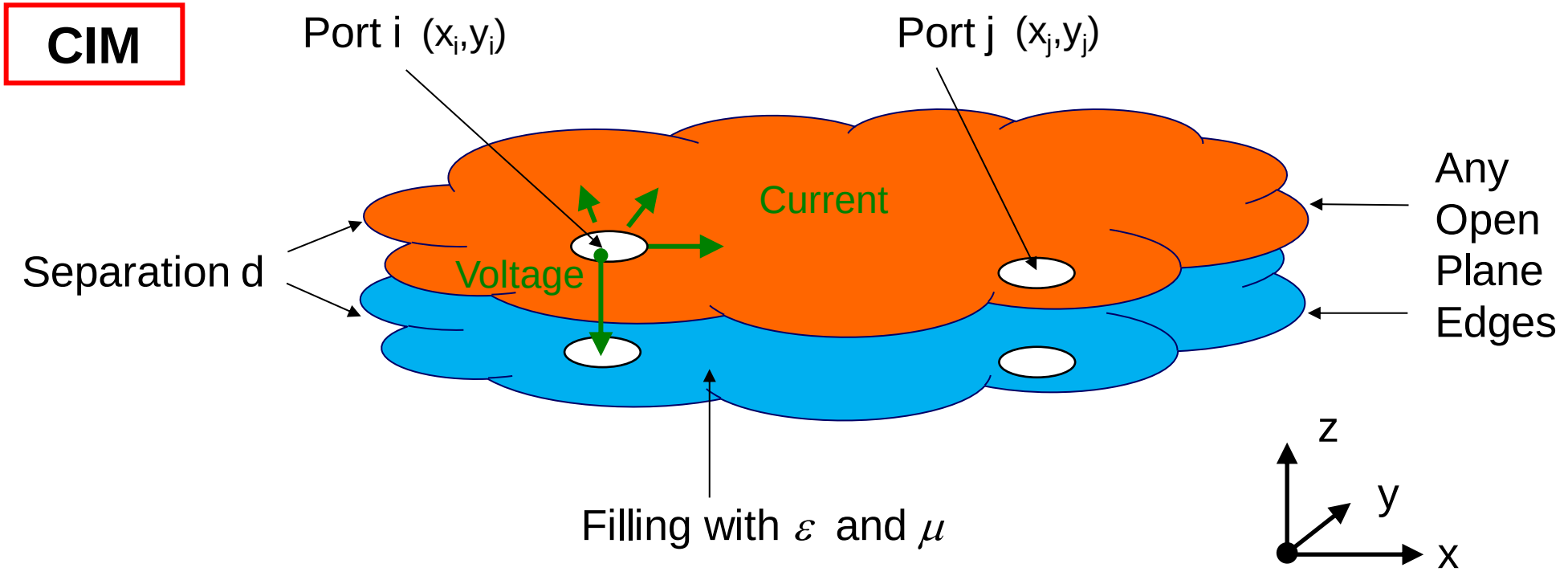


$$Z_{ij}^{pp}(\omega) = \frac{jd}{2\pi\rho_0} \cdot \sqrt{\frac{\mu}{\varepsilon}} \cdot \frac{H_0^{(2)}(k\rho_{ij})}{H_1^{(2)}(k\rho_0)}$$

$$\rho_0 = \text{port radius}, \quad \rho_0 = \text{port dist.}, \quad k = \omega \cdot \sqrt{\mu\varepsilon}$$

Planar Circuit Model III

CIM

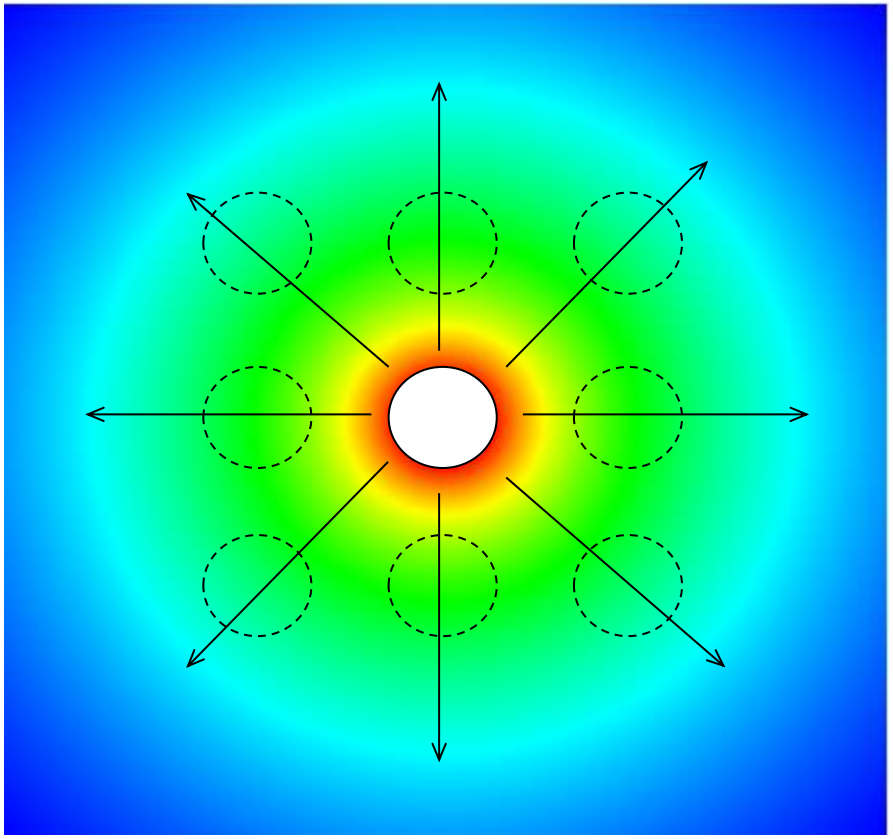


$$\underline{\underline{Z}}^{pp} = \underline{\underline{U}}^{-1} \cdot \underline{\underline{H}}$$

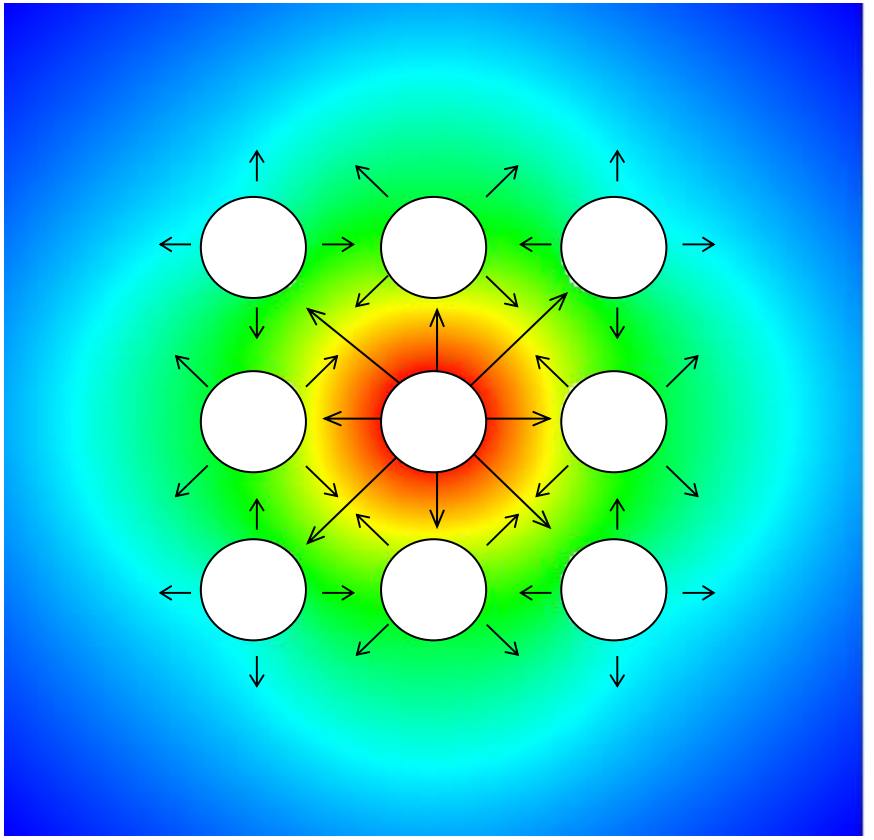
$$U_{ij} = \frac{k\pi a_j}{j} \cdot \begin{cases} J_0(ka_i) J_1(ka_j) H_0^{(2)}(kR) & i \neq j \\ J_0(ka_i) H_1^{(2)}(ka_i) & i = j \end{cases}$$

$$H_{ij} = \frac{k\eta d}{2} \cdot \begin{cases} J_0(ka_i) J_0(ka_j) H_0^{(2)}(kR) & i \neq j \\ J_0(ka_i) H_0^{(2)}(ka_i) & i = j \end{cases}$$

Effect of Multiple Scatterings



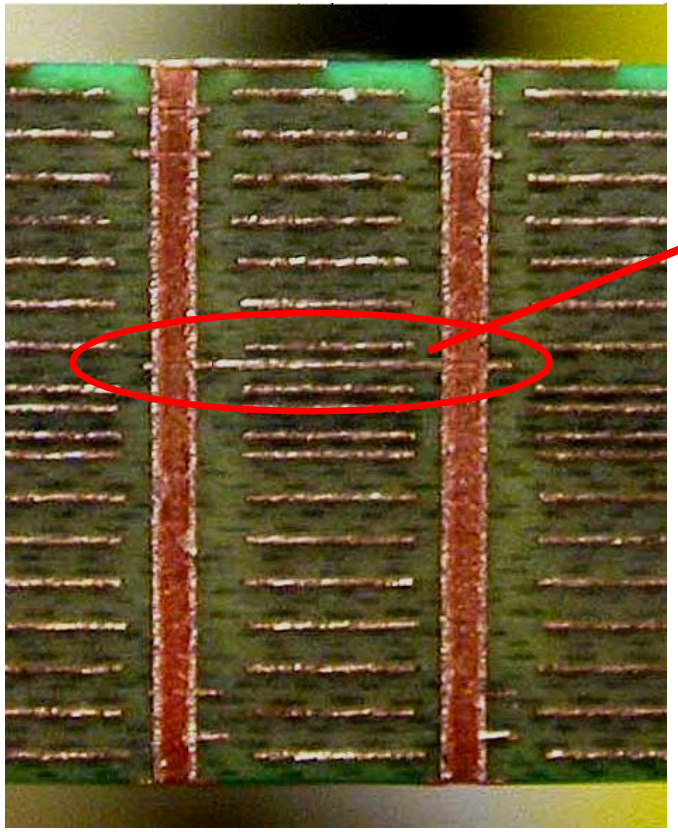
Fields “seen by” CRM & RWG



Fields “seen by” CIM

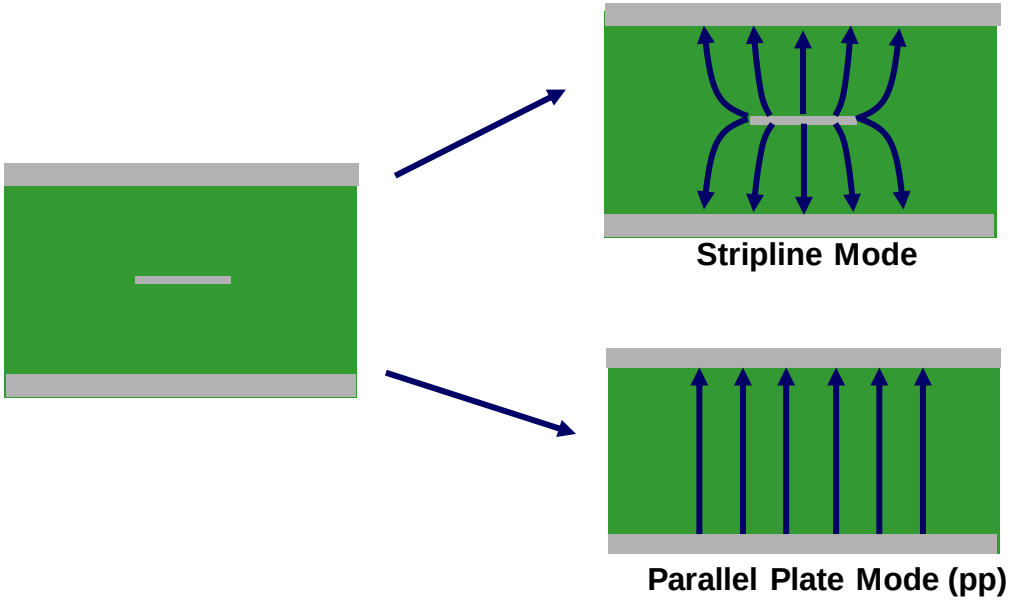
X. Duan, R. Rimolo-Donadio, S. Müller, K. Han, X. Gu, Y. Kwark, H.-D. Brüns, C. Schuster, **„Impact of Multiple Scattering on Passivity of Equivalent-Circuit Via Models“,** IEEE Electrical Design of Advanced Package & Systems Symposium (EDAPS), Hangzhou, China, December 12-14, 2011.

Including Striplines

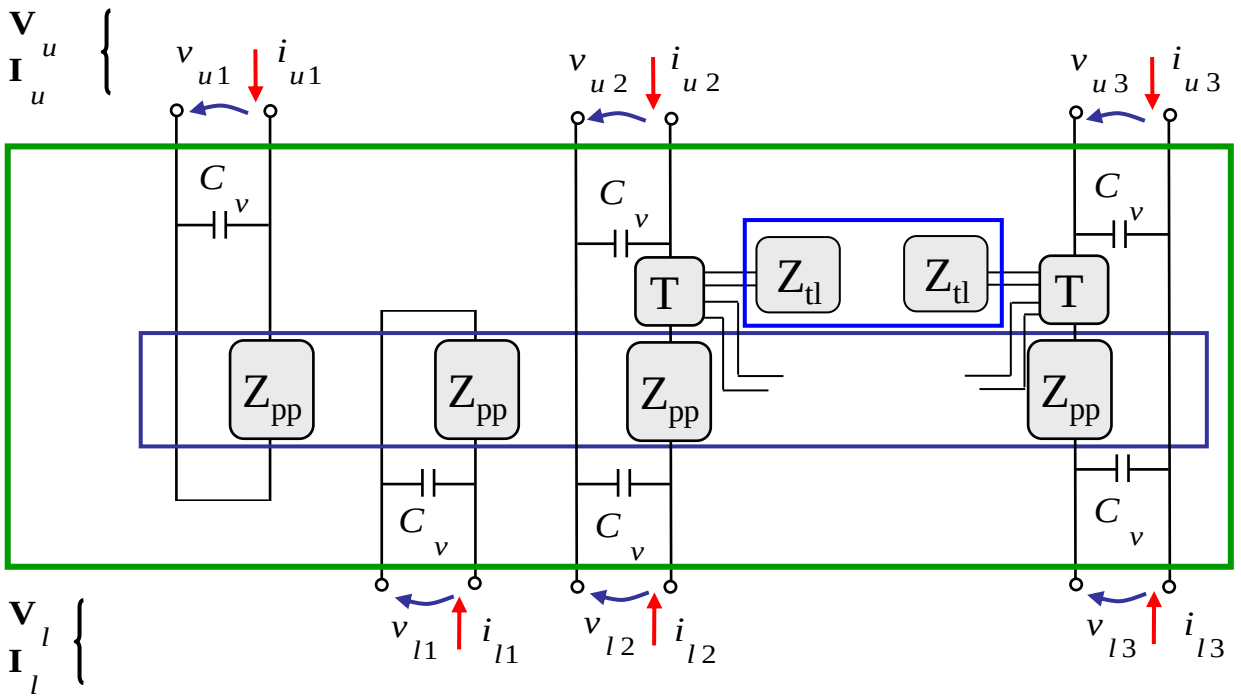


Trace between planes:

2 Modes: Stripline + Parallel Plate



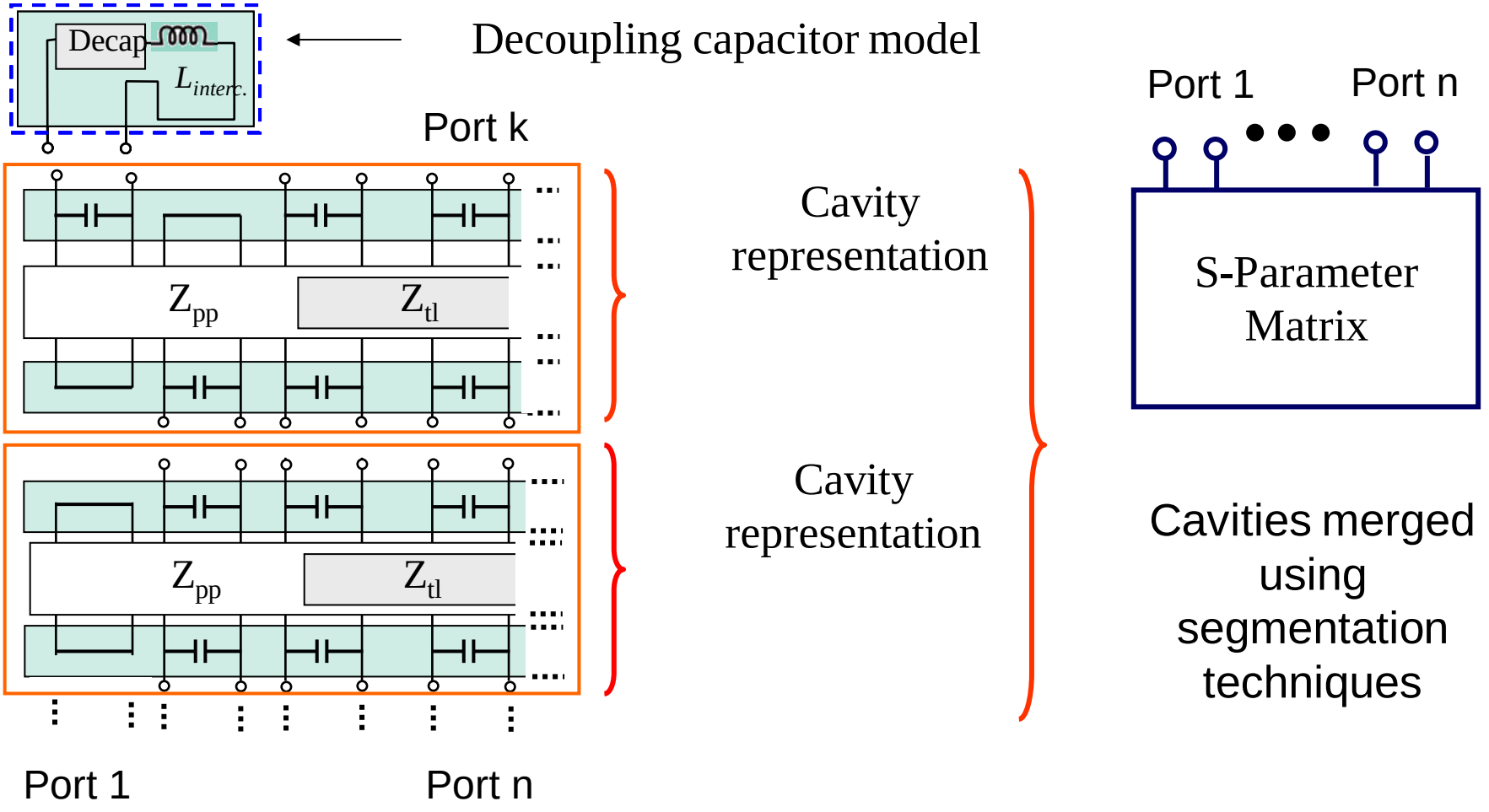
Complete Model for One Cavity



$$\begin{bmatrix} \mathbf{I}_u \\ \mathbf{I}_l \end{bmatrix} = \left[\begin{pmatrix} \mathbf{Y}_{vu} & \mathbf{0} \\ \mathbf{0} & \mathbf{Y}_{vl} \end{pmatrix} + \begin{pmatrix} +\mathbf{Y}_{pp} & -\mathbf{Y}_{pp} \\ -\mathbf{Y}_{pp} & +\mathbf{Y}_{pp} \end{pmatrix} + \begin{pmatrix} -\mathbf{k}\cdot\mathbf{Y}_{tl} & \mathbf{0} \\ \mathbf{0} & (\mathbf{k}+1)\cdot\mathbf{Y}_{tl} \end{pmatrix} + \begin{pmatrix} (\mathbf{k}^2+\mathbf{k})\cdot\mathbf{Y}_{tl} & -(\mathbf{k}^2+\mathbf{k})\cdot\mathbf{Y}_{tl} \\ -(\mathbf{k}^2+\mathbf{k})\cdot\mathbf{Y}_{tl} & (\mathbf{k}^2+\mathbf{k})\cdot\mathbf{Y}_{tl} \end{pmatrix} \right] \cdot \begin{bmatrix} \mathbf{V}_u \\ \mathbf{V}_l \end{bmatrix}$$

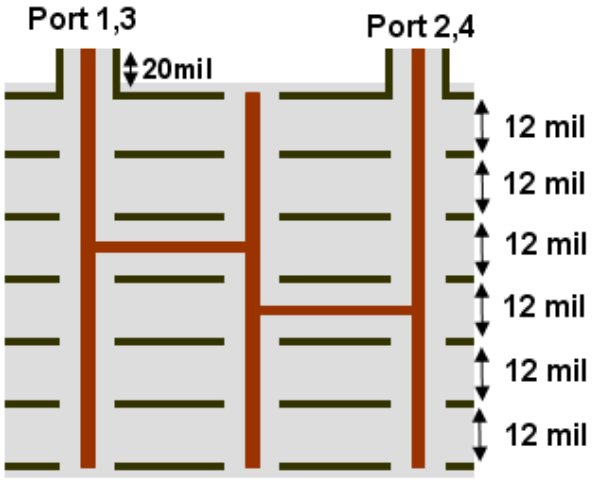
R. Rimolo-Donadio, X. Gu, Y. H. Kwark, M. B. Ritter, B. Archambeault, F. D. Paulis, Y. Zhang, J. Fan, H.-D. Brüns, C. Schuster, **"Physics-based via and trace models for efficient link simulation on multilayer structures up to 40 GHz,"** *IEEE Trans. on Microwave Theory and Techniques*, vol. 57, no. 8, pp. 2072-2083, August 2009.

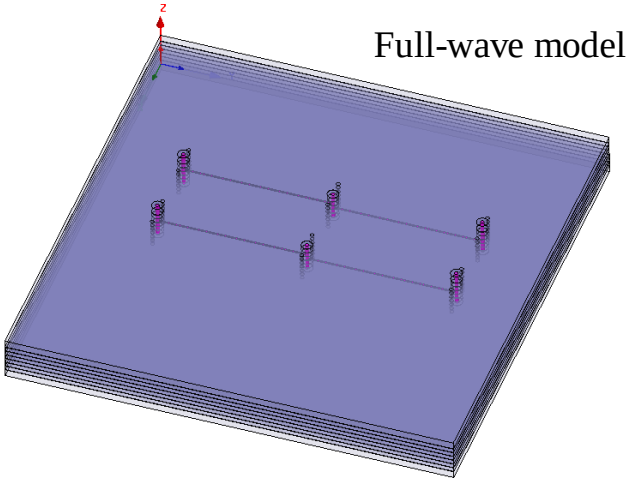
Complete Model for Full PCB



R. Rimolo-Donadio, X. Gu, Y. H. Kwark, M. B. Ritter, B. Archambeault, F. D. Paulis, Y. Zhang, J. Fan, H.-D. Brüns, C. Schuster, **"Physics-based via and trace models for efficient link simulation on multilayer structures up to 40 GHz,"** *IEEE Trans. on Microwave Theory and Techniques*, vol. 57, no. 8, pp. 2072-2083, August 2009.

Comparison with Full-Wave Results

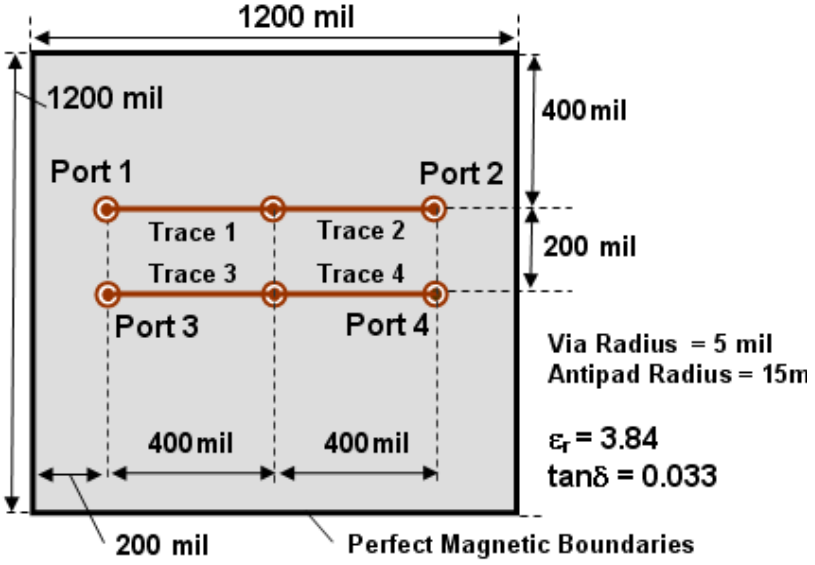


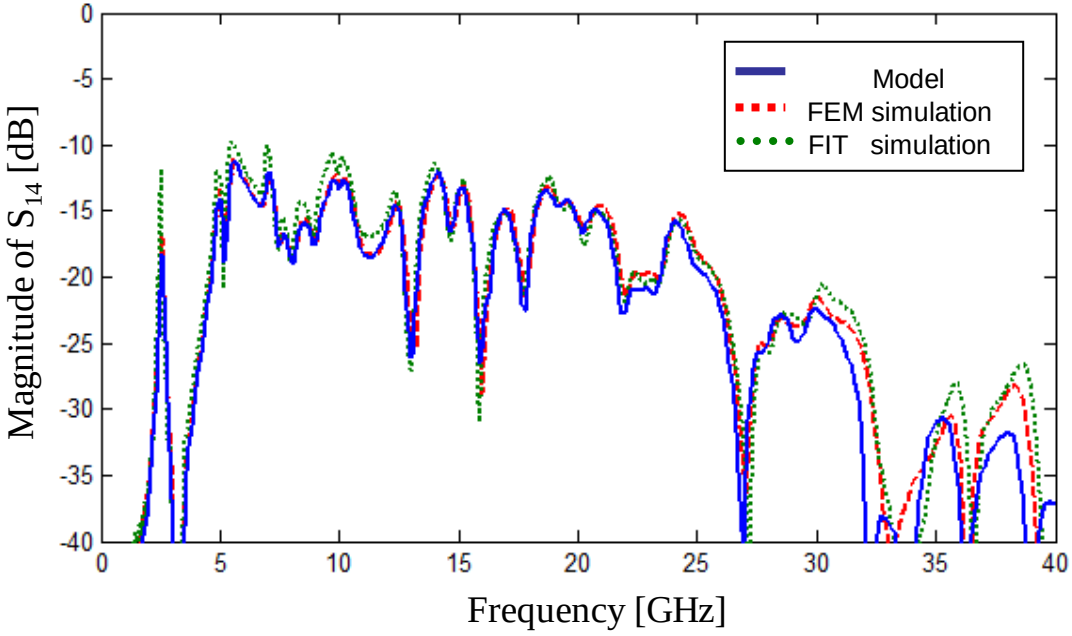


Full-wave model

6 Vias, 4 traces case

Centered striplines at two levels, and thru vias in a 6 cavity stackup





Comparison with Full-Wave Results

COMPUTATION TIMES OBTAINED BY DIFFERENT METHODS

Finite element method simulation (200 freqs)	Finite integration technique simulation	Proposed models (200 frequency points)	
		Cavity model double sum, 100x100 modes	Cavity model single sum, 50 iterations
11 144 s (~3 h 5 min)	24 804 s (~4 h 53 min)	23 s	9 s

*computed on a 3.0 GHz PC, with 4GB RAM.

3D Model required

Field information available

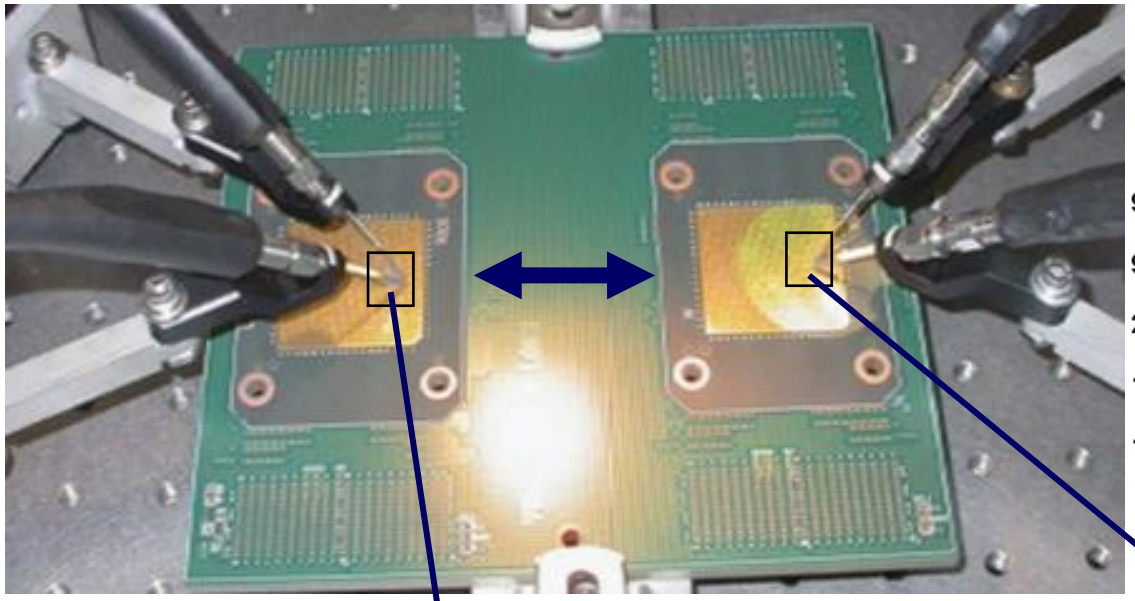
High level description (text-based)

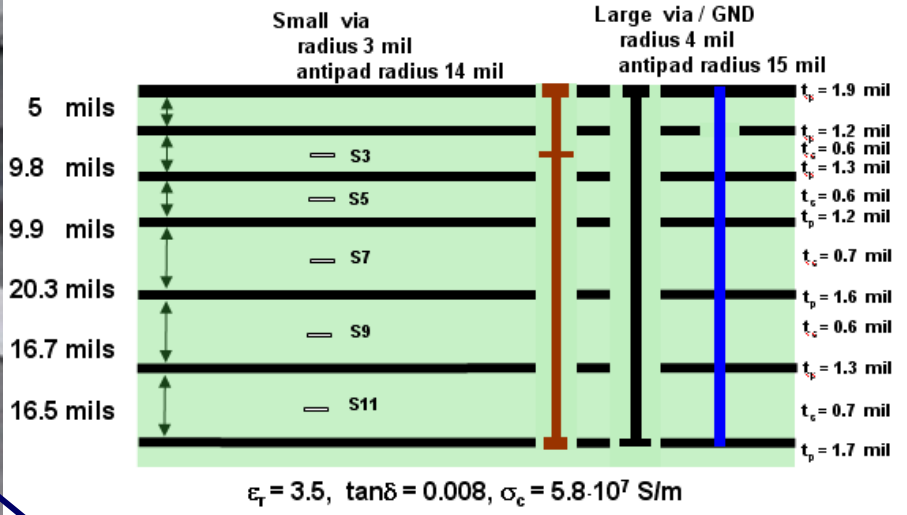
Network Parameters

Computation is 2 to 3 orders of magnitude faster in comparison to general-purpose numerical methods!

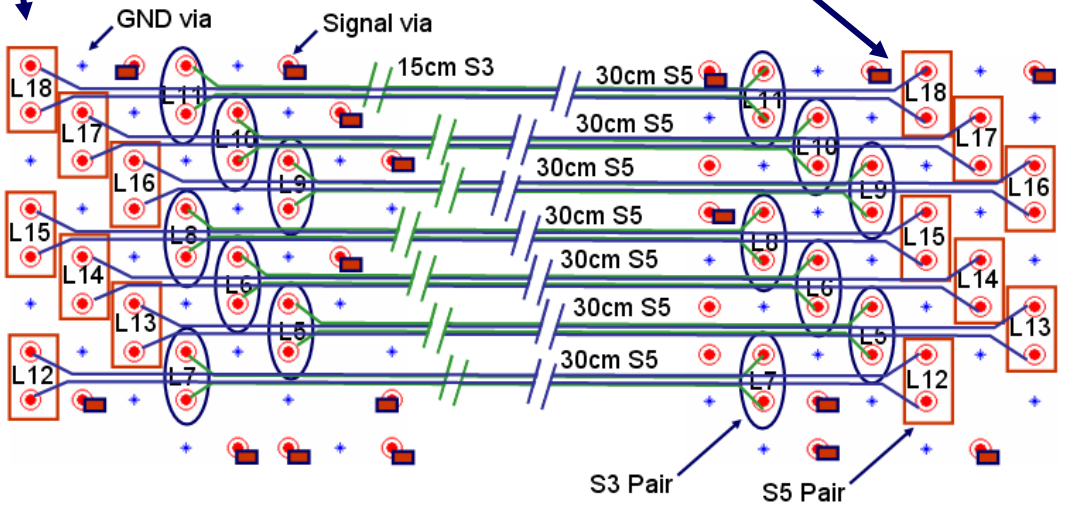
R. Rimolo-Donadio, X. Gu, Y. H. Kwark, M. B. Ritter, B. Archambeault, F. D. Paulis, Y. Zhang, J. Fan, H.-D. Brüns, C. Schuster, **"Physics-based via and trace models for efficient link simulation on multilayer structures up to 40 GHz,"** *IEEE Trans. on Microwave Theory and Techniques*, vol. 57, no. 8, pp. 2072-2083, August 2009.

Comparison with Measurements





Assumption of infinite plates



- 119 vias (76 signal, 43 ground)
- 14 differential striplines (2D)
- 6 cavities
- Terminations

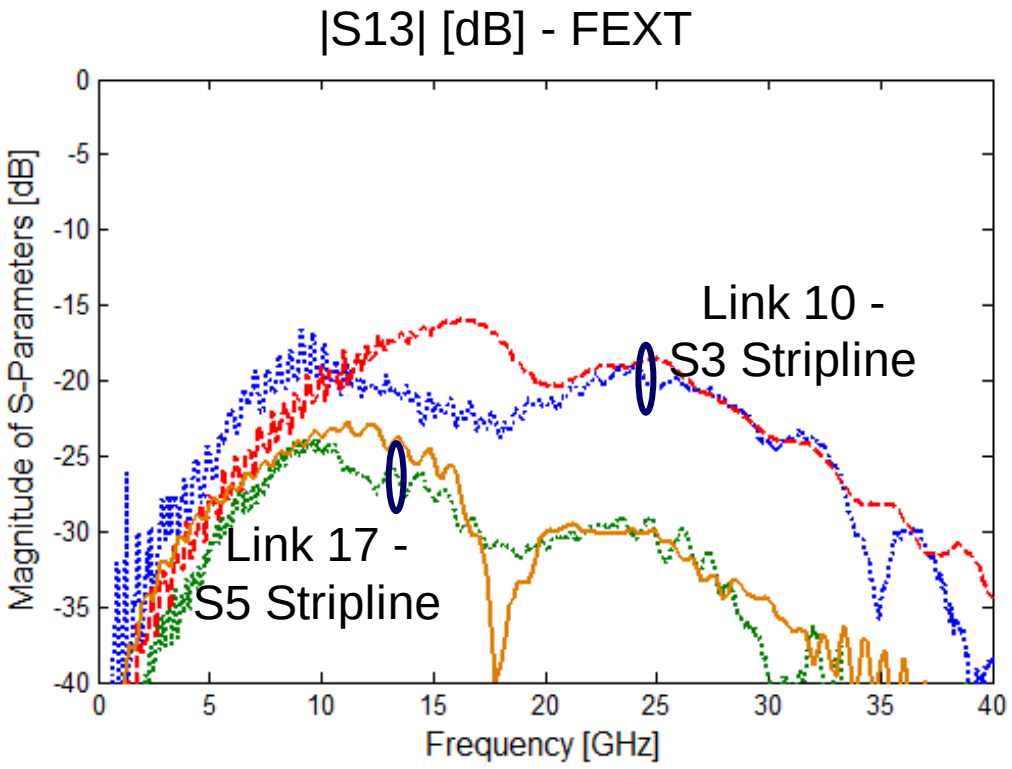
Comp. time: < 3 min

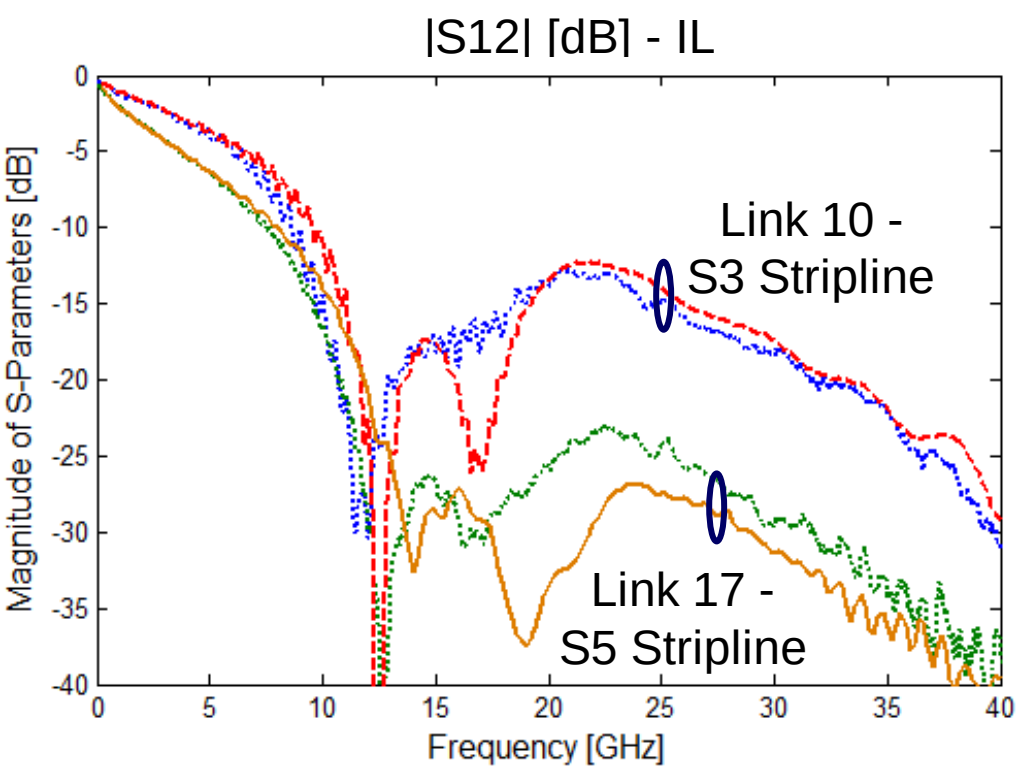
R. Rimolo-Donadio, X. Gu, Y. H. Kwark, M. B. Ritter, B. Archambeault, F. D. Paulis, Y. Zhang, J. Fan, H.-D. Brüns, C. Schuster, **"Physics-based via and trace models for efficient link simulation on multilayer structures up to 40 GHz,"** *IEEE Trans. on Microwave Theory and Techniques*, vol. 57, no. 8, pp. 2072-2083, August 2009.

TET

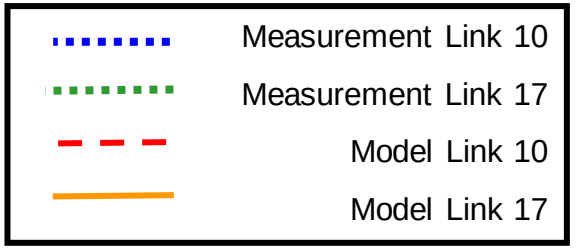
UHH Universität Hamburg-Harburg

Comparison with Measurements

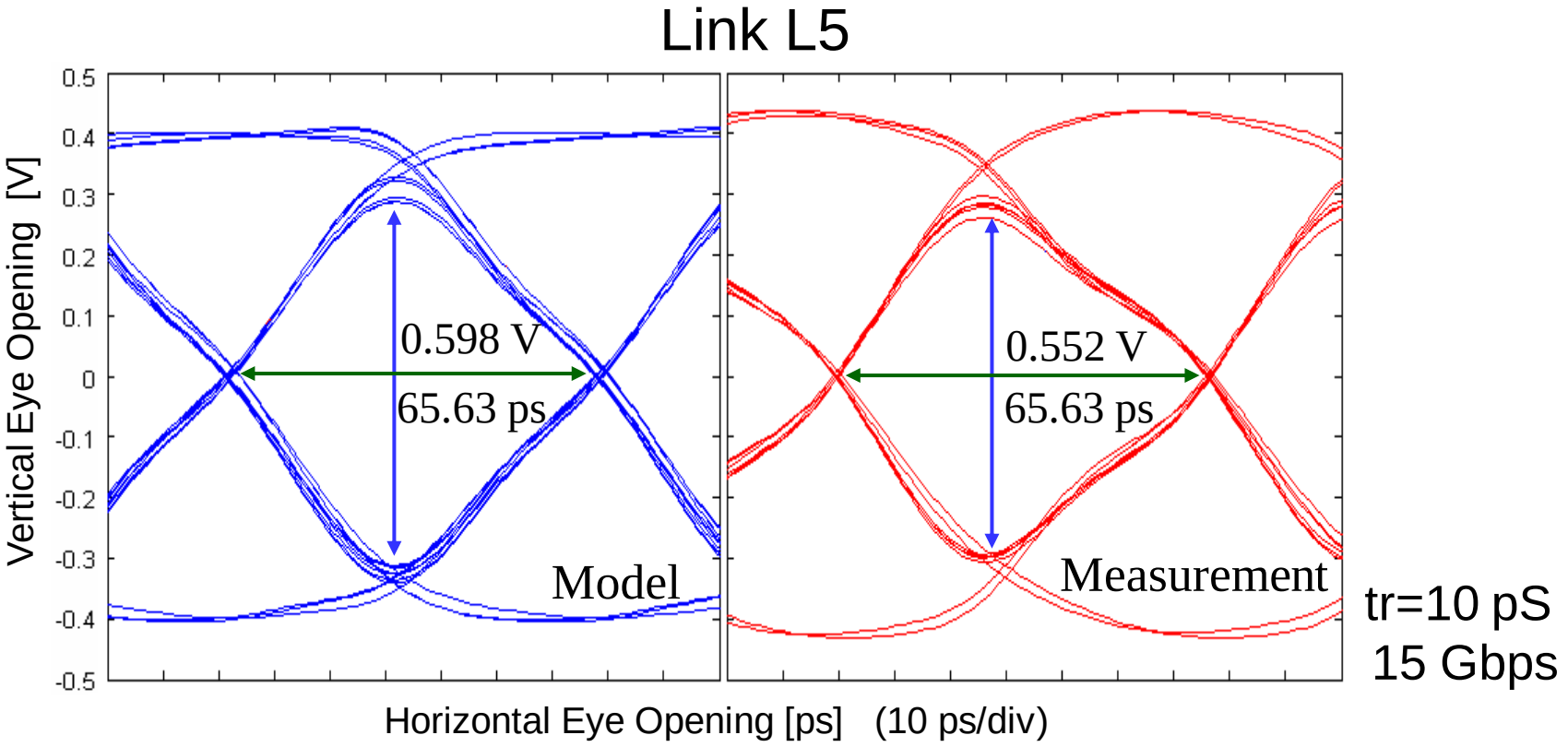




Models capture the salient features of the hardware response despite simplifications



Comparison with Measurements



tr=10 pS
15 Gbps

Simulation of the time domain link performance up to 15 Gbps within 10% accuracy!

Models for Vias – Summary

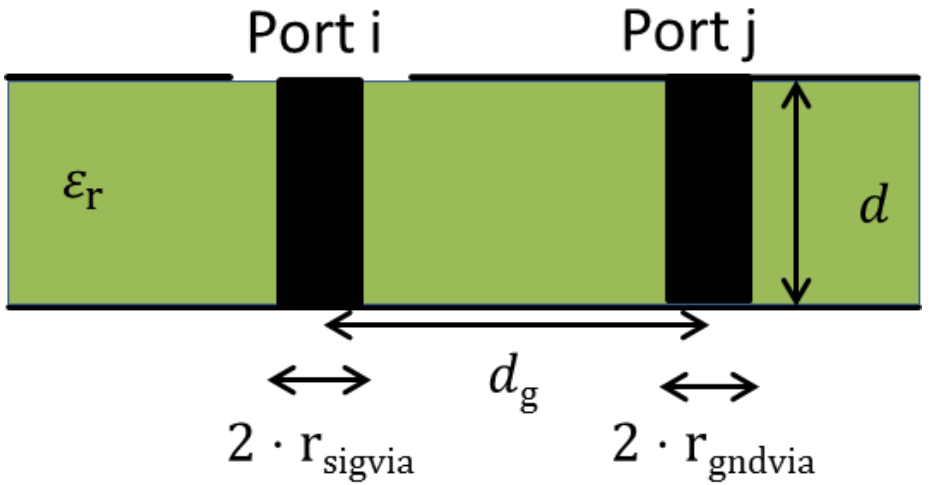
- ➔ Physics based via models can predict SI, PI, and EMC issues on PCBs up to tens of GHz
- ➔ They do this (very) efficiently
- ➔ They do this (quite) accurately
- ➔ … but limitations exist with regard to shape, size, and proximity of vias!

(4)

Application Example

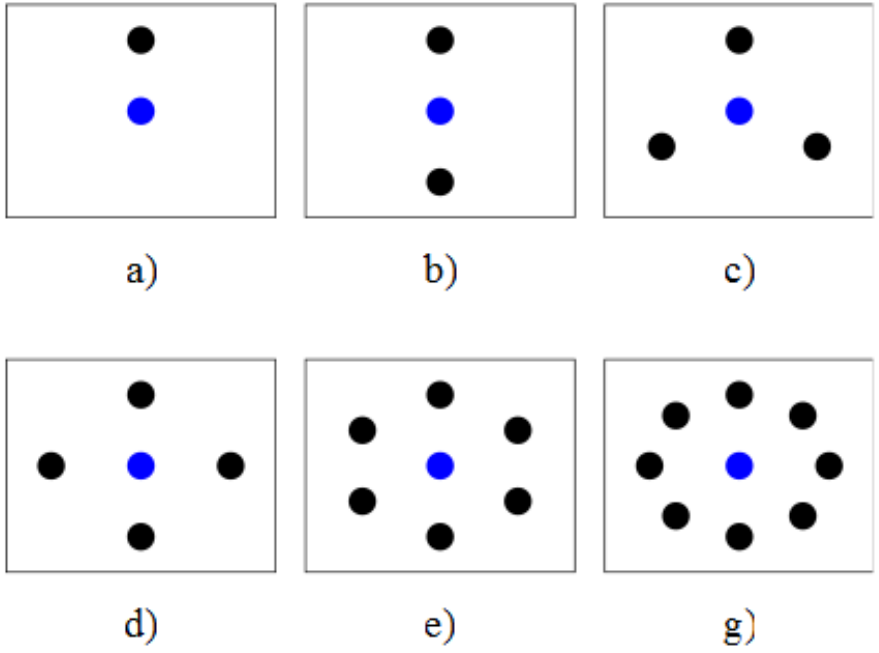
1. Design of Controlled Vias

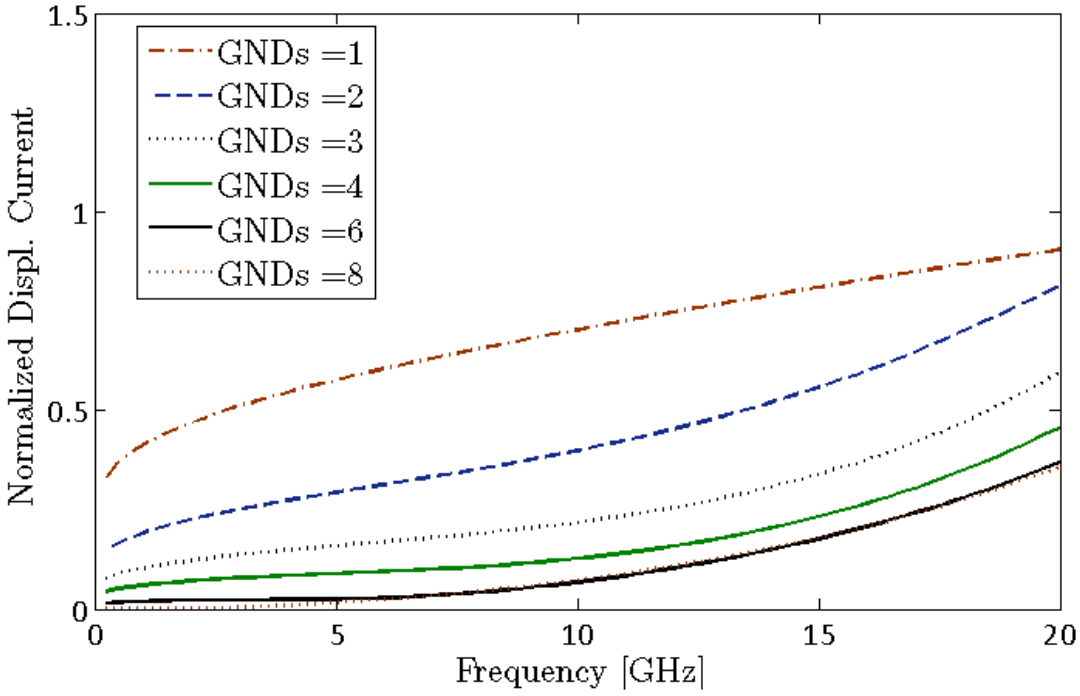
Calculation of Ground and Displacement Return Currents using CIM



1. Design of Controlled Vias

Effect of Number of Ground Vias



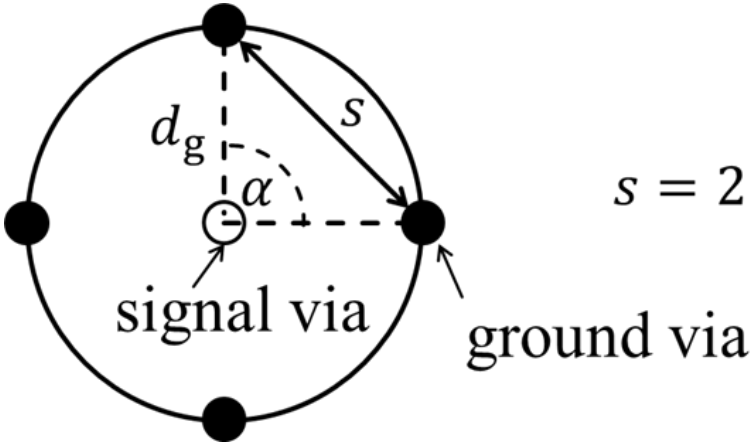


1. Design of Controlled Vias

Engineering Rules for Design

1.) The number of ground vias should always be ≥ 2!

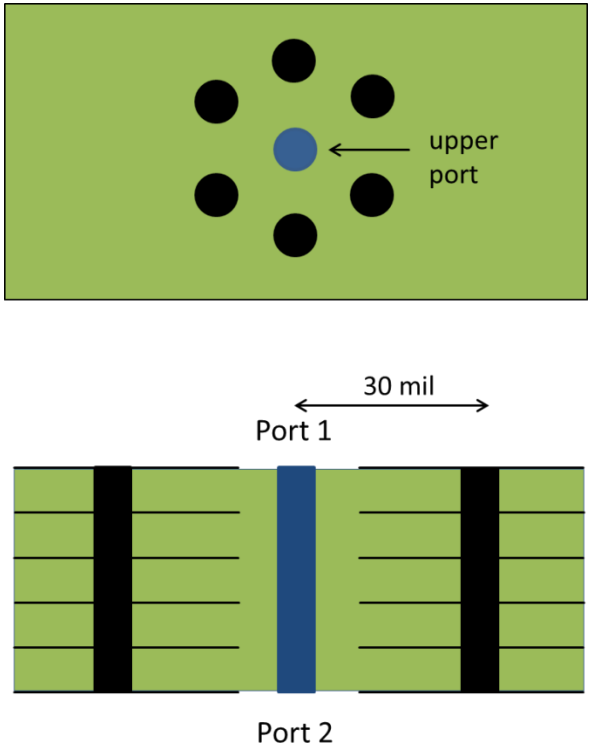
2.) The aperture *s* should not exceed $0.08 \cdot \lambda$ where λ is the wavelength at 20 GHz for a normalized displacement current of less than 10%!

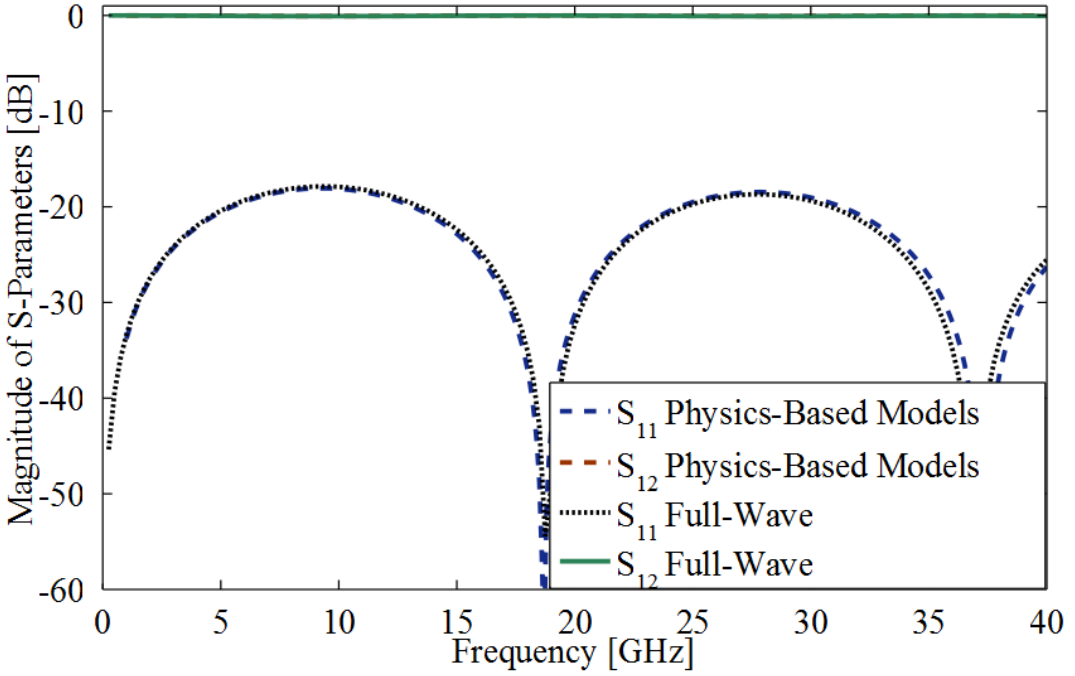


$$s = 2 \cdot \left(d_g \sin\frac{\alpha}{2} - r_{gndvia} \right) \qquad \alpha = 360°/N_{gnd}$$

1. Design of Controlled Vias

Application Example





13 layers

The via shows a typical transmission line behavior (reflection)

The transmission is above -1dB up to 40GHz

Application Examples – Summary

- ➔ Physics based via models can be used to mitigate common SI and PI issues
- ➔ They are especially useful for pre-layout analysis
- ➔ Due to their efficiency PCB layout automation and optimization become „viable“

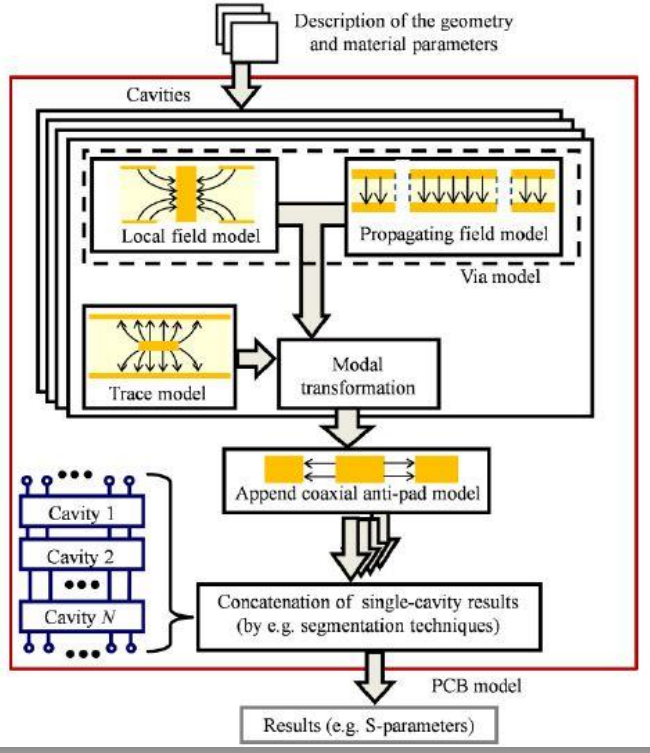
For More Information

Complete Modeling of Large Via Constellations in Multilayer Printed Circuit Boards

S. Müller, *Student Member, IEEE*, F. Happ, X. Duan, *Member, IEEE*,
R. Rimolo-Donadio, *Member, IEEE*, H.-D. Brüns, and C. Schuster, *Senior Member, IEEE*

***Abstract*— This paper presents for the first time the comprehensive modeling of complete via constellations of up to 10,000 elements in multilayer printed circuit boards with up to 8 cavities using the physics-based approach. For each computational step of the physics-based approach, several alternatives are analyzed with regard to their computational efficiency, and calculation times are discussed as a function of the number of simulated vias. The results of this analysis are used in combination with previous studies to determine an efficient yet accurate algorithm for the simulation of large numbers of vias. The impact of the stackup configuration on the computational effort of the algorithm is analyzed, and the most computationally expensive parts of the calculation process are identified. A parallelization of the algorithms is carried out to accelerate the critical calculation tasks. As an evaluation example, simulation results for a via array consisting of 10,000 vias and 8 cavities are shown. With the proposed simulation methods, the computation time for this via array is about 6.5 hours per frequency point on a single CPU and about 40 minutes per frequency point with the parallel version running on 16 CPUs.**

***Index Terms*—through-hole via, multilayer printed circuit board, equivalent circuit model, computational electromagnetics**



I. INTRODUCTION

Published in IEEE Transactions on Components, Packaging, and Manufacturing Technology, vol. 3, no. 3, March 2013

Technische Universität Hamburg-Harburg

Contact Information

Jan Birger Preibisch,
Prof. Dr. sc. techn. Christian Schuster

Institut für Theoretische Elektrotechnik
Technische Universität Hamburg-Harburg
Harburger Schloss Str. 20
21079 Hamburg, Germany

Tel: +49 40 42878 3116
WWW: http://www.tet.tu-harburg.de/
E-Mail: jan.preibisch@tuhh.de, schuster@tuhh.de