European IBIS Summit

Berlin, Germany
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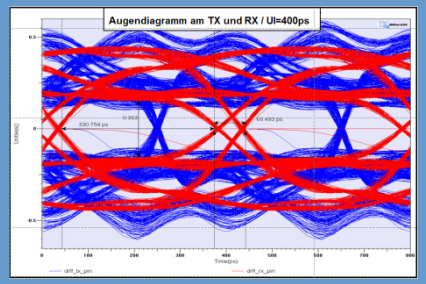

SSO Experience with IBIS

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Overview

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What is SSO / SSN (Simultaneous Switching Outputs /Noise)

- General terms to SSO
- Examples with Transistor based models

How exact will IBIS models describe the SSO?

- Results of SSO with IBIS models

Conclusions

SSO Simulation Setup / m+1

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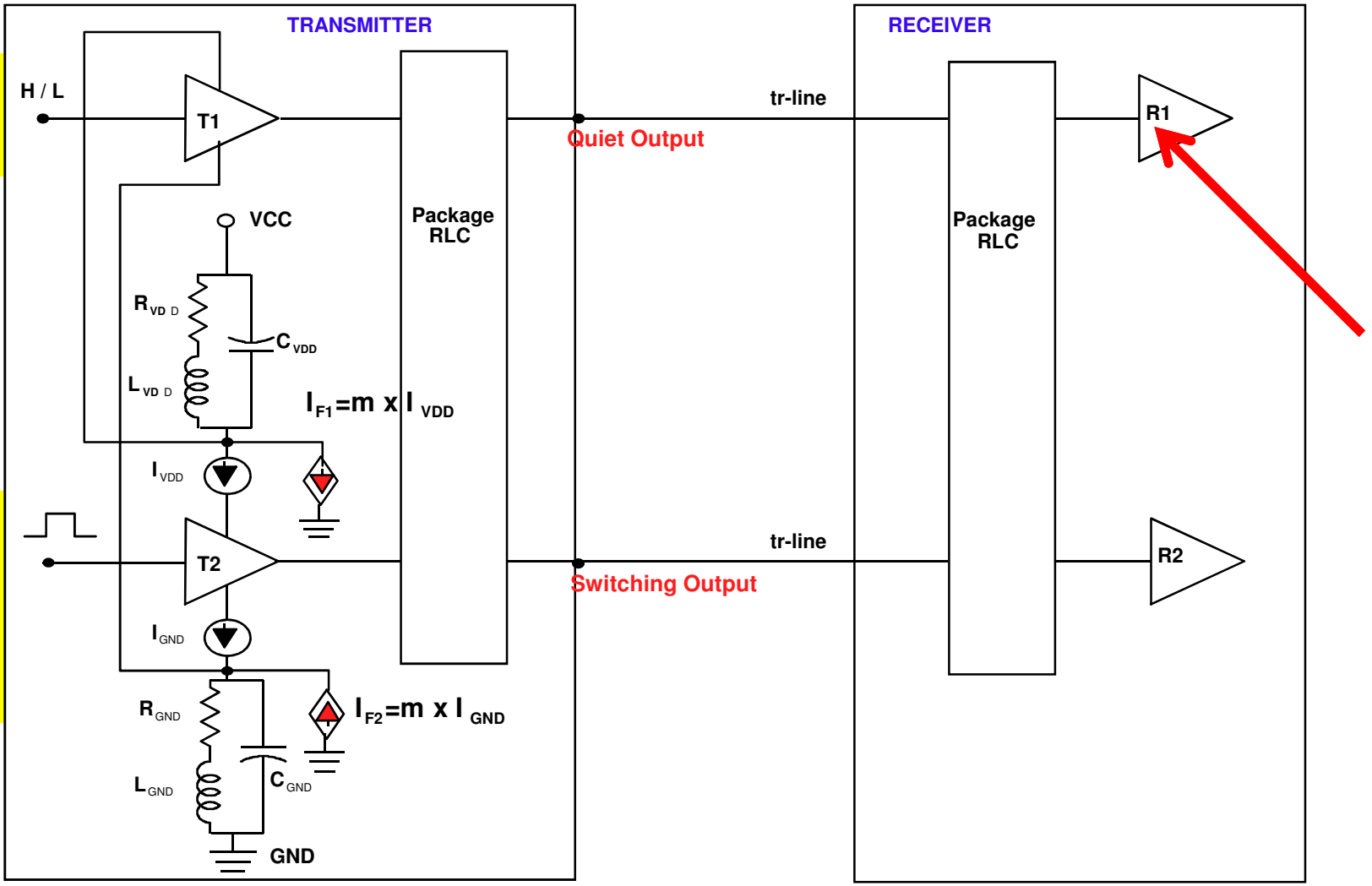
1 x output
➔ quiet

m x outputs
➔ simultaneous switching



What are the SSO effects?

Supply Voltage drop + Ground Bounce

➔ **Additional Timing delay**

➔ **Wrong signaling**

FF toggle

Oscillating output signal

(increasing power +additional heat)

Why SSO is no (more) actual issue?

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➔ **HS-Signal transmissions have changed from parallel to serial**

➔ **Differential signaling instead of single ended**

➔ **CML technology has replaced the Totem Pole technology**

Output Signal and I_vdd / I_gnd

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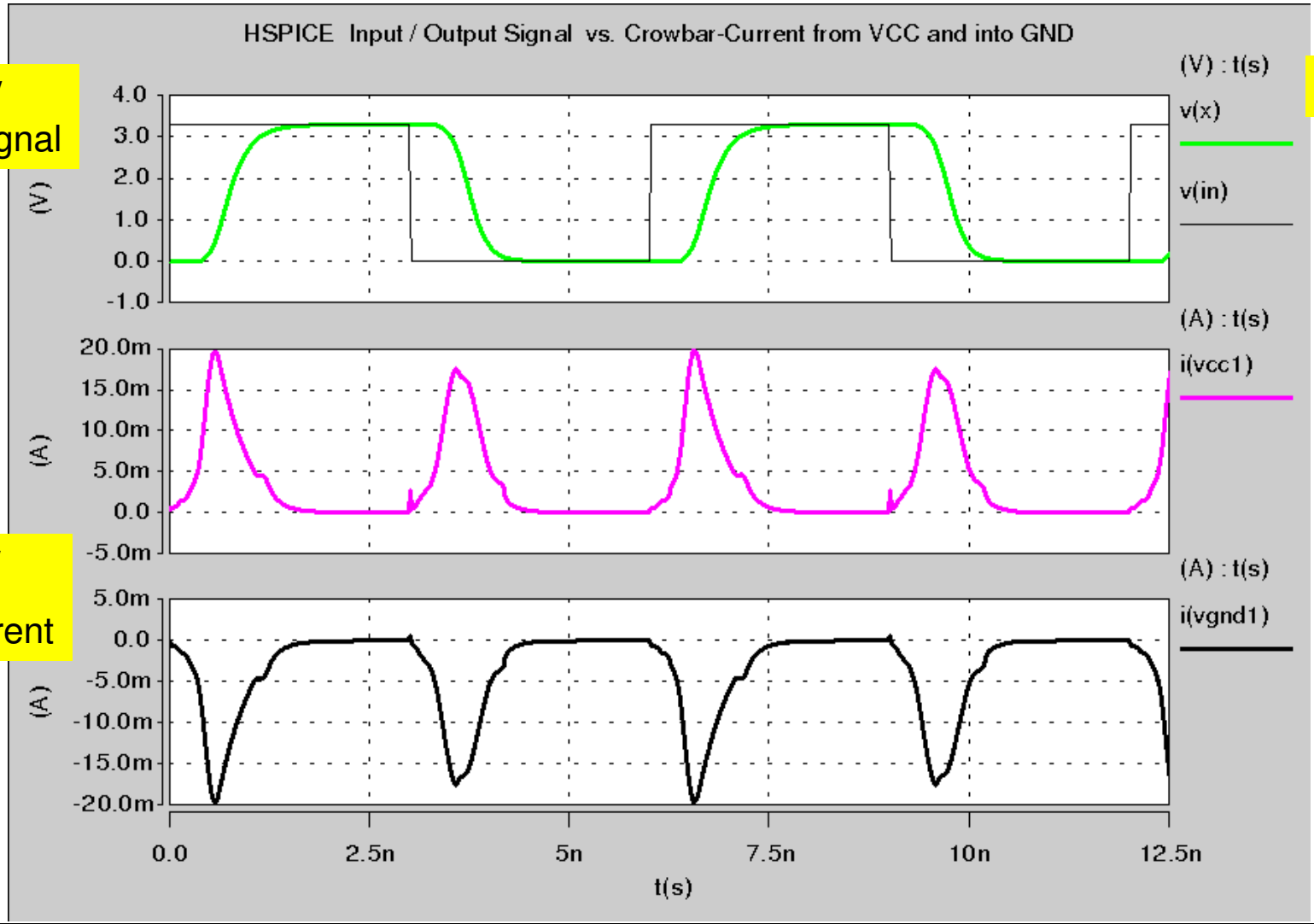
Input / Output Signal

VDD-/ GND-current

C_load=0pF



Output Signal and I_vdd / I_gnd

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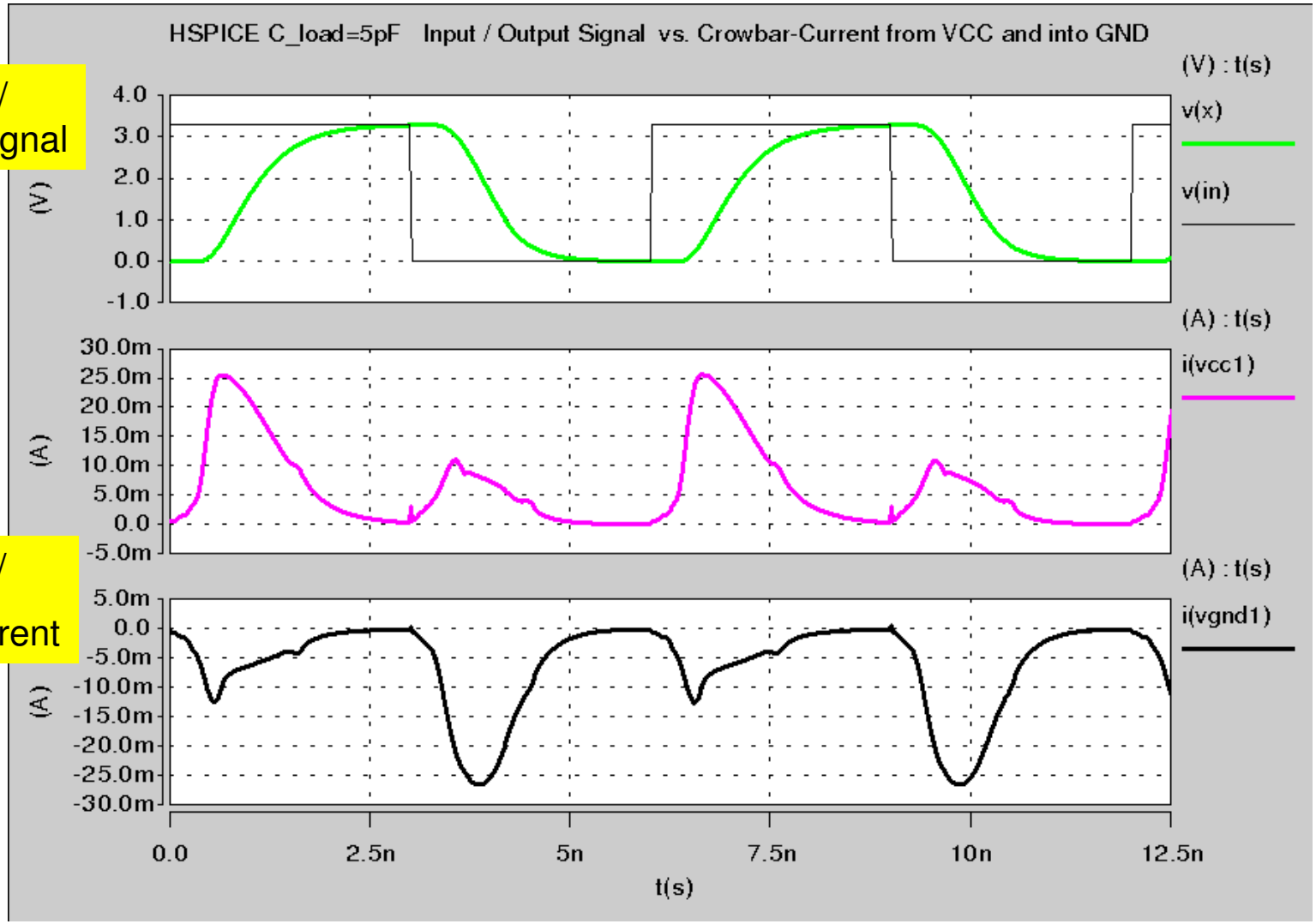
Input / Output Signal

VDD-/ GND-current

C_load=5pF



VDD / GND – voltage drop

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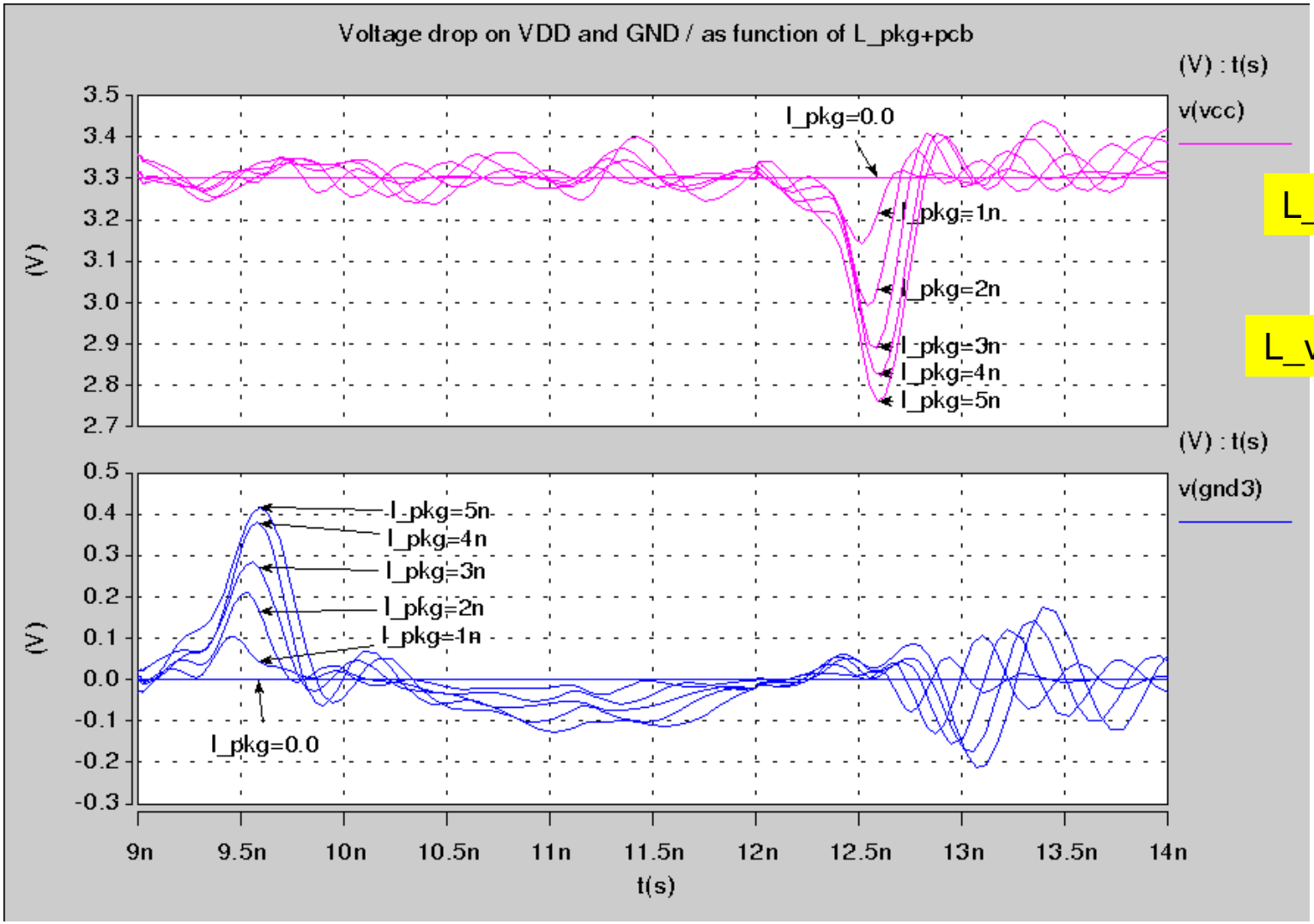
Vdd

GND



L_vdd = L_gnd

L_vdd = 0 …5nH

6 x SSO / C_load=5pF / L_vdd=2nH

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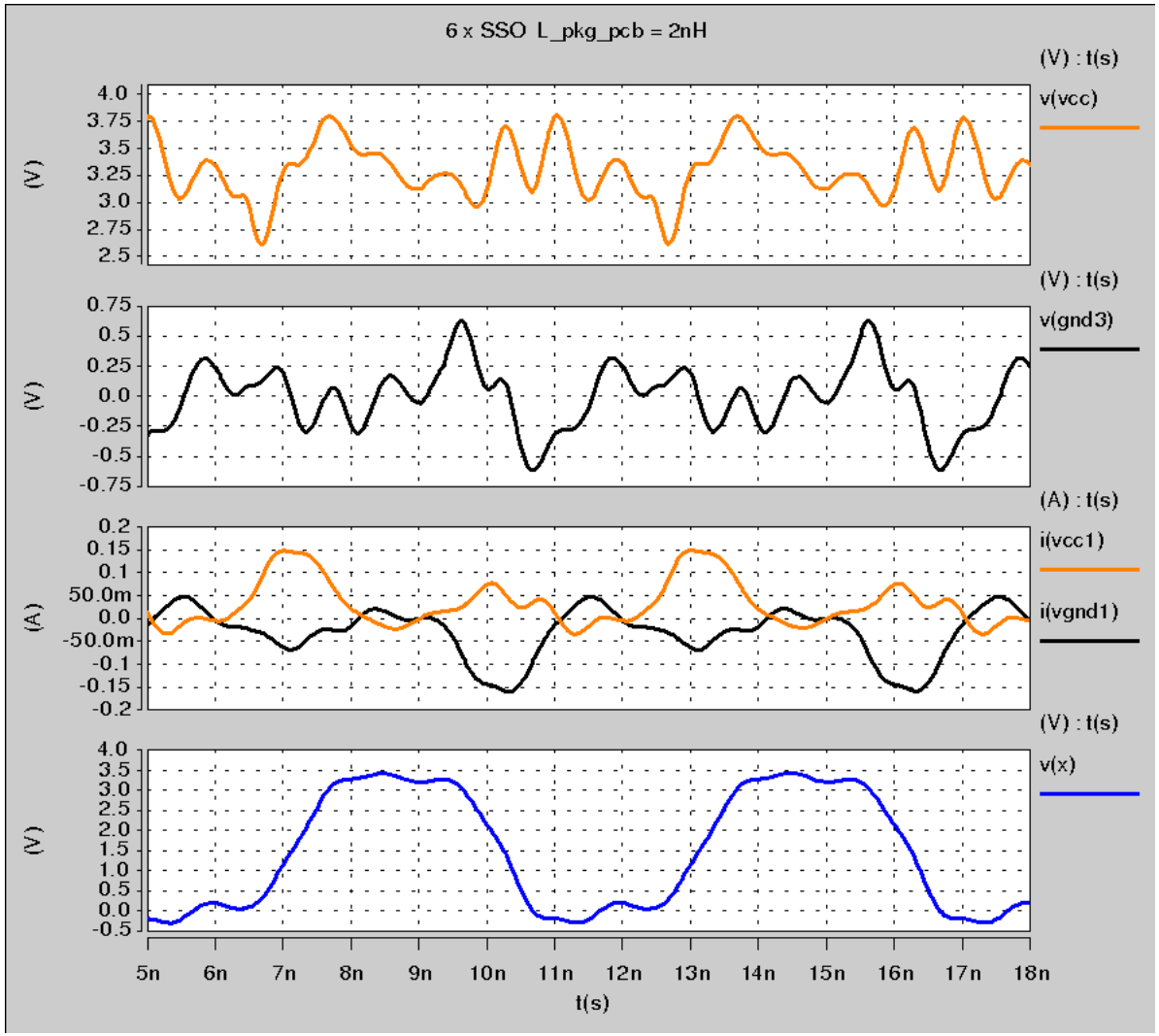
Vdd

GND

I_vdd/I_gnd

Output



C_load=5pF

6 x SSO / C_load=5pF / L_vdd=0..3nH

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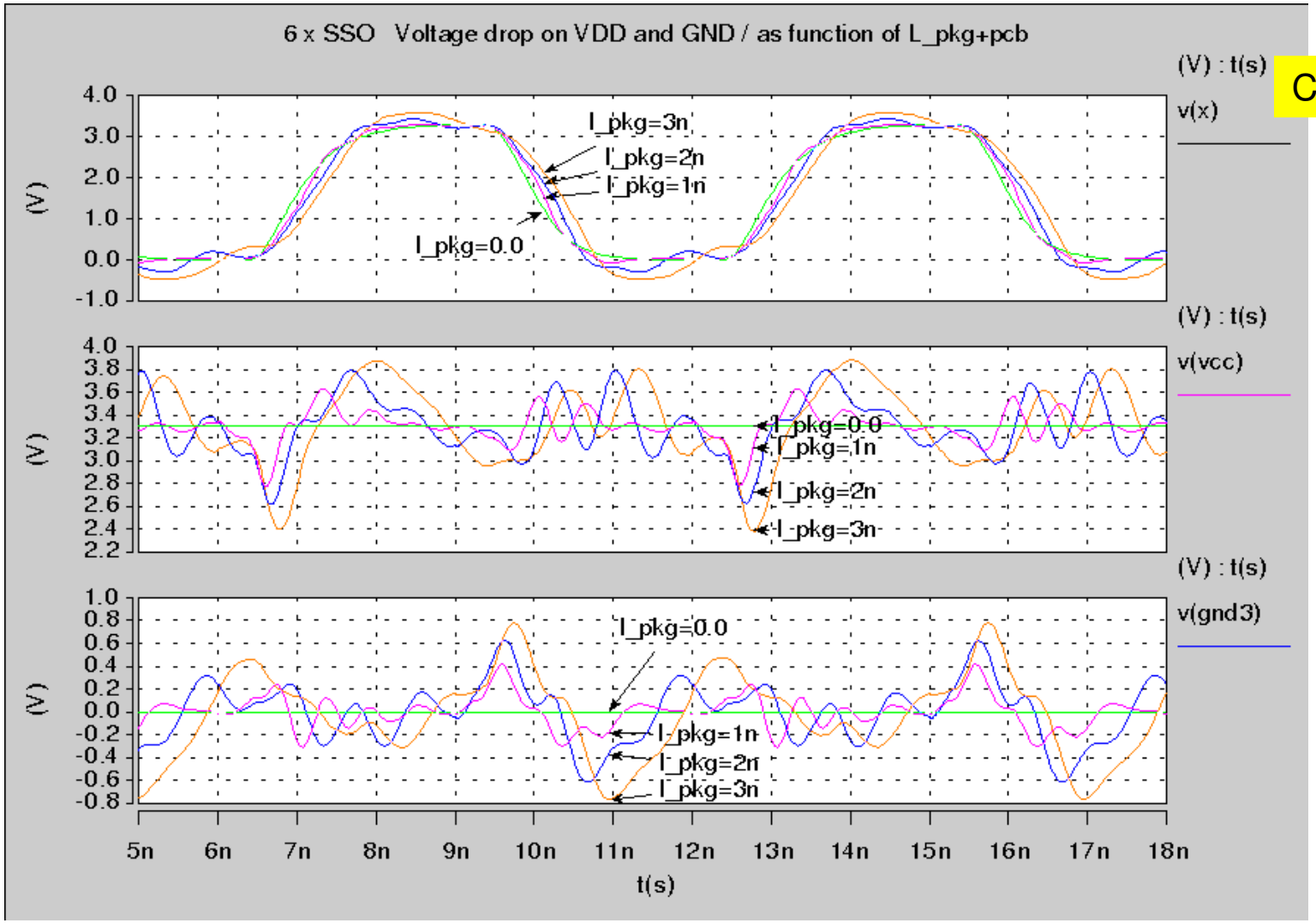
Output

Vdd

GND



C_load=5pF

Vdd/GND-Current of a IBIS Model

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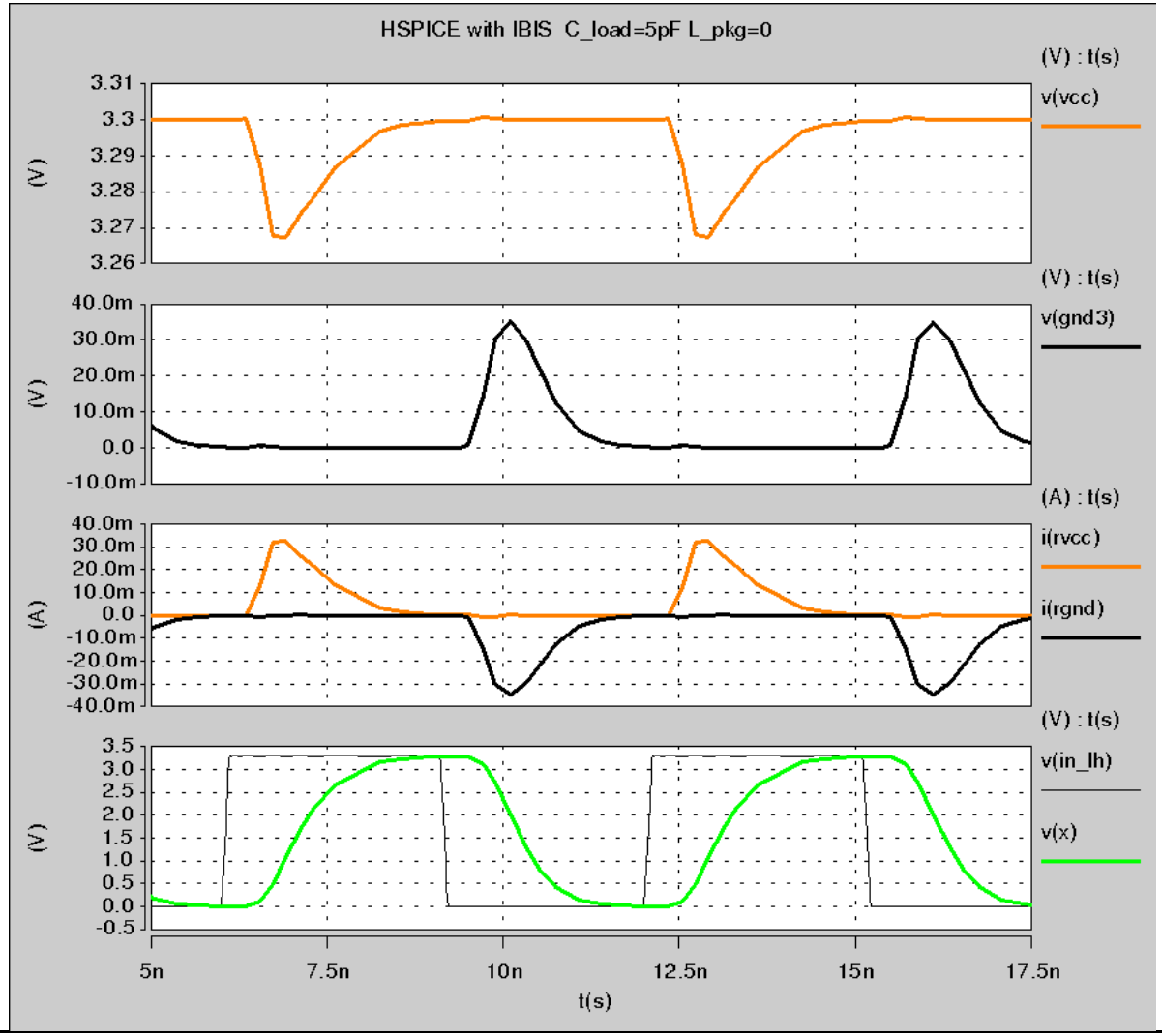
Vdd

GND

I_vdd/I_gnd

Output



C_load=5pF

Vdd/GND-Current + Voltage drop

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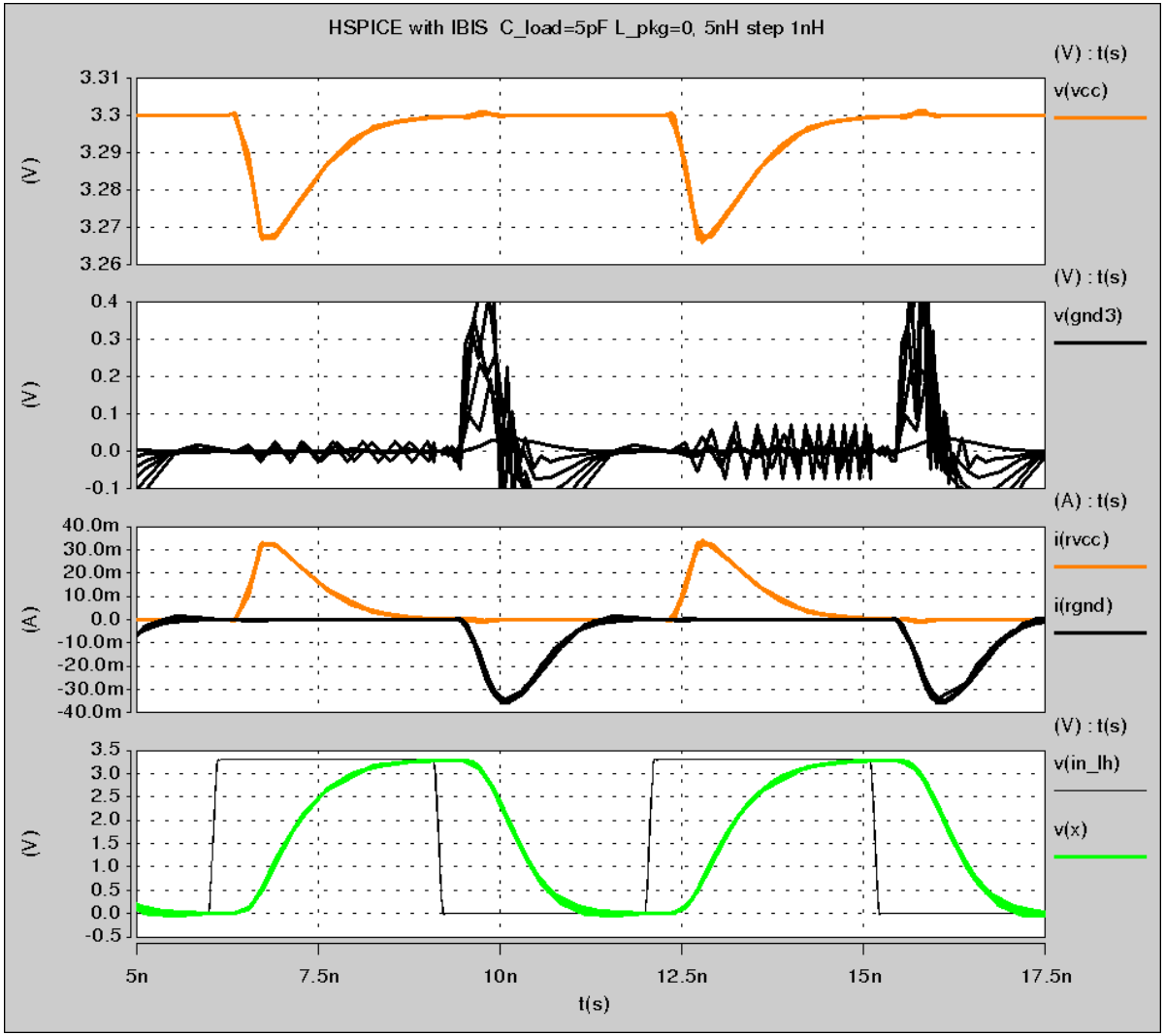
Vdd

GND

I_vdd/I_gnd

Output



C_load=5pF

L= 0…5nH

➔ NO ~~L

➔ NO time delay

Vdd/GND-Current + Voltage drop

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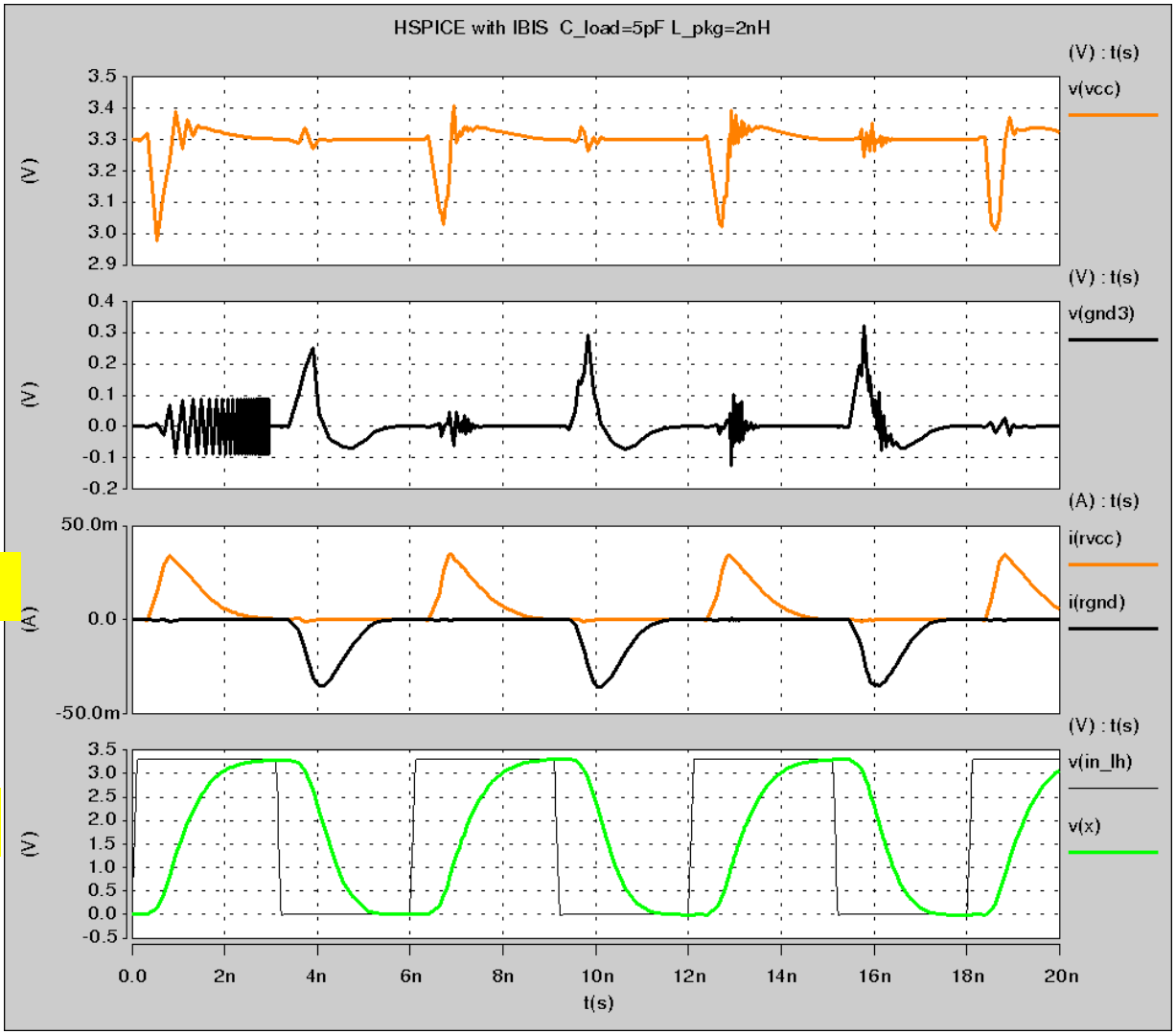
Vdd

GND

I_vdd/I_gnd

Output



C_load=5pF

L= 2nH

2 x SSO ➔ Voltage drop

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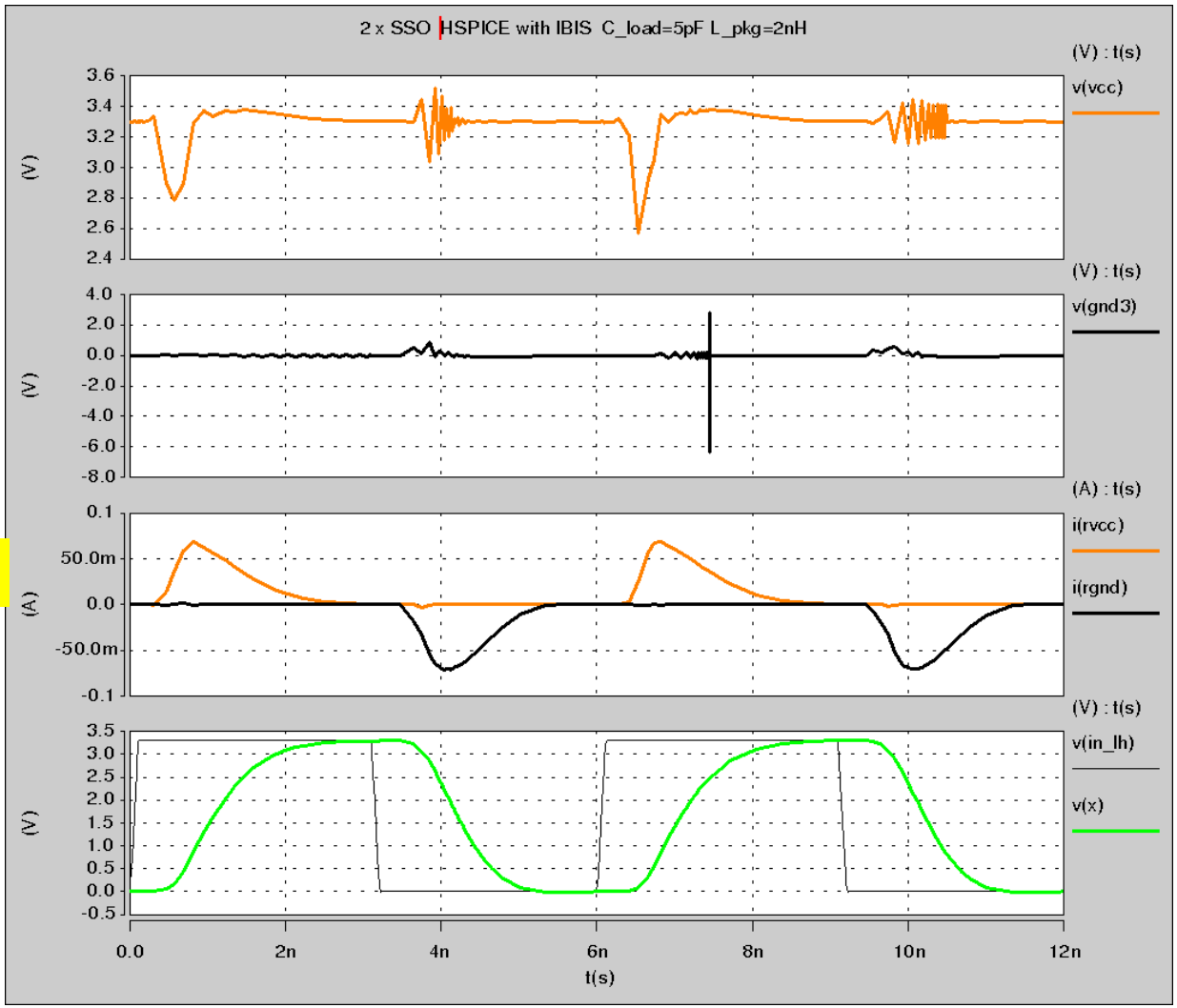
Vdd

GND

I_vdd/I_gnd

Output



C_load=0pF

L= 2nH

➔ math. artifacts

➔ oscillating

Conclusions

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IBIS models with required Keywords, only

➔ ➔ are not fitted for SSO simulation

- NO Timing Delay is obtained by SSO

- NO dependancy to the inductance of the PKG and PCB is included

- Mathmatical instabilities are very time consuming

Outlook

IF **SSO simulations with IBIS models,**

THEN **it is mandatory to have additional IBIS Keywords,**

as ISSO_pu and ISSO_pd

AND

Reasonable PKG and PCB models,

➔ ➔➔ Models extracted by 3-D Fieldsolver

Note: Unfortunately, IBIS models with ISSO_pu/pd are very rare,
and on the other side, the tool vendors are still waiting