IBIS MODEL FORMULATION AND EXTRACTION FOR SPI EVALUATION

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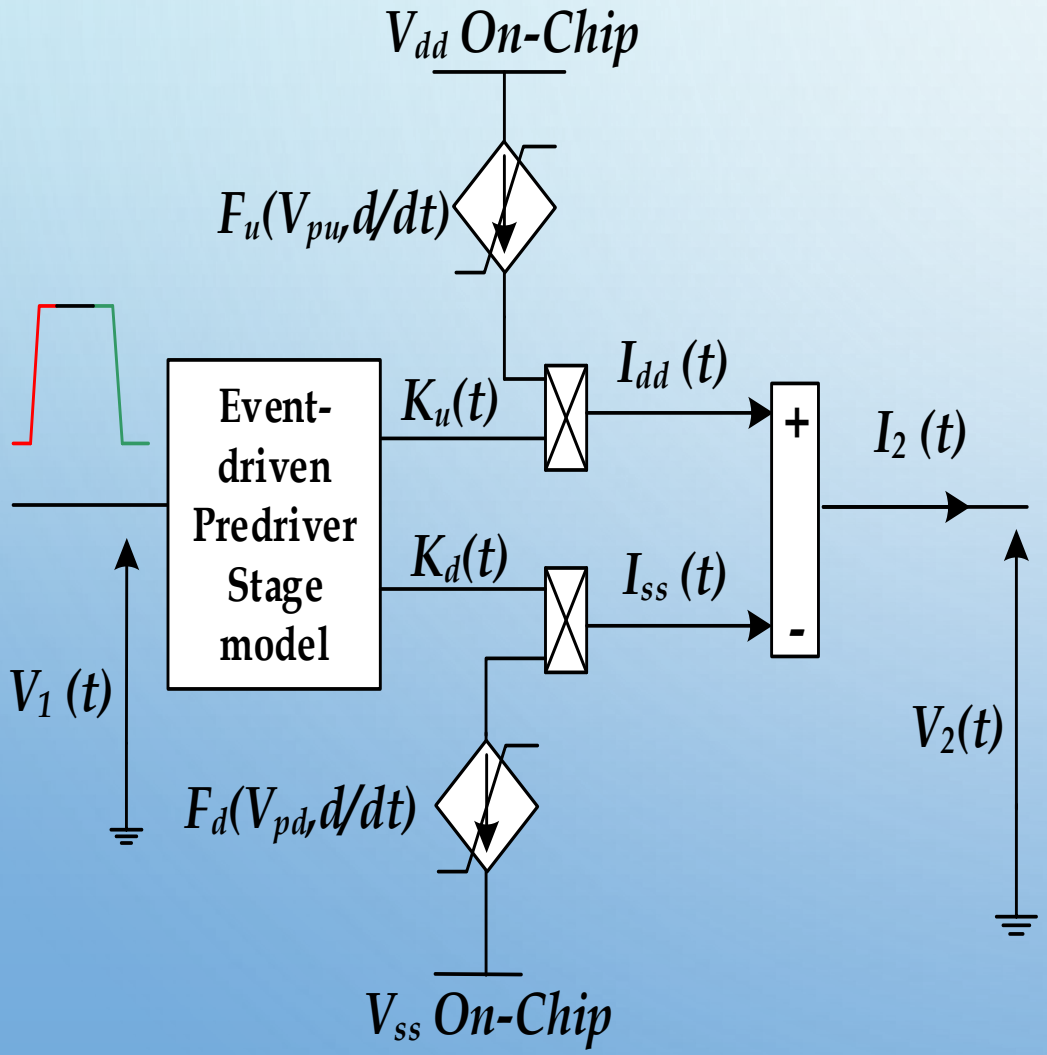
PRESENTATION OUTLINES

IBIS STATIC EXTENSION : BIRD-98,3

- ✓ Driver's IBIS model element for the pull-up (PU) and pull-down (PD) network.



- ✓ Extracting the gate modulation effect functions:

$$G_{dd}(V_{dd}) = \frac{I_{dd}(V_{dd})}{I_{dd,sat}}$$

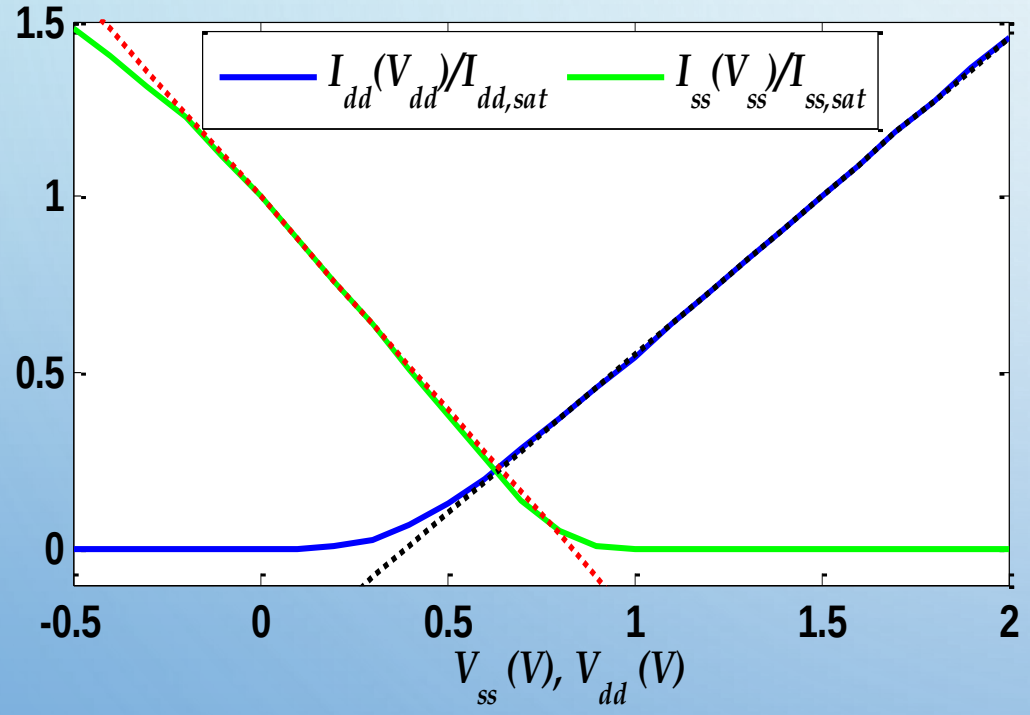
$$G_{ss}(V_{ss}) = \frac{I_{ss}(V_{ss})}{I_{ss,sat}}$$

- ✓ DC voltage sweep while the PU and PD are active and in saturation. The recorded output power and ground (PG) dc currents is then normalized to their saturation currents $I_{dd,sat}$ and $I_{ss,sat}$, respectively [3].

$$I_2(t) = K_u^n(t) \cdot G_u\left(V_{dd}(t)\right) \cdot F_u\left(V_{pu}(t), d/dt\right) + K_d^n(t) \cdot G_d\left(V_{ss}(t)\right) \cdot F_d\left(V_{pd}(t), d/dt\right) ; n = r, f$$

LINEAR INTERPOLATION THE G(•) FUNCTIONS

- ✓ Example of the $G(\cdot)$ functions extracted for the PU and PD networks and their linear interpolation (dashed line).



- ✓ First order interpolation of the nonlinear static (dc) part of the $F_u(\cdot)$ and $F_d(\cdot)$ functions

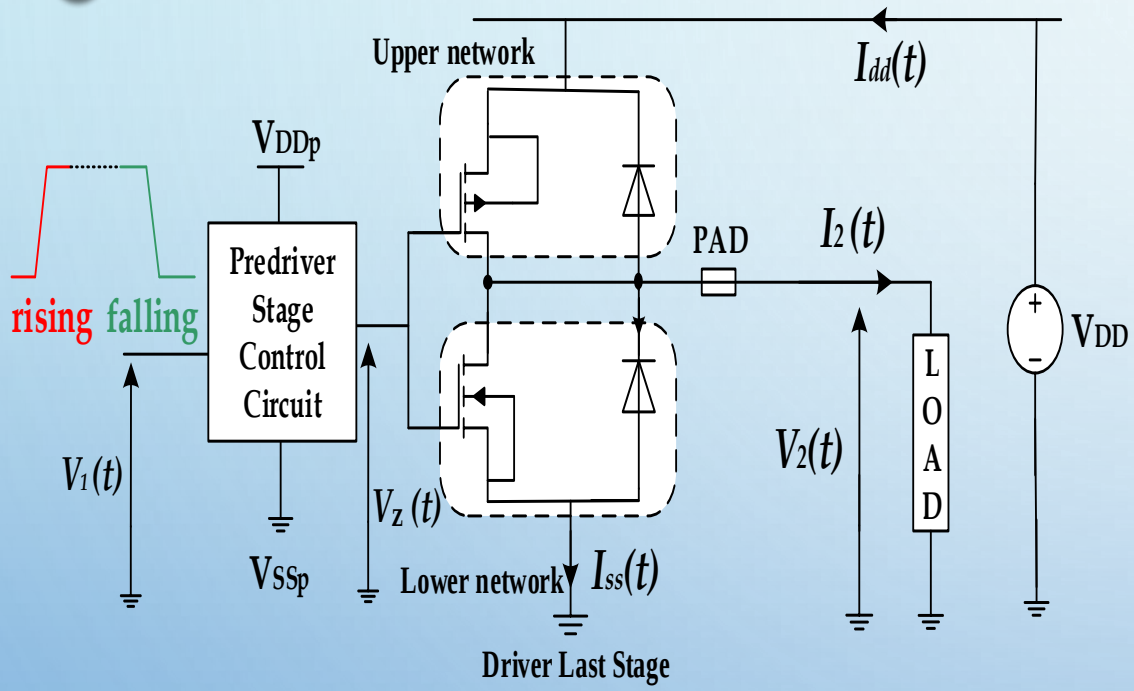
$$F_u^{dc}\left(V_1 = V_{DD}, V_{pu}(t)\right) \cong \frac{V_{dd}(t) - V_{DD2}}{V_{DD1} - V_{DD2}} \cdot F_u^{dc}\left(V_2(t), V_{DD1}\right) + \frac{V_{dd}(t) - V_{DD1}}{V_{DD2} - V_{DD1}} \cdot F_u^{dc}\left(V_2(t), V_{DD2}\right)$$

$$F_d^{dc}\left(V_1 = 0, V_{pd}(t)\right) \cong \frac{V_{ss}(t) - V_{ss2}}{V_{ss1} - V_{ss2}} \cdot F_d^{dc}\left(V_2(t), V_{ss1}\right) + \frac{V_{ss}(t) - V_{ss1}}{V_{ss2} - V_{ss1}} \cdot F_d^{dc}\left(V_2(t), V_{ss2}\right)$$

- The DC I-V curves of the $F_u^{dc}(.)$ for fixed V_{DD1} and V_{DD2} can be extracted directly from the (typ, min, max) corners in the IBIS model.
- Additional I-V curves can be added to the PD network for different V_{ss1} and V_{ss2} values to model the $F_d^{dc}(.)$.

IBIS DYNAMIC EXTENSION : BIRD-95.6

✓ Simulation setup for the power current I-t measurements $I_{com}^{dyn}(t) = I_{dd}^{TL}(t) - I_{dd}^{IBIS}(t)$



✓ RLC impedance extracted through AC sweep while the driver's input is kept at *H* and *L* levels and driving the load (*c*).

✓ Three different loading conditions (load (a) 50Ω, load (b) $50\Omega + V_{DD}$, and load (c)1MΩ)

✓ BIRD 95.6 presents a correction term only for the power $I_{dd}(t)$ current and has overlooked the ground $I_{ss}(t)$ current.

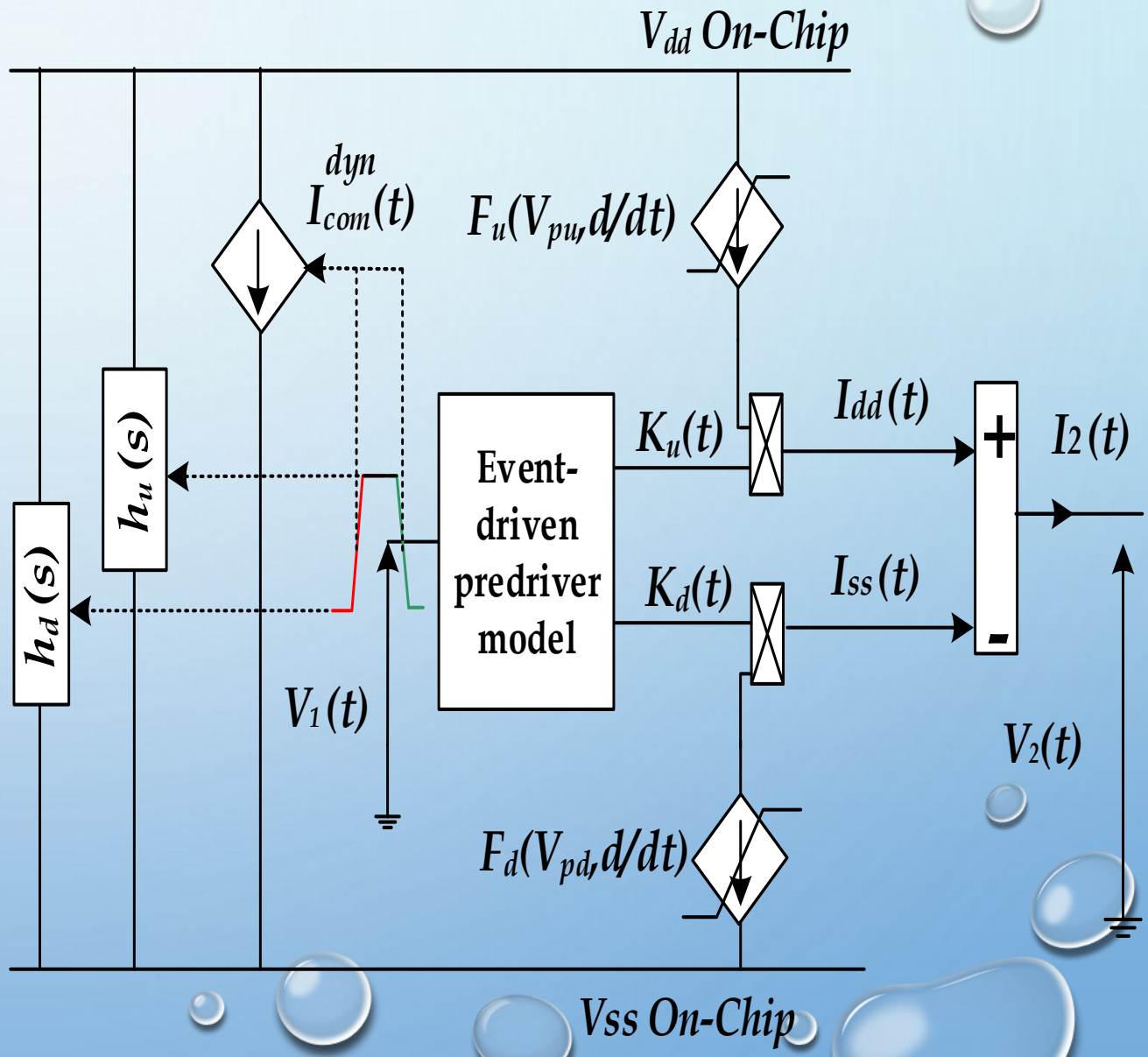
✓ The six $I_{com}(t)$ currents, in fact, model both the missing dynamic current at the PU and PD devices ($I_{dd}^{dyn}(t) - I_{ss}^{dyn}(t)$) which leads to an incorrect formulation for predicting the ground currents and therefore the $V_{ss}(t)$.

IBIS BIRD 95.6 MODEL IMPLEMENTATION

- ✓ RLC impedance can also be represented by the impulse response $h_u(t)$ and $h_d(t)$ between the PG ports (e.g. $p(t) = V_{dd}(t) - V_{ss}(t)$).

- ✓ The BIRD 95.6 implementation is illustrated in this Figure [6] and formulated in the time domain as follows:

$$I_2(t) = K_u^n(t) \cdot F_u\left(V_{pu}(t), d/dt\right) + \int_0^{+\infty} h_u(t-\tau) \cdot p(\tau) d\tau + \int_0^{+\infty} h_d(t-\tau) \cdot p(\tau) d\tau + K_d^n(t) \cdot F_d\left(V_{pd}(t), d/dt\right) + I_{com}^{dyn,n}(t);\ n = r, f$$

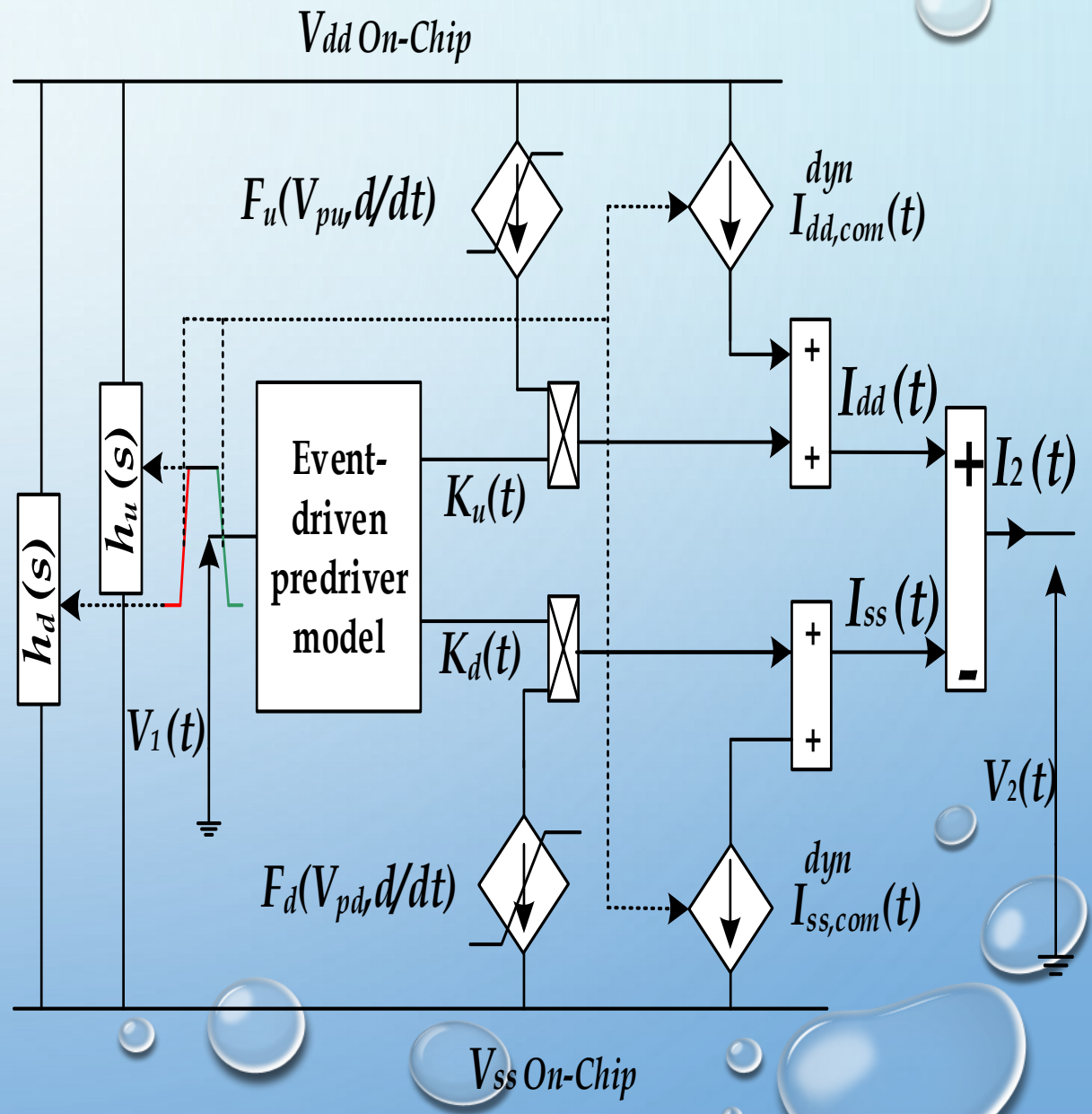


CORRECTED IBIS BIRD 95.6 IMPLEMENTATION

- ✓ A more consistent model extraction and formulation should consider a timing current correction terms for both the PU and PD networks, respectively.

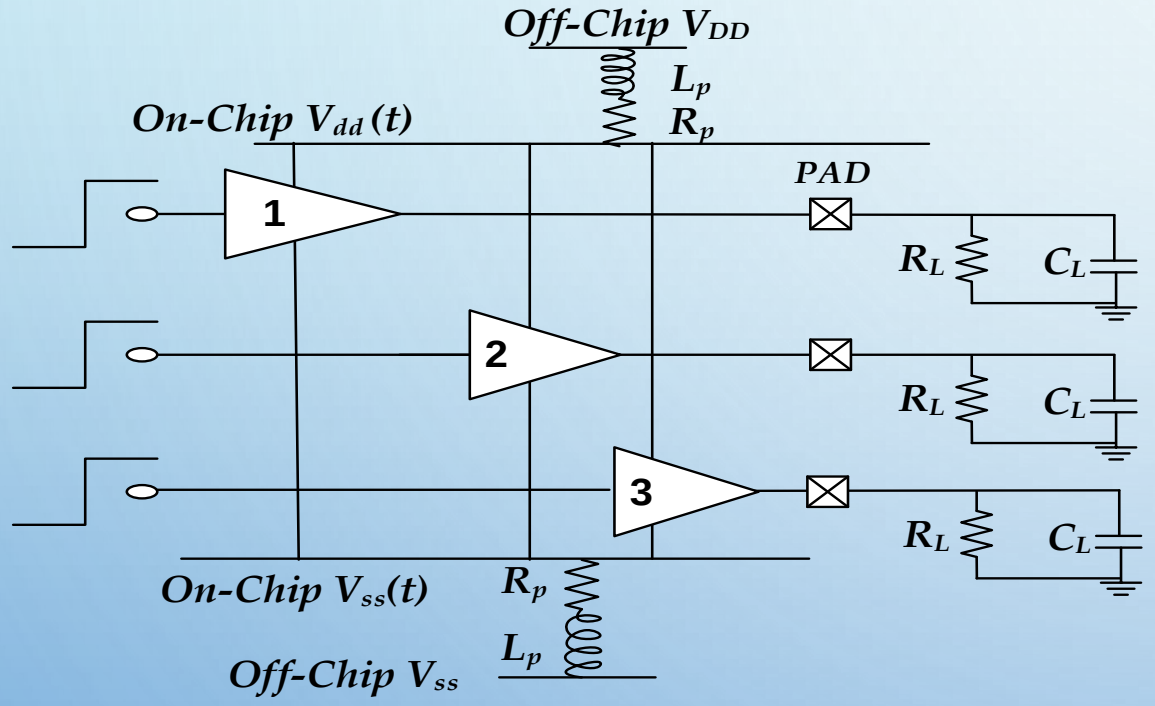
$$\begin{cases} I^{\,dyn}_{dd,com}(t) = I^{TL}_{dd}(t) - I^{IBIS}_{dd}(t) \\ I^{\,dyn}_{ss,com}(t) = I^{TL}_{ss}(t) - I^{IBIS}_{ss}(t) \end{cases}$$

- ✓ more six I-t curves should be extracted and included to compensate the missing dynamic current, $I^{\,dyn}_{ss,com}(t)$, at the ground node.



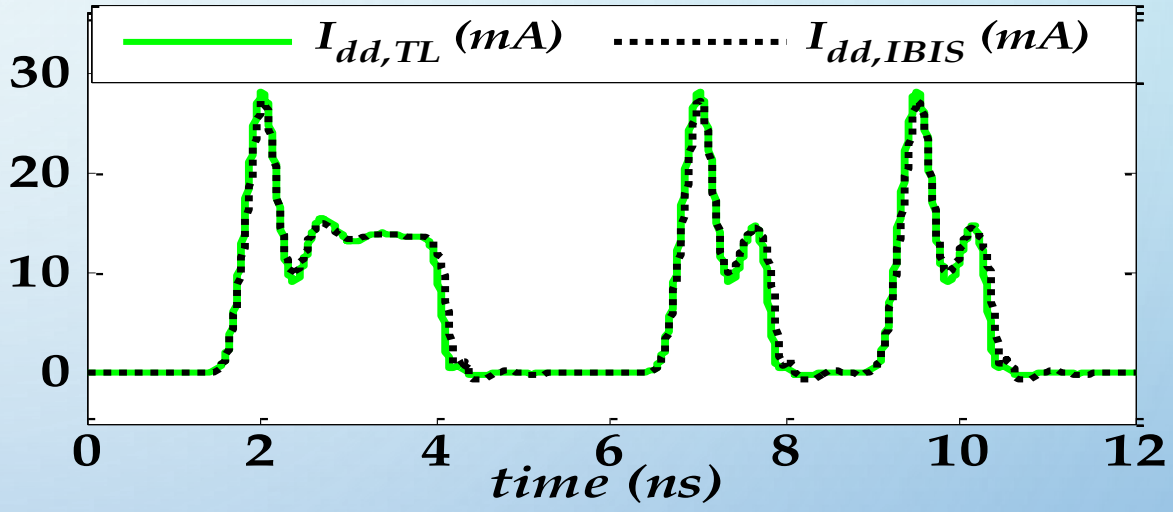
MODEL NUMERICAL RESULTS

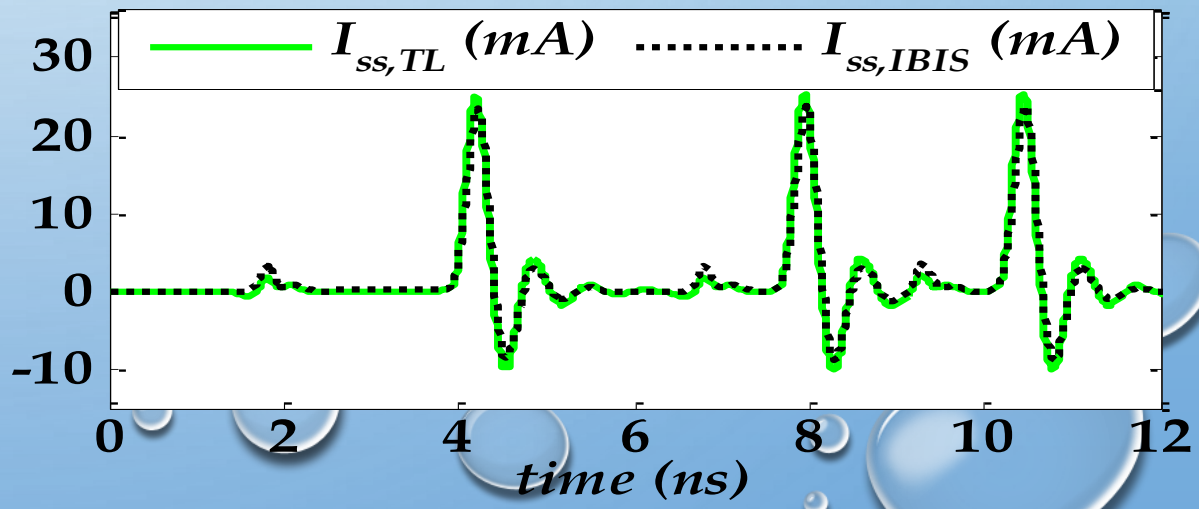
- ✓ Validation Setup with three simultaneously switching output buffers



The single driver is designed as a four cascaded inverter with increasing driving capability based on CMOS fully depleted silicon on isolator (FDSOI) technology at 28nm node from STMicroelectronics

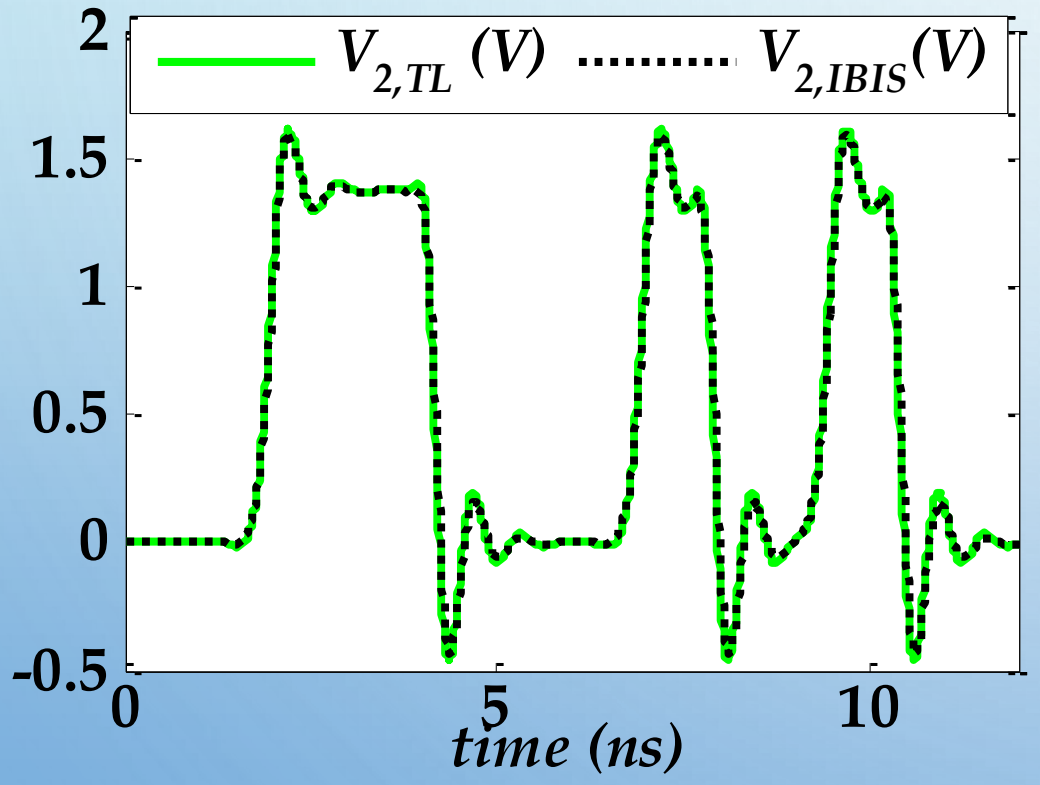
- ✓ Comparison between model's prediction of the $I_{dd}(t)$ and $I_{ss}(t)$





MODEL SIMULATION PERFORMANCE

- ✓ Comparison between model's prediction of the output voltage $V_2(t)$ at the first output pin.



- ✓ Performance of the Transient Simulation of the proposed Model in the validation setup

Model	$NMSE_{V_{ss}}$	$NMSE_{V_{dd}}$	$NMSE_{V_2}$	CPU time
Transistor Level	-	-	-	95.41 s
Proposed Model	-23.74 dB	-25.1 dB	-27.3 dB	39.76 s

- ✓ The accurate prediction of the output pin voltage of the first driver is illustrated in this figure. As seen from Table, the developed model speed-up the simulation by 58.33% while keeping acceptable NMSE around -25 dB.

For more results and explanation please see the paper [1]:

[1] W. Dghais, J. Rodriguez "IBIS Model Formulation and Extraction for SPI Evaluation", IEEE workshop on signal and power integrity (SPI), Berlin, Germany, May 2015.

CONCLUSIONS

- ✓ This paper has proposed a complementary extension of the previous IBIS model for SPI evaluations based on BIRDs 95.6 and 98.3.
- ✓ The proposed extraction procedure simplifies the static gate modulation effect and extend the dynamic PG timing I-t, and merges this with the V-t characterization.
- ✓ The accuracy and computational efficiency of the resulting model was analyzed.
- ✓ The achieved results confirm the validity of this method for modelling PG bouncing under the SSO scenario.
- ✓ A slight modification of the two-port characterization procedure of the IBIS model by measuring the $I_{dd}(t)$ and $I_{ss}(t)$ currents instead of $I_2(t)$ will merge both characterization setups for both V-t and I-t waveform extractions in a single step.

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