Interconnect Modeling Update - EMD Specification

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Outline

- EMD Specification
  - Overview
  - Draft 8 status
  - Syntax examples
  - Issues to resolve
  - Work in progress

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EMD Specification Overview

- EMD – Electrical Module Description
  - Describes electrical connectivity between and within modules
  - What are modules?
    - MCMs (multi chip modules), DIMMs, connectors, cables, packages, on-die interconnect
  - Supports connecting components in IBIS files and connecting to other EMD files
  - Future alternative to IBIS-EBD

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EMD Specification Overview

- EBD (Electrical Board Description)
  - Uncoupled paths, non-lossy, limited topology descriptions
  - Compact model within one file still ok for low frequency applications
- EMD Advantages
  - Uses subcircuits defined by IBIS-ISS
  - Direct support for Touchstone files
  - Supports coupled, broadband, lossy models
  - Parameter passing for corner case analysis
  - Simplified parameter tree structure (variant of IBIS-AMI)
    - Easy to parse and expand

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EMD Draft 8

- Draft 8 released May 3, 2013
  - http://www.eda.org/ibis/interconnect_wip/EMD_Draft_8.pdf
  - Work in progress
  - Recent progress includes:
    - Syntax cleanup
    - Expansion of some Leaf and Branch descriptions
    - Added External_Designators Branch for modules that have two or more external connection designators (e.g. cables)

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EMD Syntax

- Root Definition – Root name of the EMD
- Header_Information Branch
  - Required Leaves are EMD_Version, File_Name, File_Rev
  - Optional Leaves are Manufacturer, Date, Source, Notes, Disclaimer, Copyright

```
(RDIMM
  (Header_Information
    (EMD_Version 1.0)
    (File_Name rdimm.emd)
    (File_Rev 1.0)
    (Manufacturer "Number One DRAM Corp.")
    (Date 4/01/2013)
    (Source "From 2D EM field solver simulation at Number One DRAM Corp.")
    (Notes "Rev. 1.0")
    (Disclaimer "This information is for modeling purposes only and is not guaranteed.")
    (Copyright "Copyright 2013, Number One DRAM Corp., All Rights Reserved")
  )
```


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EMD Syntax

- External_Pin_List Branch
  - Contains Leaves defining the module's external pins

```
(External_Pin_List
   (1 VCC)
   (2 DQ0)
   (3 A0)
   (4 VSS)
   (5 VTT)
)
```

- Reference_Designators Branch
  - Contains Leaves defining reference designators of each module and component

```
(Reference_Designators
   (U1  (Type EMD)  (File ddr3_twindie.emd))
   (U2  (Type EMD)  (File ddr3_twindie.emd))
   (U3  (Type IBIS)  (File reg.ibs)  (Component Register))
)
```


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EMD Syntax

- Connections Branch
  - Contains Leaves defining the related connections between external pins and internal component and module pins
  - Also known as Extended Nets in some EDA tools

```
(Connections
   (VCC    1  U1.A1 U1.A3 U2.A1 U2.A3 U3.G6 U3.B6)
   (DQ0    2  U1.B3 U2.B3)
   (A0     3  U3.F7)
   (A0_post_reg U3.C2 U1.K3 U2.K3)
   (VSS    4  U1.A2 U1.A4 U2.A2 U2.A4 U3.G5 U3.B5)
   (VTT    5)
)
```


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EMD Syntax

- Interconnect Branch
  - Contains Branches defining Model Interconnect Protocols (MIP) for IBIS-ISS subckts or Touchstone files
  - Each MIP might describe:
    - single, uncoupled net
    - differential net
    - group of coupled signal nets
    - supply connection
    - group of supply connections
    - group of supply and signal connections
  - A connection may appear in one or more Interconnects

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EMD Syntax

- Interconnect Branch

```
(Interconnect
  (DQ0
    (IBIS_ISS_File RDIMM_subckts.iss)
    (IBIS_ISS_Circuit DQ0_net)
    (Parameters
      (Length1 3.3)
    )
    (Ports
      (1 2)       | Edge connector DQ0 pin
      (2 U1.B3) | DRAM U1 DQ0
      (3 U2.B3) | DRAM U1 DQ0
    )
  )
)
```

```
(Interconnect
  (A0_post_reg
    (IBIS_ISS_File RDIMM_subckts.iss)
    (IBIS_ISS_Circuit A0_post_reg_net)
    (Parameters
      (Rtt (Corner 36 39.6 32.4))
    )
    (Ports
      (1 U3.C2) | Register A0 output
      (2 U1.K3) | DRAM U1 A0 input
      (3 U2.K3) | DRAM U2 A0 input
      (4 5)       | VTT
    )
  )
)
```

  - Tstonefile is alternate Branch instead of IBIS_ISS_File
  - Parameters can include Corners Branch
  - Parameters not allowed for a Tstonefile Branch

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EMD Syntax

- Supply Branch
  - Contains Branches defining the names and voltage values of supply connections to the module
  - Corners may be defined
  - EDA tool may use the value as voltage supplied to the EMD or may connect external pins of supply connection to an external power distribution circuit

```
(Supply
   (VCC   (Corner 1.5 1.425 1.575))
   (VSS   0)
   (VTT   (Corner 0.75 0.7125 0.7875))
)
```


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Issues to Resolve

- Connector modeling including pin syntax (A.1, B.1)
- Overlapping Interconnect MIPs
  - How does an EDA tool choose the desired MIP Branch if a net is included in multiple MIPs (coupled vs. uncoupled)?
  - Terminations of unused ports in Touchstone files
- Parameterizing include files
  - May be useful addition for corner case models
- Can EMD be extended into the IBIS realm of packaging and on-die interconnect modeling?

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Work in Progress

- Interconnect task group meets Wednesdays, 8:00am PT
- Draft documents and presentations at:
  - http://www.eda.org/ibis/interconnect_wip/
- Are we covering your interconnect modeling needs?
  - If not, let us know!
  - Join the task group or send an email to ibis-interconn@freelists.org

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References

- Draft 8 of the EMD Specification
  - http://www.eda.org/ibis/interconnect_wip/EMD_Draft_8.pdf
- 2013 DesignCon IBIS Summit presentation by Walter Katz, "Interconnect Modeling Status"
  - http://www.eda.org/ibis/summits/jan13/katz.pdf
- Freelists email archive for IBIS Interconnect task group
  - http://www.freelists.org/archive/ibis-interconn

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