European IBIS Summit Meeting

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Thévenin's theorem revisited.

A new approach to IC buffer modeling and it's relation to IBIS

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Outline

- Context
- Building a nonlinear Thévenin-like model for IC buffers
- Demonstrating the approach on a TI driver
- Showing the mathematical relation between the new method and IBIS
- Conclusion

Context

Joint research on buffer modeling

Politecnico di Torino, Italy and Université de Brest, France

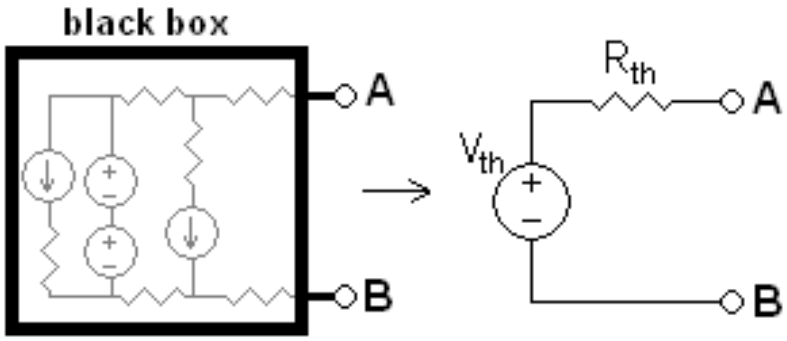
Focus:

- New methodologies and approaches to IC buffer macromodeling
- Better accuracy in critical conditions, more general approach to modeling

Nonlinear Thévenin-like model

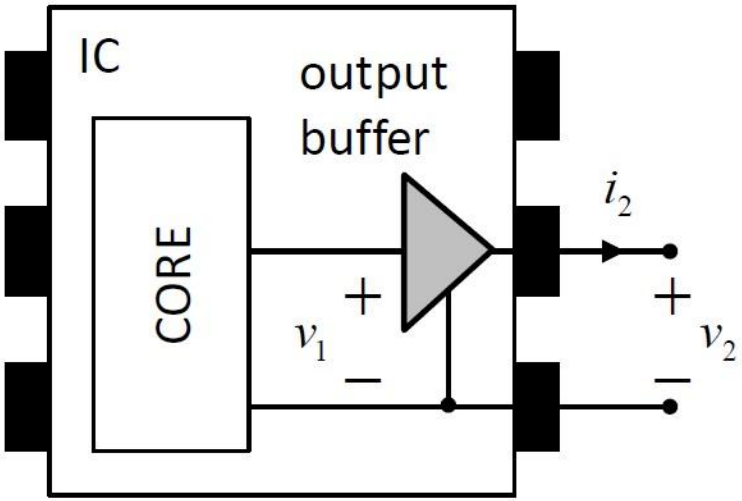
Thévenin's theorem for a linear two-port

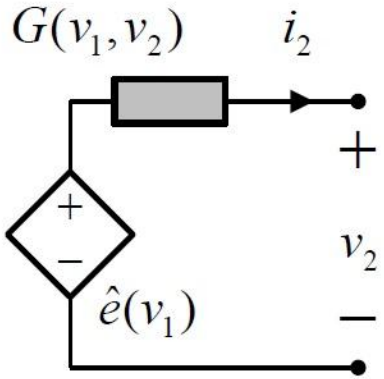
Léon Charles Thévenin (1857-1926)



Nonlinear Thévenin-like model

…adapting the idea to model a single ended driver



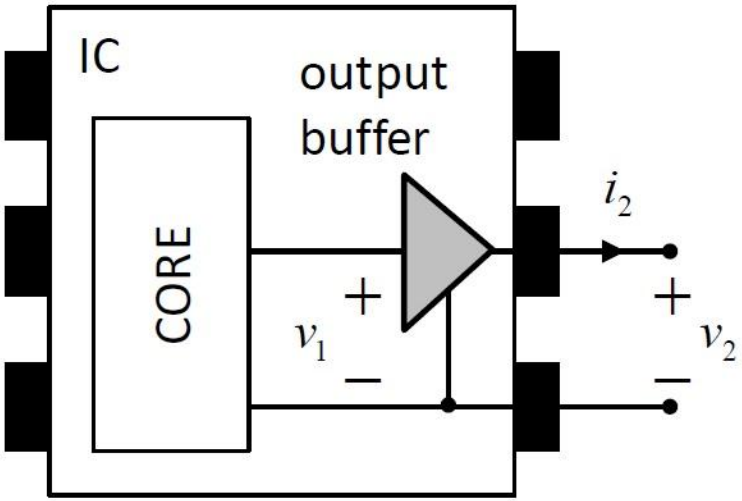


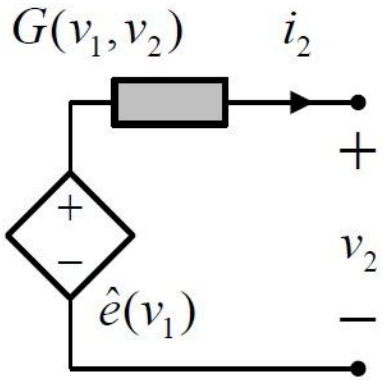
Objectives:

- Show that the structure constitutes a reasonable choice
- Show that the resulting model is mathematically related to IBIS

Nonlinear Thévenin-like model

…adapting the idea to model a single ended driver



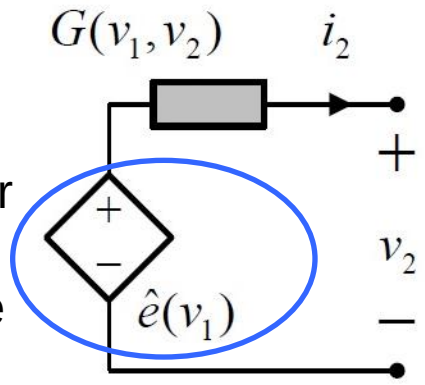


Example: Texas Instruments driver
SN74ALVCH16973, VDD = 2,5V

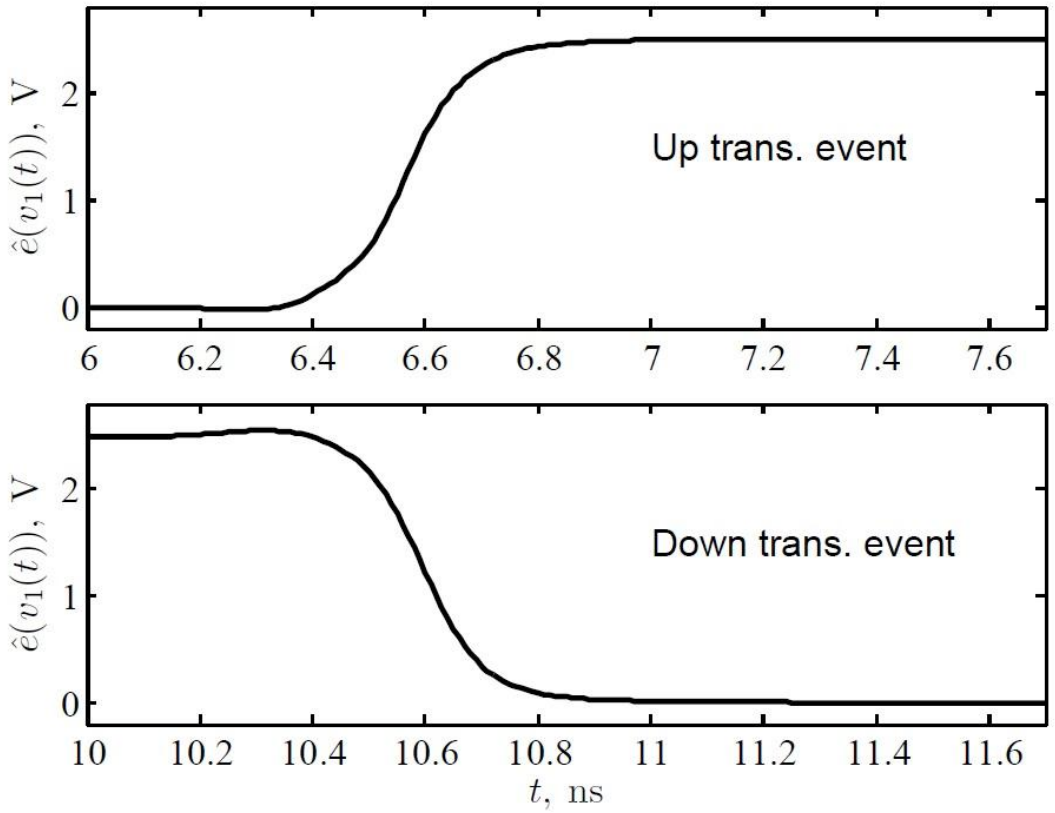
Nonlinear Thévenin-like model

OPEN CIRCUIT VOLTAGE

- Single-input-single-output nonlinear element
- Gives the input-output characteristic of the driver
- Can be modeled in different ways
- Considered an independent voltage source here
- Will be discussed further on in relation to IBIS



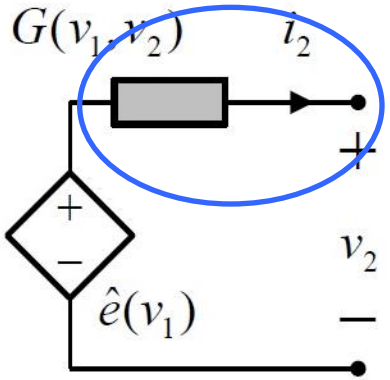
Nonlinear Thévenin-like model



Nonlinear Thévenin-like model

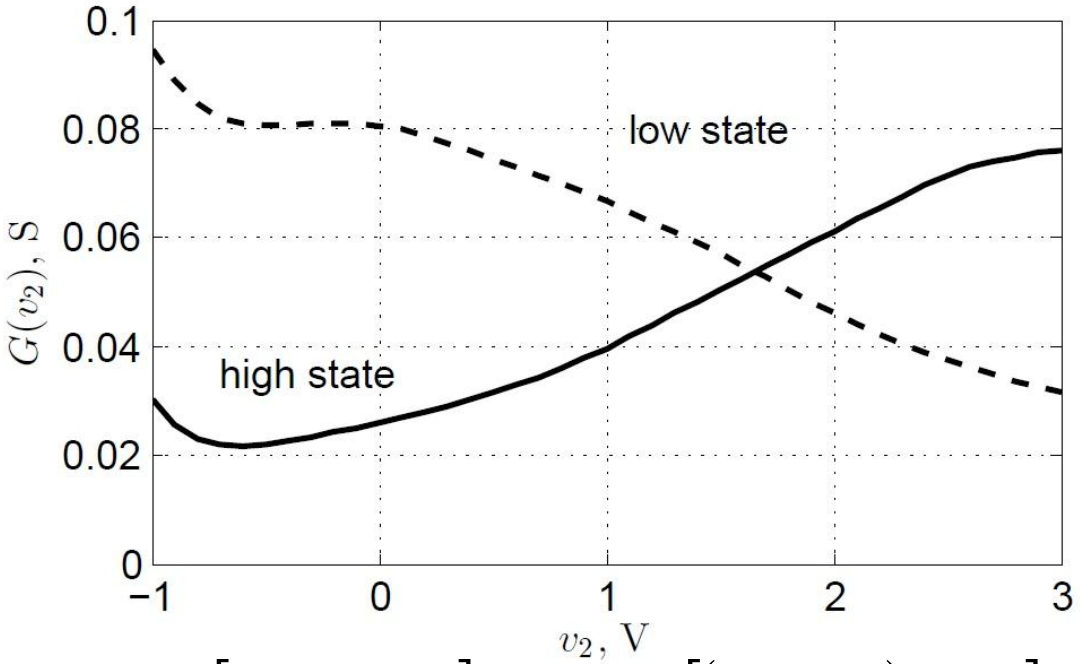
Nonlinear conductance

- On state / off state separation
- Static table based model at this stage



$$G(v_1, v_2) = \left[\hat{e}(v_1)/V_{DD}\right] G_H(v_2) + \left[\left(1-\hat{e}(v_1)\right)/V_{DD}\right] G_L(v_2)$$
$$= \tilde{w}_H G_H(v_2) + \tilde{w}_L G_L(v_2)$$

Nonlinear Thévenin-like model



$$G(v_1, v_2) = \left[\hat{e}(v_1)/V_{DD}\right] G_H(v_2) + \left[\left(1-\hat{e}(v_1)\right)/V_{DD}\right] G_L(v_2)$$
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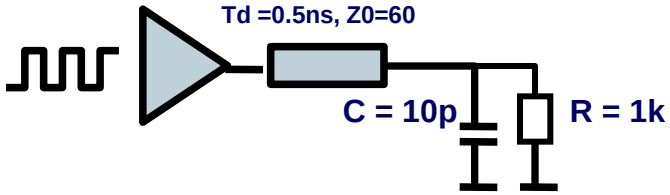
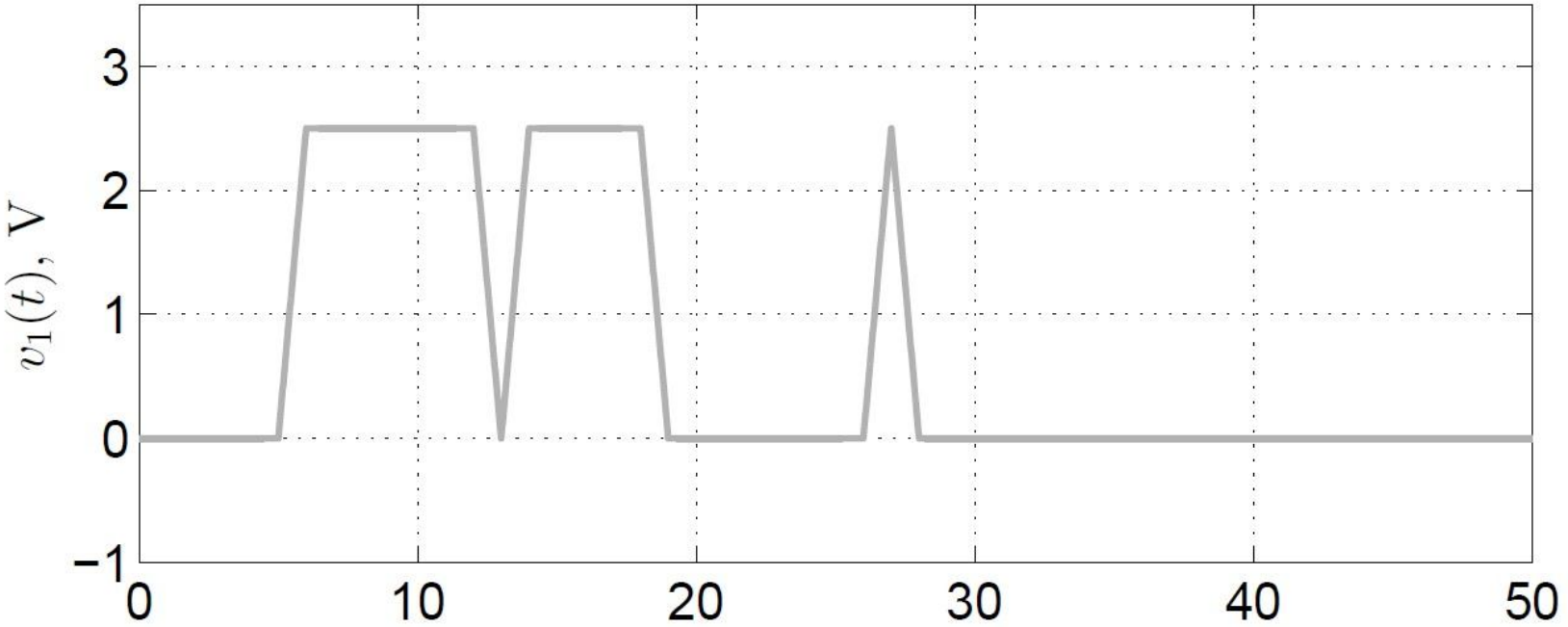
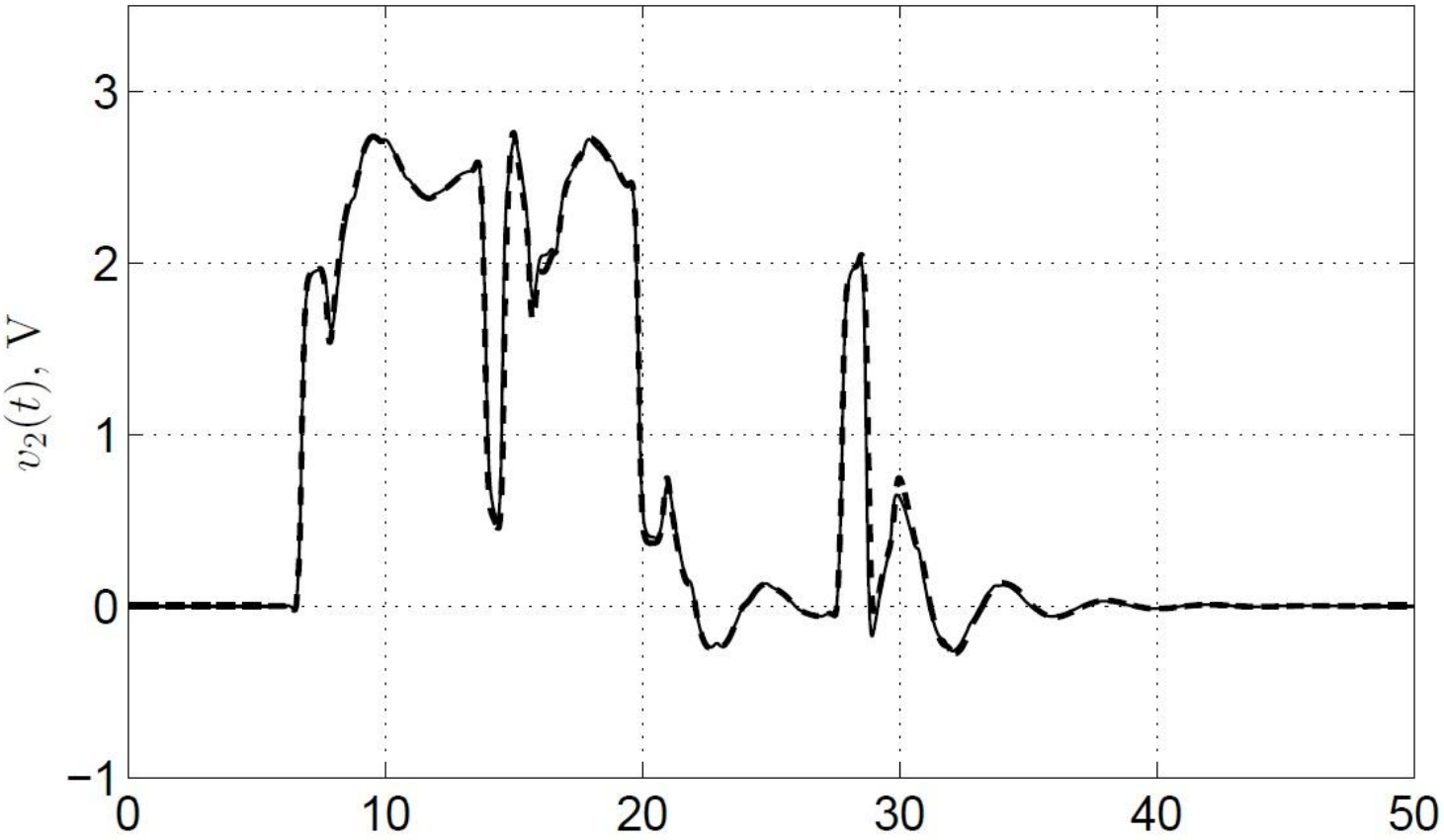
Transient simulation results

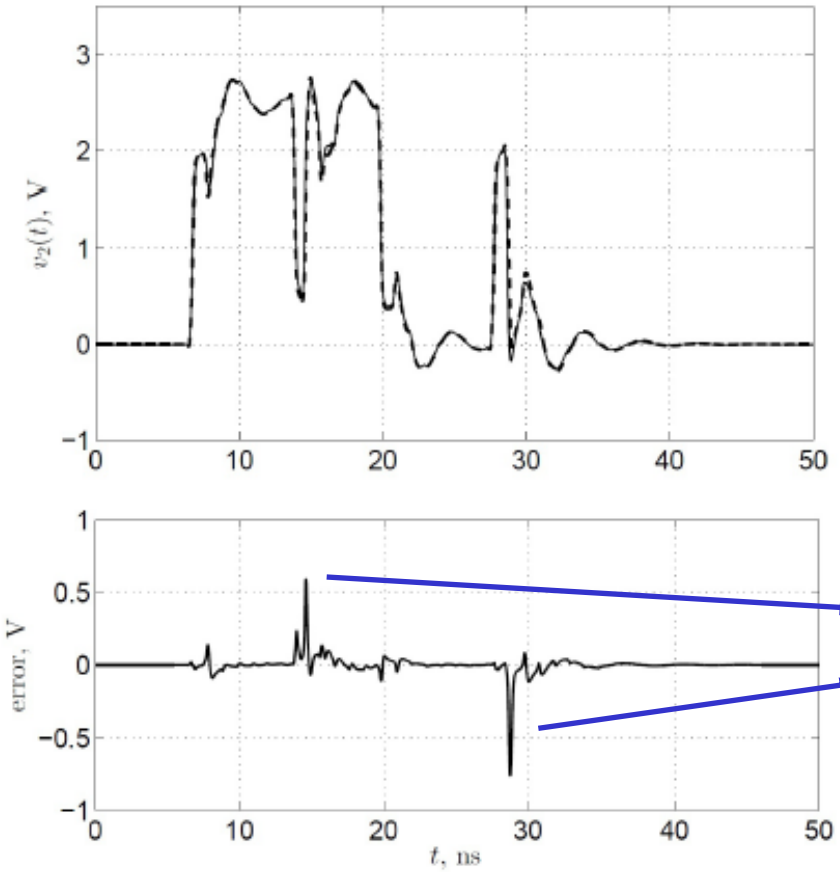




Transient simulation results



Transient simulation results



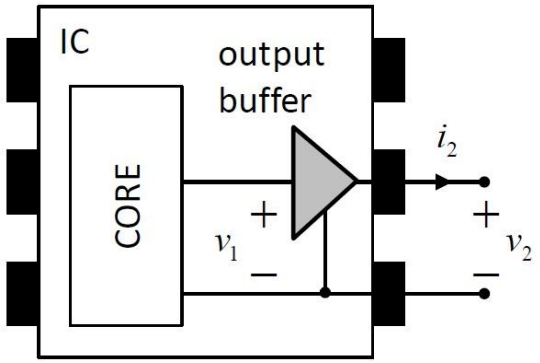
Device model	Memory	Speed-up
reference transistor-level	2092 kB	–
proposed model	303 kB	10×

Error due to edge misalignment during spurious events → can be compensated by a capacitance, simple FIR etc.

Relation with IBIS

Thévenin-like

$$i_2(t) = G(v_1, v_2)\left[\hat{e}(v_1) - v_2\right]$$
$$= \left[\left(\hat{e}(v_1)/V_{DD}\right)G_H(v_2) + \left(\left(1-\hat{e}(v_1)\right)/V_{DD}\right)G_L(v_2)\right]\left[\hat{e}(v_1) - v_2\right]$$
$$= \left[\tilde{w}_H G_H(v_2) + \tilde{w}_L G_L(v_2)\right]\left[\hat{e}(v_1) - v_2\right]$$
$$= \tilde{w}_H\left[\hat{e}(v_1) - v_2\right]G_H(v_2) + \tilde{w}_L\left[\hat{e}(v_1) - v_2\right]G_L(v_2)$$
$$= \tilde{w}_H\,\tilde{f}_H(v_1, v_2) + \tilde{w}_L\,\tilde{f}_L(v_1, v_2)$$



IBIS-like

$$i_2(t) = w_H\, f_H(V_{DD} - v_2) + w_L\, f_L(v_2)$$

- Static characteristics of the output port in high and low state
- Weighting functions computed from devices responses on two resistive loads

Relation with IBIS

Thévenin-like

$$i_2(t) = G(v_1, v_2)\left[\hat{e}(v_1) - v_2\right]$$
$$= \left[\left(\hat{e}(v_1)/V_{DD}\right)G_H(v_2) + \left(\left(1-\hat{e}(v_1)\right)/V_{DD}\right)G_L(v_2)\right]\left[\hat{e}(v_1) - v_2\right]$$
$$= \left[\tilde{w}_H G_H(v_2) + \tilde{w}_L G_L(v_2)\right]\left[\hat{e}(v_1) - v_2\right]$$
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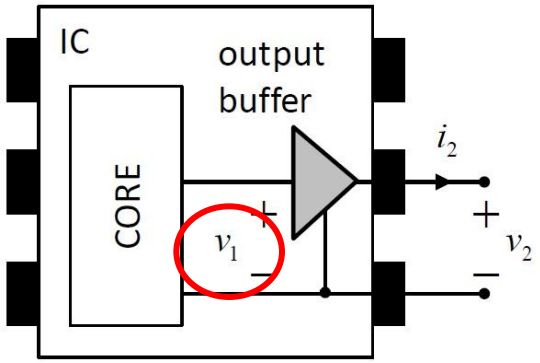
$$= \tilde{w}_H\,\tilde{f}_H(v_1, v_2) + \tilde{w}_L\,\tilde{f}_L(v_1, v_2)$$

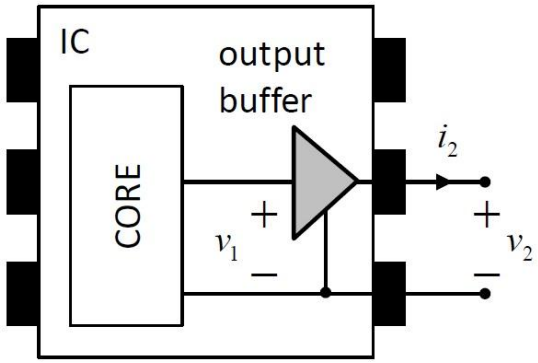


IBIS-like

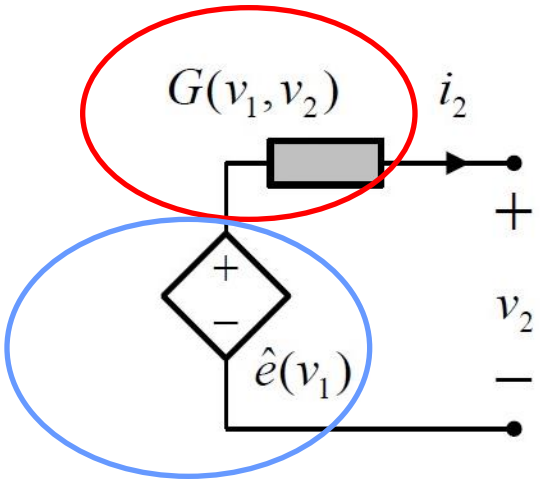
$$i_2(t) = w_H\, f_H(V_{DD} - v_2) + w_L\, f_L(v_2)$$

In the Thévenin-like model both $\tilde{w}_{H,L}$ and $\tilde{f}_{H,L}$ depend on v_1
In the IBIS-like model only $w_{H,L}$ depend on v_1

Summing things up…



Static table-based model here → dynamic models: compensation capacitance, linear FIR, nonlinear model if needed



Independent voltage source here → heuristic nonlinear model, polynomial Volterra-like filter, neural network etc.

Conclusions and future developments

- Top down approach: circuit theory → macromodel
- Basic building block for future EDA tools
- Enhanced models should account for circuit dynamics, V_{DD} variation, differential devices
- Good potential in solving inaccuracies related to jitter, overclocking, etc.