IBIS Open Forum Minutes

Meeting Date: **May 15, 2013**
Meeting Location: **SPI-E IBIS Summit, Paris, France**

VOTING MEMBERS AND 2013 PARTICIPANTS

Agilent	Radek Biernacki, Pegah Alavi, Heidi Barnes, Fangyi Rao, Colin Warwick, Tarun Kalwani
Altera	David Banas, Hsinho Wu
ANSYS	Luis Armenta, Ben Franklin*
Applied Simulation Technology	Fred Balistreri, Norio Matsui
ARM	(Vipul Patel)
Cadence Design Systems	Terry Jernberg, Joy Li, Yingxin Sun, Ambrish Varma, Kevin Yao, Brad Brim
Ericsson	Anders Ekholm*, Martina Fiammengo
Foxconn Technology Group	(Sogo Hsu)
Freescale	Jon Burnett
Huawei Technologies	(Jinjun Li)
IBM	Greg Edlund, Adge Hawes, Dale Becker*
Infineon Technologies AG	(Christian Sporrer)
Intel Corporation	Michael Mirmak, Mohammad Bapi, Stewart Gilbert, Ravindra Rudraraju
IO Methodology	Lance Wang*
LSI	Brian Burdick, Sarika Jain
Maxim Integrated Products	Hassan Rafat, Mahbubul Bari, Ron Olisar
Mentor Graphics	Arpad Muranyi, Ed Bartlett, Vladimir Dmitriev-Zdorov
Micron Technology	Randy Wolff*
Nokia Siemens Networks GmbH	(Eckhard Lenski)
QLogic	James Zhou
Signal Integrity Software	Walter Katz, Mike LaBonte, Mike Steinberger, Todd Westerhoff
Synopsys	John Ellis, Ted Mido, Scott Wedge, Rinsha Reghunath
Teraspeed Consulting Group	Bob Ross, Tom Dagostino
Texas Instruments	(Pavani Jella)
Toshiba	(Yasumasa Kondo)
Xilinx	(Raymond Anderson)
ZTE	(Huang Min)
Zuken	Masaud Raeisi, Reinhard Remmert, Michael Schaeder*, Alfonso Gambuzza*

OTHER PARTICIPANTS IN 2013

Bayside Design	Elliot Nahas
Computer Simulation Technology	Heiko Grubrich*
ECL Advantage	Thomas Iddings

Granite River Labs	Vamshi Kandalla, Miki Takahashi
Hewlett-Packard	Yongjin Choi, Ting Zhu
KEI Systems	Shinichi Maeda
Molex	Davi Correia*
National Instruments	Lee Mohrmann
Nvidia	Eric Hsu
Qualcomm	Scott Powers
TechAmerica	(Chris Denham)
Teradyne	Raymond Yakura
Université de Brest	Mihai Telescu*
University of Illinois	Tom Comberiate*, José Schutt-Ainé, Xu Chen*
Vitesse Semiconductor	Sirius Tsang

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
May 17, 2013	205 475 958	IBIS

For teleconference dial-in information, use the password at the following website:

https://ciscosales.webex.com/ciscosales/j.php?J=205475958

All teleconference meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The IBIS Open Forum Summit was held in Paris, France at the Hyatt Regency Paris Etoile hotel following the 2013 SPI conference. About 12 people representing 10 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda.org/ibis/summits/may13/

Lance Wang welcomed all the participants and thanked the co-sponsors Micron Technology and Zuken. He asked all the participants to introduce themselves. There were a wide variety of people from many countries and organizations including academia and industry.

IBIS MODELING FOR LOAD DEPENDENT CURRENT MODE DIFFERENTIAL DRIVERS

Lance Wang, IO Methodology, USA

Lance Wang began by showing details of the current flow in a load dependent current mode differential driver. He then showed the I-V and V-t curves extracted from the buffer Spice model while treating the buffer as two independent pins. The resulting correlation between IBIS and Spice results was very poor. Using an enhanced extraction method, taking into account a differential load, results in very different I-V and V-t table data and good correlation to Spice.

Lance concluded that the IBIS specification needs differential buffer models with Rref_diff and Cref_diff load information which is limited to [External Model] use now.

Dale Becker asked if this was a unique approach. Lance responded that he isn't seeing many load dependent current mode differential drivers yet. He added that the bias level seen on slide 4 can be changed to vary the common mode voltage level.

X2IBIS: USING X-PARAMETERS TO GENERATE IBIS MODELS

Tom Comberiate and José Schutt-Ainé*, University of Illinois at Urbana-Champaign, USA

Tom Comberiate began by noting that a motivation for using X-parameters to generate IBIS models is to be able to send a non-Spice buffer model to a third party IBIS model generator. X-parameters are large signal extensions of S-parameters that can describe non-linear effects and be measured with a NVNA. His starting point was a Spice netlist for a basic inverter. His goal was to generate X-parameters of this inverter, then convert them to I-V and V-t data in an IBIS file, excluding parasitics and clamps.

X-parameters are generated with a harmonic balance simulation, setting proper values for frequency range, fundamental power and DC bias. A low frequency output voltage sweep with the input bias at VCC and 0V, measuring current response results in an .xnp file for the I-V data. A high frequency input sweep with the output bias at VCC and 0V results in an .xnp file for the V-t data. Multiple frequencies in the V-t curve .xnp file could be included for varying rise/fall times of the input. Tom then performed harmonic balance simulations using the X-parameter data, using scattered and incident waves to calculate voltage and current needed for IBIS tables. The I-V curve generation results matched closely to the results from s2ibis. The V-t curve generation results were a reasonable match to s2ibis results.

Future work will include performing x2ibis on more complicated buffers, developing transient simulation techniques for use with .xnp files, and implementing power aware modeling techniques.

Anders Ekholm asked if Tom had done much to model inputs. Tom responded that he only has access to limited models, so he is only modeling a Tx so far. Anders noted that in addition to the comparison to s2ibis, he would like to see how x2ibis results correlate to the original Spice results. Tom added that x2ibis results were closer to Spice results. Lance Wang asked what the harmonics are in an .xnp file. Tom responded that they come from a harmonic balance simulation. Including more harmonics makes the solution a closer match to the original. Tom is also looking at how to use X-parameters directly with no translation to IBIS. He sees potential here.

THEVENIN'S THEOREM REVISITED. A NEW APPROACH TO IC BUFFER MODELING AND ITS RELATION TO IBIS

Igor Stievano*, Cherif Diouf**, Mihai Telescu**, N. Tanguy**, and Flavio Canavero*, *Politecnico di Torino, Italy; **Université Européenne de Bretagne, Université de Brest, France

Mihai Telescu presented a new modeling approach for IC buffers, building a nonlinear Thevenin-like model. The IC buffer is modeled as a nonlinear, independent voltage source in series with a nonlinear conductance. The G element is a static, table based model currently. Transient simulation results show a good match to Spice and a speed up of 10x. Mihai showed that there are similarities in the underlying equations used in IBIS simulation with the equations used in the Thevenin-like model. One difference is that the Thevenin-like model has extra dependencies on the input voltage stimulus. Mihai concluded that the enhanced models should account for circuit dynamics, power supply variation and differential devices. They also have good potential for solving inaccuracies related to jitter and overclocking.

Mahai described the definition of overclocking in response to a question from Dale Becker. Dale also asked if he was doing some sort of black box modeling. Mihai responded that this was correct. This approach has the potential for modeling more complex behaviors, such as adding temperature dependencies. Someone also asked what he meant by jitter. Mihai responded that misalignment of timing can come from having no information about input voltage in the output transfer function. Delay information can be fed into $\hat{e}(v_1)$.

BEHAVIORAL MODEL SOLUTION FOR DRIVER'S OVERCLOCKING SIMULATION

Wael Dghais, Universidade de Aveiro, Instituto de Telecomunicações, Portugal

Randy Wolff presented. He described how IBIS simulation equations include weighting functions derived from the V-t table data that attempt to describe the switching behavior of the pre-driver stage. The inputs to an IBIS driver model are based on concatenation of step input describing functions. It is hard to line these functions up properly, especially with overclocking, where the gate voltage on the driver stage does not reach steady state. The objective of Wael Dghais' work was to develop an effective large signal behavioral model for transient simulation under overclocking conditions.

Wael's model requires access to the output driver gate voltage. Ids versus Vgs characteristics of the final driver stage are captured. The pre-driver stage is modeled with a transfer function implementing delay and a low pass filter. The pre-driver circuit naturally acts as a low pass filter, attenuating higher frequencies of the input waveform. This makes the output signal mostly

independent of the rise/fall times of the input signal. Under severely overclocked conditions, the new model shows much better correlation to the Spice model than the IBIS model.

Michael Schaeder wondered how the implementation of the new model compares to IBIS. IBIS implementation is up to the EDA software, so he would like to see more details of how this model could be implemented in software tools.

Mihai Telescu noted that other modeling approaches besides IBIS such as Mpilog can have advantages over IBIS in some situations. Some discussion of overclocking issues ensued, and Randy noted that handling of overclocking is not defined in the IBIS specification, so overclocking algorithms are EDA tool independent.

Randy noted that this modeling technique requires access to the gate node of the driver. This is a deviation from IBIS, since this node cannot typically be measured physically. So, this modeling approach can only come from simulation.

Further discussion on overclocking led to the comment from Michael Schaeder that it would be nice to have specific recommendations in the IBIS specification or cookbook for how to trim V-t data tables.

Mihai commented that maybe IBIS could be expanded to have a three dimension table to understand the delay through the pre-driver, such as voltage versus time versus delta time.

Anders Ekholm wondered if the pre-driver and driver sections of a typical buffer could be modeled in IBIS through two cascaded IBIS models, one for the driver and one for the pre-driver.

TABLE-BASED EXTRACTION FOR MODELING DRIVER'S OUTPUT ADMITTANCE
Wael Dghais, Universidade de Aveiro, Instituto de Telecomunicações, Portugal

Randy Wolff presented. He noted that Wael Dghais' objective in this modeling work was to develop an extraction process to create an effective large-signal behavioral model of a driver stage. Under a pulse excitation of the output driver, the Ids-Vds curve shows a looping characteristic. This indicates a voltage-dependent capacitive effect in the driver. This effect can be modeled with an output impedance I-Q model. At a constant input voltage, the output buffer can be considered as a one-port voltage-controlled device. It consists of the parallel connection of a static non-linear conductance and a non-linear static charge representing the conduction and displacement current in the driver, respectively. The I-Q model formulation is suitable for modeling MOSFET transistors and diodes.

The new extraction procedure relies on the linear least-squares method. Theoretically, two independent measurements are required to extract the Cj and Gj functions. Nevertheless, it is possible to extract the two unknowns by means of only one transient measurement, detailed in the presentation. The switching characteristics of the model are extracted using a similar procedure to IBIS models, where weighting functions are extracted from V-t switching data. Examples of the conduction and displacement curves for the pullup and pulldown devices of the driver's last stage were shown. Validation results showed very good agreement between the Spice model and the I-Q model. The proposed formulation was more accurate than the IBIS model for the same level of computational complexity.

Anders Ekholm commented that this looked like a good improvement for C_comp modeling. He would like to see a partnership with an EDA vendor to look further into implementing this modeling approach in IBIS.

INTERCONNECT MODELING UPDATE – EMD SPECIFICATION
Randy Wolff, Micron Technology, USA

Randy Wolff presented an update on the EMD specification being developed by the Interconnect task group. EMD is Electrical Module Description, a specification to describe electrical connectivity between and within modules such as DIMMs, MCMs, connectors, cables, packages and on-die interconnect. EMD is a future alternative to IBIS-EBD. Advantages of EMD include allowing the use of IBIS-ISS to model subcircuits and direct support for Touchstone files. Randy presented examples of the current syntax from draft 8 of the specification. The syntax uses a simplified parameter tree structure that is easy to parse and expand.

There are several issues to resolve in subsequent drafts of the specification. These include connector model syntax, suggestions for EDA tool handling of subcircuit selection when a net is included in multiple coupled and uncoupled subcircuits, terminations of unused ports in Touchstone files, parameterization of include files, and extension of EMD for modeling packaging and on-die interconnect.

Alfonso Gambuzza asked why the EMD specification is using the parameter tree syntax. There is a large ecosystem existing to support other syntaxes such as XML or Relax NG. Why define something new? Anders Ekholm asked if there was a way to parse IBIS with RNG. Alfonso did not know if this existed.

Michael Schaeder asked what the three corners mean for interconnect modeling. Randy responded that they could be defined in several ways, and these corners do not relate to corners in IBIS models. Michael commented that the specification should clearly define the use of corners. It would also be nice to include a built-in capability for setting corners up for worst-case. Randy commented that this would be somewhat like dependency tables in IBIS-AMI.

Alfonso commented that the ability to replace subcircuits easily for what-if analysis would be useful. Randy questioned if parameterizing include files could address this capability.

IBISCHK5 SPECIFICATION AND PARSER
Bob Ross* and Mike LaBonte**, *Teraspeed Consulting Group and **Signal Integrity Software (SiSoft), USA

Anders Ekholm presented. Bob Ross and Mike LaBonte are working on a specification document for the ibischk5 parser. Ibischk5 includes numbered error, warning, note, caution, and bug messages. There are over 1200 unique message strings. The specification document will provide better documentation of these messages.

Ibischk5 version 5.1.3 fixed 6 bugs. The presentation detailed a fix for BUG140 in this release. BUG140 dealt with changing warning messages related to non-monotonic checking of combined I-V curves into notes. Anders concluded by recommending use of the latest version of ibischk5 for best checking results.

Lance Wang asked about EDA software related to BUG140. Isn't it true that you always have some smoothing taken care of because you deal with numerical error? Michael Schaeder responded that he always tries to use the original model data as much as possible. Lance asked about setting a tolerance limit to deal with BUG140. Randy Wolff responded that it is arbitrary to set that limit. He thinks it is a good solution to turn the warning into a note, and let the model maker look at it.

CLOSING REMARKS

Lance Wang closed the meeting by thanking the co-sponsors and the presenters. He also thanked all the attendees for making the meeting a success. The meeting concluded at approximately 5:15 PM.

NEXT MEETING

The next IBIS Open Forum teleconference will be held May 17, 2013 from 8:00 to 10:00 AM US Pacific Standard Time.

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NOTES

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To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the IBIS Open Forum as a full Member.

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To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.eda.org/ibis/bugs/ibischk/
http://www.eda.org/ibis/bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.eda.org/ibis/tschk_bugs/
http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/
http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eda.org/ibis

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/ibis/directory.html

To create an account on the TechAmerica KAVI workspace, check out:

http://workspace.techamerica.org/kwspub/join/

IBIS – TECHAMERICA STANDARDS BALLOT VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	March 15, 2013	April 5, 2013	April 26, 2013	May 15, 2013
Agilent Technologies	User	Active	X	-	X	-
Altera	Producer	Active	-	X	X	-
ANSYS	User	Inactive	-	-	-	X
Applied Simulation Technology	User	Inactive	-	-	-	-
ARM	Producer	Inactive	-	-	-	-
Cadence Design Systems	User	Active	X	X	X	-
Ericsson	Producer	Inactive	X	-	-	X
Foxconn Technology Group	Producer	Inactive	-	-	-	-
Freescale	Producer	Inactive	-	-	-	-
Huawei Technologies	Producer	Inactive	-	-	-	-
IBM	Producer	Active	X	X	X	X
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	X	X	X	-
IO Methodology	User	Active	X	X	-	X
LSI	Producer	Inactive	-	X	-	-
Maxim Integrated Products	Producer	Inactive	-	-	-	-
Mentor Graphics	User	Active	X	X	X	-
Micron Technology	Producer	Active	X	X	X	X
Nokia Siemens Networks	Producer	Inactive	-	-	-	-
QLogic	Producer	Inactive	-	-	-	-
Signal Integrity Software	User	Active	X	X	X	-
Synopsys	User	Inactive	X	-	-	-
Teraspeed Consulting	General Interest	Active	X	X	X	-
Texas Instruments	Producer	Inactive	-	-	-	-
Toshiba	Producer	Inactive	-	-	-	-
Xilinx	Producer	Inactive	-	-	-	-
ZTE	User	Inactive	-	-	-	-
Zuken	User	Inactive	-	-	-	X

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

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