Behavioral Model Solution for Driver's Overclocking Simulation

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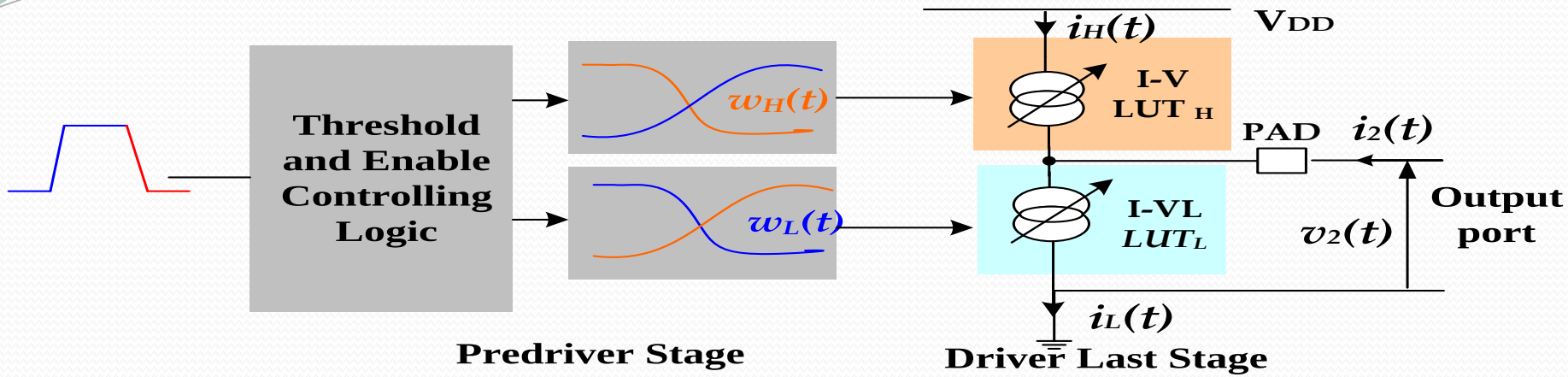
PRESENTATION OUTLINE

1. IBIS BUFFER MODEL STRUCTURE
2. WHY IBIS IS NOT SUITED FOR OVERCLOCKING
3. BEHAVIORAL MODELING SOLUTION ACCOUNTING OVERCLOCKING
4. MODEL EXTRACTION: INPUT/OUTPUT STAGE
5. MODEL VALIDATION : OVERCLOCKING CONDITION
6. CONCLUSIONS

IBIS BUFFER MODEL STRUCTURE



Basic elements of the digital IBIS output buffer behavioral model.

Global Model Structure :

$$i_2(t) = w_L^n(t).i_L(v_2(t), d/dt) + w_H^n(t).\ i_H(v_2(t), d/dt)\ ;\ n = u, d$$

- $i_H(.)$ and $i_L(.)$ are local nonlinear dynamic functions describing the driver's last stage output impedance.
- $w^n{}_H$ and $w^n{}_L$ are step input describing functions (StDFs) capturing the behavior of the predriver device stage.

Objective: Develop an effective large-signal behavioral model valid for transient simulation under overclocking conditions.

WHY IBIS is NOT SUITED FOR OVERCLOCKING

•**The StDFs capture the predriver nonlinear dynamics and the static nonlinear driver's last stage.**

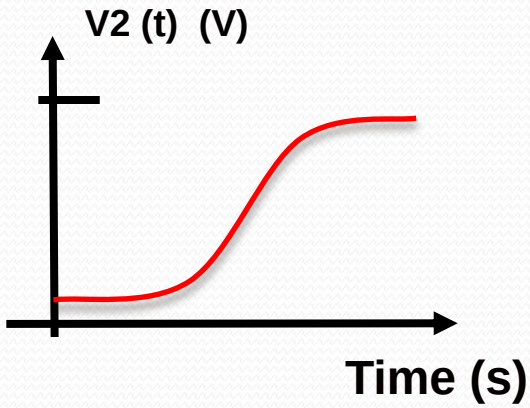
•**The inputs to the IBIS model are based on the concatenation of the StDFs. Therefore, it can be hard to line up properly these functions.**

⇒**Generates discontinuities and delays (i.e. the gate voltage does not reach steady state due to the overclocking).**

•**The StDFs should be concatenated insuring no discontinuity following the excitation parameters.**

PREDRIVER CIRCUIT UNDER STEP INPUT EXCITATION

From observation : the output waveforms of intrinsic driver's circuit under step input has monotonic evolution.

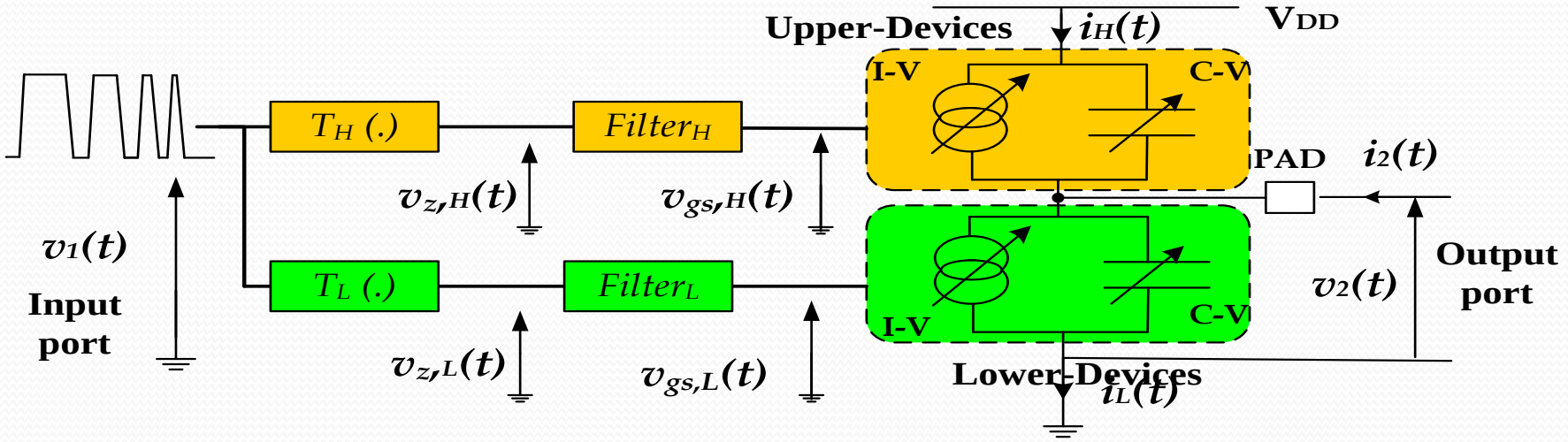


There are two physical interpretations that could be attributed to this behavior :

1- A nonlinear static behavior due to nonlinear characteristics of the predriver and driver's last stage.

2- The predriver stage dynamics: the driver doesn't respond immediately to the step input level change.

BEHAVIORAL MODELING SOLUTION ACCOUNTING OVERCLOCKING



$$\begin{cases} v_{z,j}(t) = T_j\left(v_1(t)\right) \\ v_{g,j}(t) = \int_0^t h_j(\rho) v_{z,j}(t-\rho)\, d\rho \end{cases} ; j = L, H$$

$$i_2\left(v_g(t), v_2(t)\right) = G_L\left(v_{g,L}(t)\right) i_L\left(v_2(t), \frac{dv_2(t)}{dt}\right) + G_H\left(v_{g,H}(t)\right) i_H\left(v_2(t), \frac{dv_2(t)}{dt}\right)$$

For complete details about the implementation please refer to :

W. Dghais, T. R. Cunha, and J. C. Pedro "A Novel Two-Port Behavioral Model for I/O Buffer Overclocking Simulation" *IEEE Trans. on Components, Packaging and Manufacturing Technology* , in press.

MODEL EXTRACTION: OUTPUT STAGE

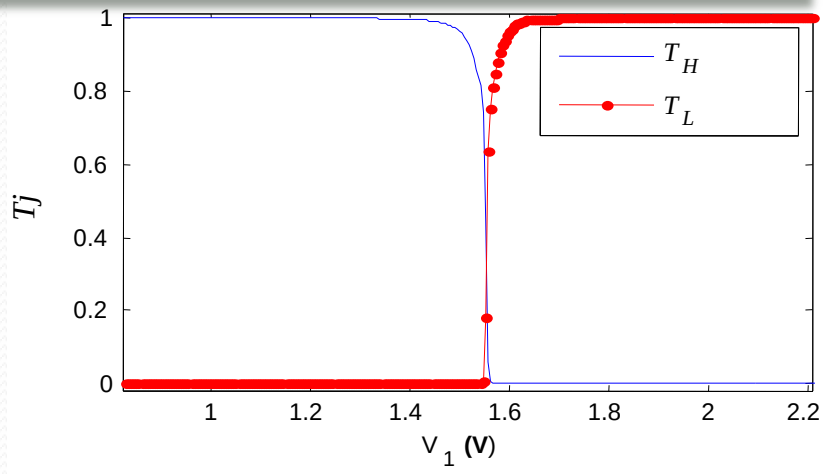
1- The $i_j(v_{gs},v_2=v_{sat})$ nonlinear static characteristics are identified via a DC sweep at the input port and keeping the output voltage port ones connected at 0V and the other to V_{dd}.

2- These nonlinear functions are normalized :

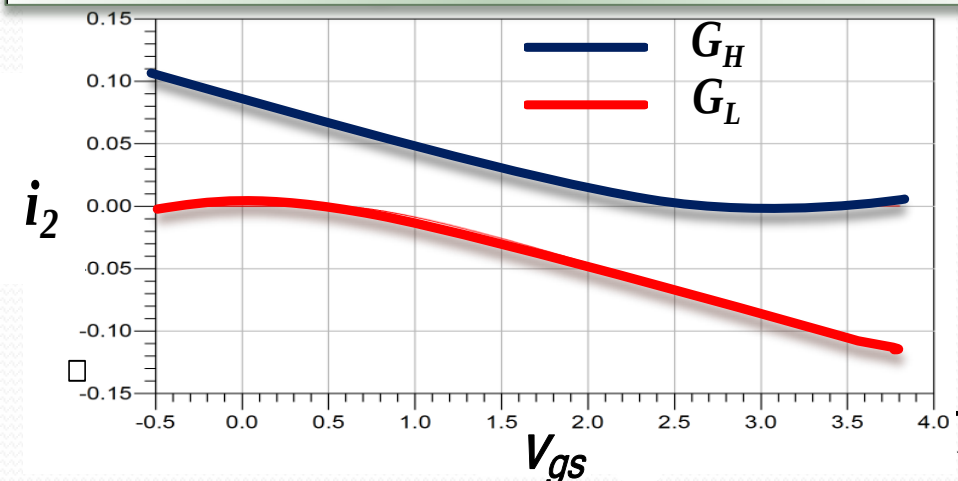
$$T_j(v_{gs},v_2=v_{sat}) = i_j(v_{gs},v_2=v_{sat})/i_2(v_{gs}=0V,v_2=v_{sat})$$

3-The nonlinear static functions are stored as look-up-tables (LUTs).

Predriver's nonlinear characteristic

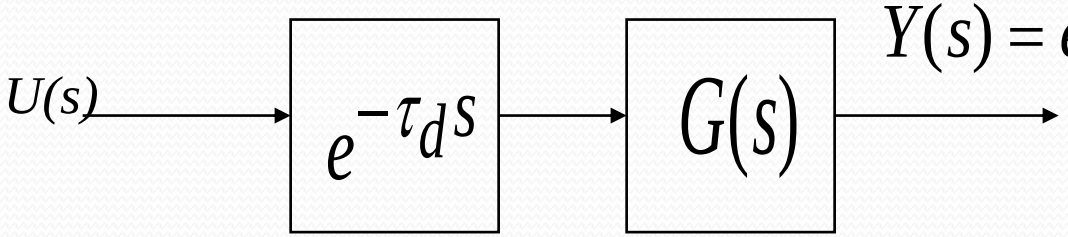


Driver's last stage nonlinear characteristic



MODEL EXTRACTION: INPUT STAGE

First-order plus dead time model formulation is used to model the predriver dynamics .



$$Y(s) = e^{-\tau_d s} G(s) U(s)$$

$$H(s) = \frac{K_0 e^{-\sigma s}}{1 + \tau * s}$$

K_0 is the dc voltage gain. The σ is dead time between the step excitation and the response. The low pass filter time constant is τ.

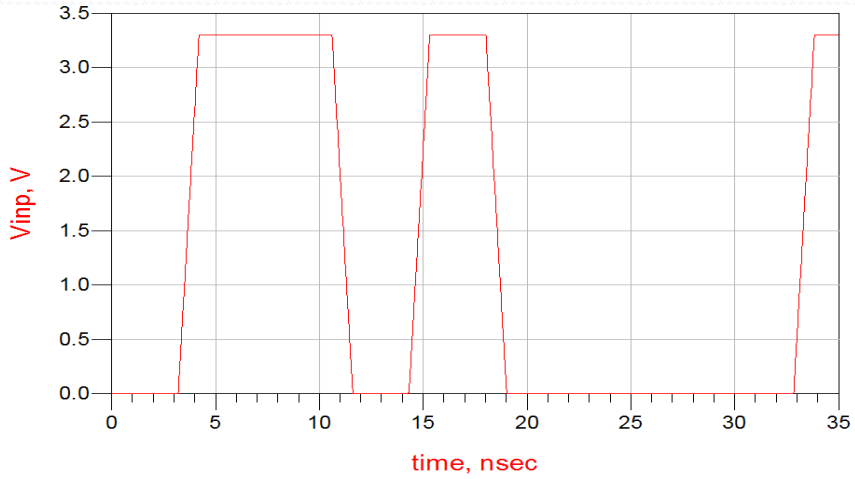
Extraction Methodologies of filter parameters (τ,σ) :

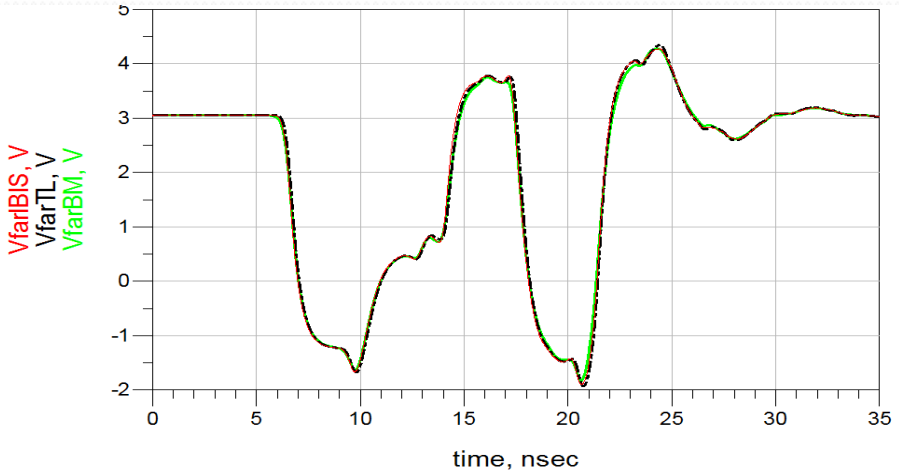
1. Statistical Approach : Least Squares Estimation

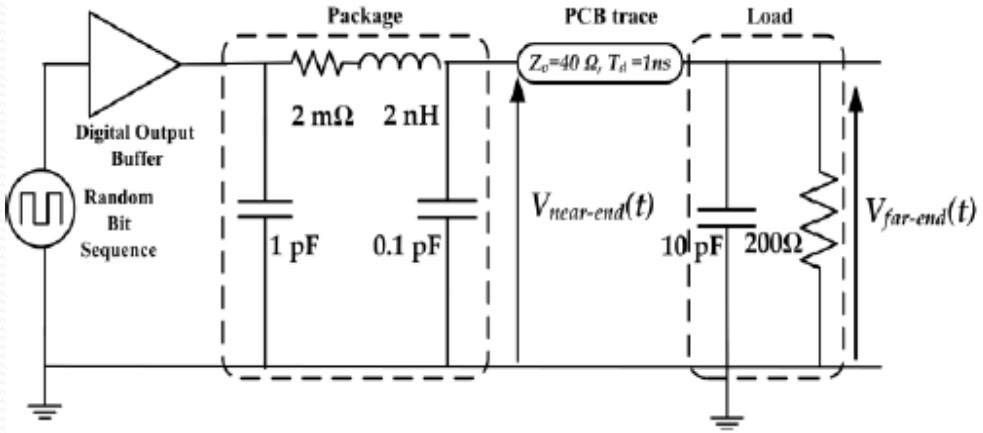
2. Curve Methods :quick and easy (i.e. based on engineering heuristics)

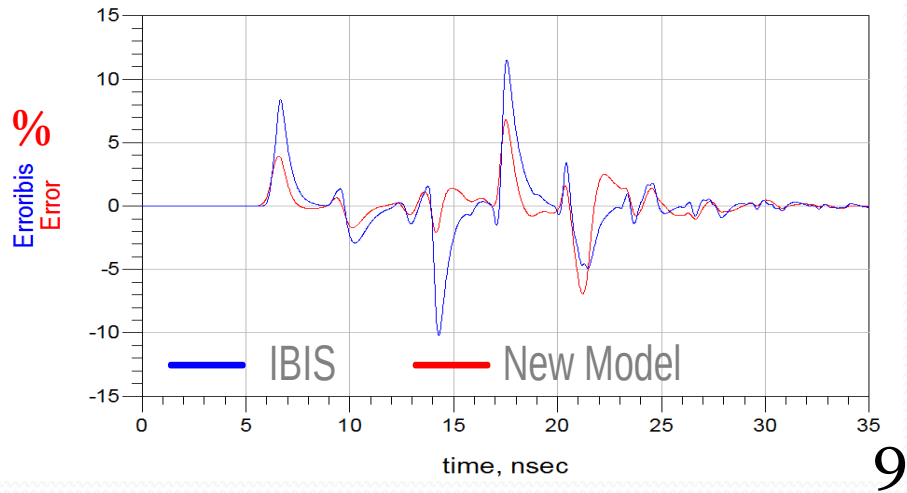
VALIDATION (1): NO OVERCLOCKING

Bit pattern “ 01101000”, Tr=Tf =1ns, Data Rate =270 Mbps



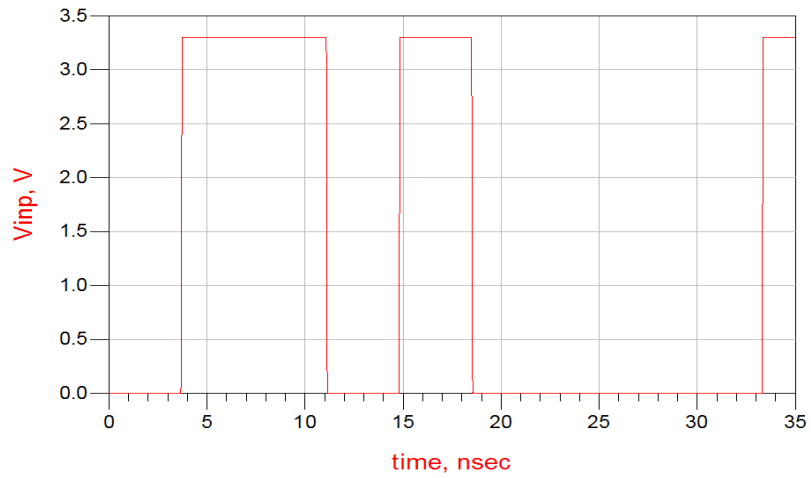


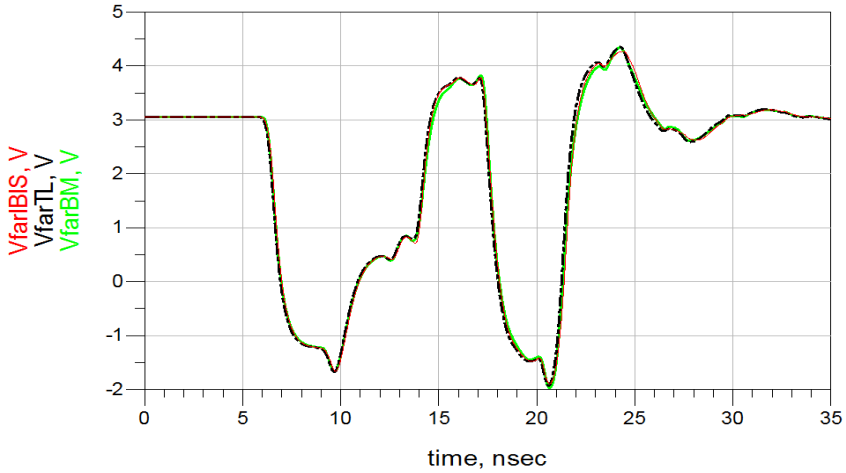


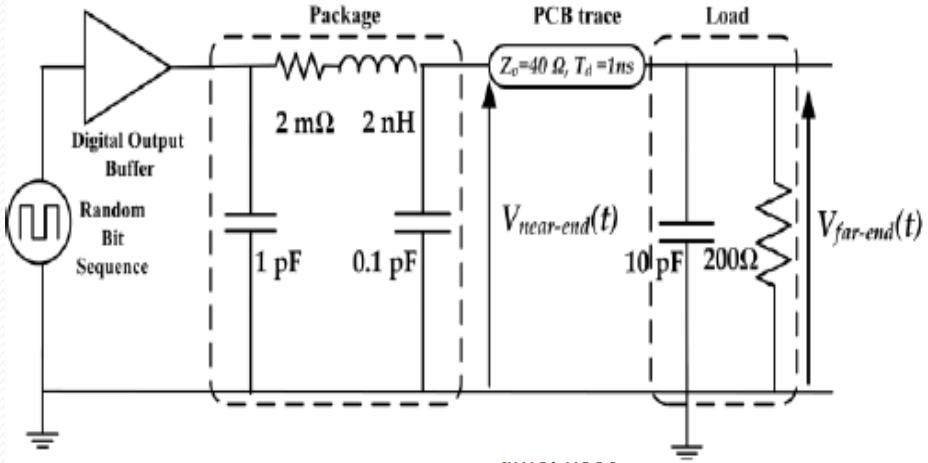


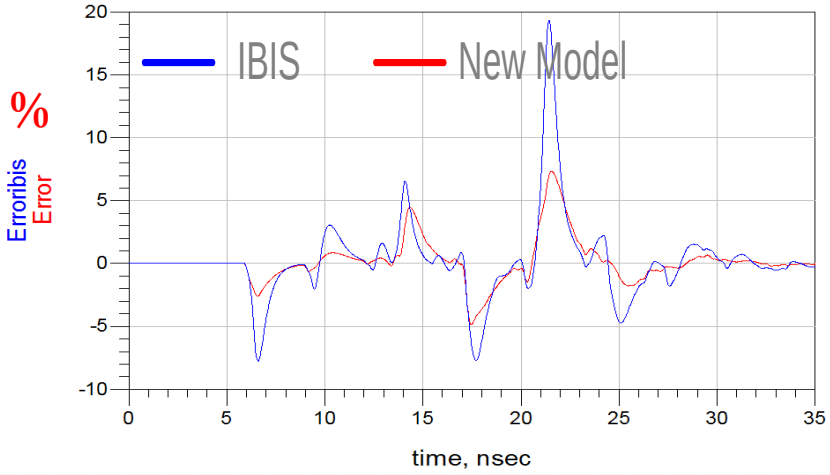
VALIDATION (2): NO OVERCLOCKING

Bit pattern " 01101000", Tr=Tf =0.3/0.1/0.05ns, Data Rate=270 Mbps



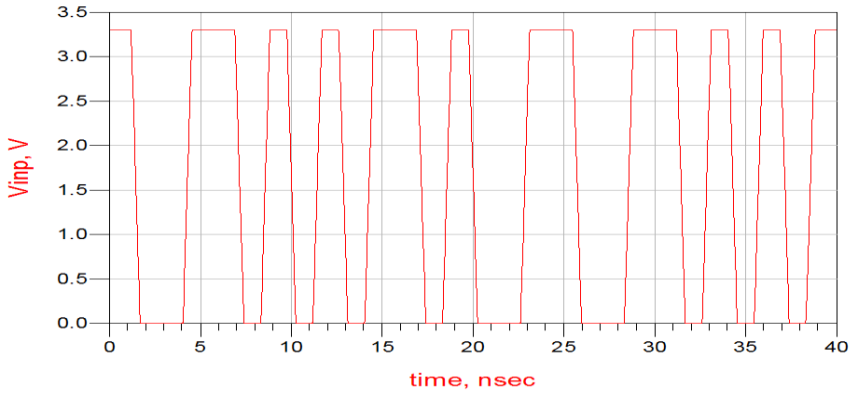


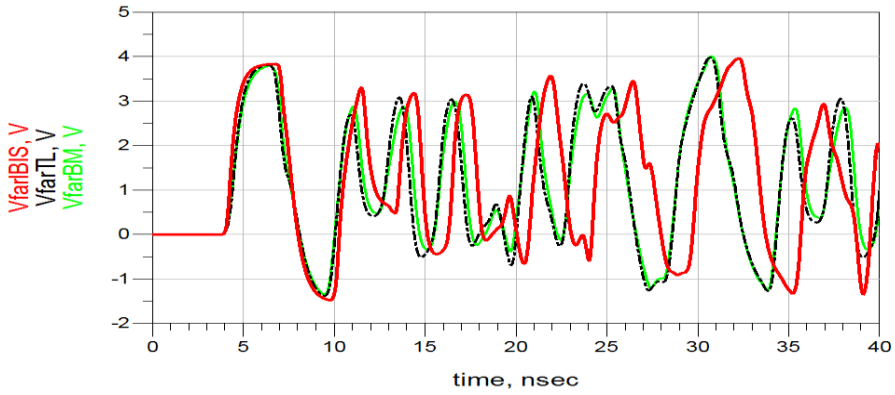


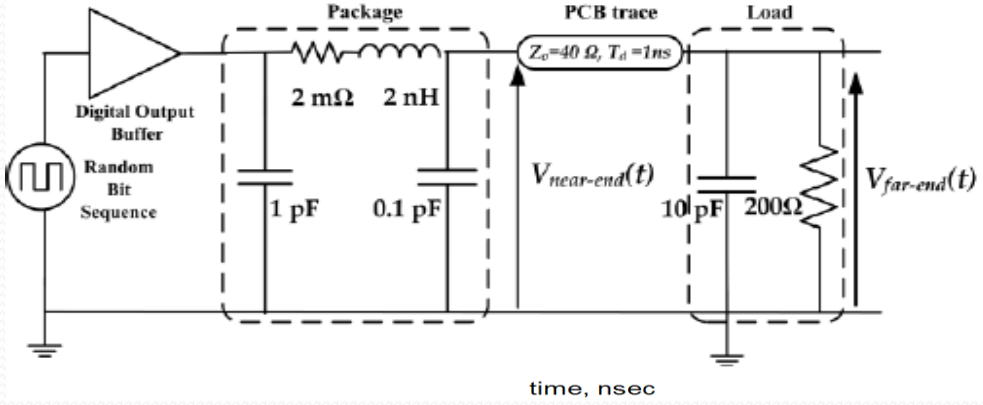


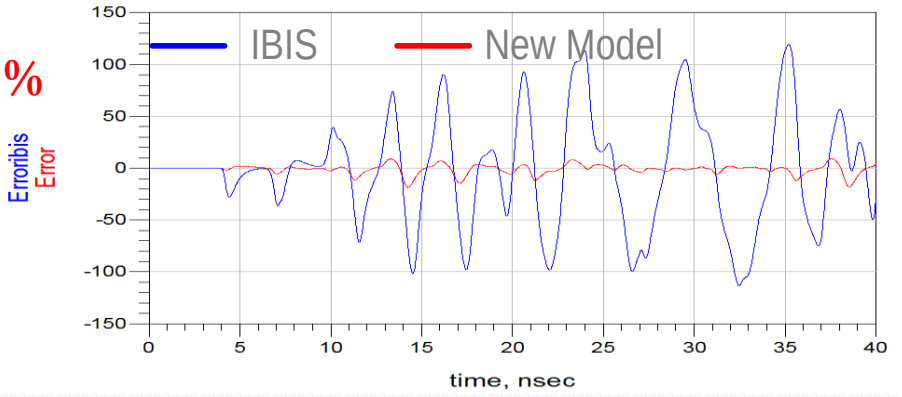
VALIDATION (3): UNDER OVERCLOCKING

Bit pattern "1001101010101101001", Tr=Tf =0.5ns, Data Rate=700 Mbps









Simulator warning : A falling IBIS trigger happens in the middle of a rising transition. A rising IBIS trigger happens in the middle of a rising transition

CONCLUSIONS

- **A novel circuit identification and implementation for Digital I/O Buffer Simulations is presented.**

- **The new model identifies the nonlinear dynamic circuit functions that map between the digital input signal and StDFs.**

- **The new model structure and implementation overcome and accuracy limitations that of the IBIS and other published approaches in nominal and overclocking operation conditions.**

- **The new model accuracy is better than IBIS model in both operating conditions.**

- **The new model does not introduce a significant CPU and memory resource consumption and maintains good simulation performance and convergence.**

Thank You for your Attention

Questions?