European IBIS Summit Meeting Sorrento, Italy, May 16, 2012

### Versatile surrogate models for IC buffers

C. Diouf<sup>1</sup>, <u>M. Telescu<sup>1</sup></u>, I. S. Stievano<sup>2</sup>, F. C. Canavero<sup>2</sup>, P. Cloastre<sup>1</sup>, N. Tanguy<sup>1</sup>

<sup>1</sup>Université Européenne de Bretagne, Université de Brest ; CNRS, UMR 6285, Lab-STICC, France

<sup>2</sup>Dipartimento di Elettronica e Telecomunicazioni (DET), Politecnico di Torino, Italy





### Outline

- o Introduction
- New approach: theoretical framework
- o Identification
- Recent developments
- o Examples
- Conclusion





## Introduction

 Nonlinear behavior of IC buffers ♦ Fading memory ♦ Highly nonlinear ♦Switching feature ♦Saturation Behavioral modeling techniques **♦ IBIS** Mπlog ♦ Neural networks, etc...





### Introduction

- 2-piece model (IBIS or Mπlog)
   ♦ Black box modeling of buffers
  - Output buffer port modeled in respect to input state (High or Low)
  - Transitions between states modeled through weighting functions
  - Output port relations, two submodels scheme





## Introduction

Mπlog + Volterra Series (SPI 2010)
 Each submodel represented by Volterra Series
 Exact static behavior not guaranteed
 Mπlog + Volterra Series + Constraints (SPI 2011)
 A posteriori mathematical constraints to improve static behavior





I/O behavioral modeling method is :

♦ Versatile

♦wide range of loads

\$ working for a wide range of frequencies

♦ Surrogate

Mathematical models

Based on Very high order Volterra-Laguerre Series





- Modeling strategy
  - Admittance, current source



#### Impedance, voltage source





 $v_2$ 

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- I/O Relations, "admittance",  $i_2[k] = f(v_1, v_2, [k])$ , "impedance"  $v_2[k] = f(v_1, i_2, [k])$
- High order Volterra-Laguerre series

$$Z\left(\phi_{n_{l},i_{l}}[k]\right)(z) = \sqrt{1 - a_{n_{l}}^{2}} \frac{z}{z - a} \left(\frac{1 - a_{n_{l}}z}{z - a}\right)^{i_{l}}$$
$$\overline{v}_{n_{l},i_{l}}[k] = \left(v_{n_{l}} * \overline{\phi}_{n_{l},i_{l}}\right)[k], n_{l} = 1, 2$$





$$\begin{split} &i_{2}[k] = \sum_{i_{1}=0}^{I_{1}-1} C_{1,1,i_{1}} \overline{v}_{1,i_{1}}[k] + \sum_{i_{1}=0}^{I_{1}-1} C_{1,2,i_{1}} \overline{v}_{2,i_{1}}[k] \\ &+ \sum_{i_{1}=0}^{I_{2}-1I_{2}-1} C_{2,1,1,i_{1},i_{2}} \overline{v}_{1,i_{1}}[k] \overline{v}_{1,i_{1}}[k] + \sum_{i_{1}=0}^{I_{2}-1I_{2}-1} C_{2,1,2,i_{1},i_{2}} \overline{v}_{1,i_{1}}[k] \overline{v}_{2,i_{1}}[k] \\ &+ \sum_{i_{1}=0}^{I_{2}-1I_{2}-1} C_{2,2,1,i_{1},i_{2}} \overline{v}_{2,i_{1}}[k] \overline{v}_{1,i_{1}}[k] + \sum_{i_{1}=0}^{I_{2}-1I_{2}-1} C_{2,2,2,i_{1},i_{2}} \overline{v}_{2,i_{1}}[k] \overline{v}_{2,i_{1}}[k] \\ &+ \sum_{i_{1}=0}^{I_{2}-1I_{2}-1} C_{2,2,1,i_{1},i_{2}} \overline{v}_{2,i_{1}}[k] \overline{v}_{1,i_{1}}[k] + \sum_{i_{1}=0}^{I_{2}-1I_{2}-1} C_{2,2,2,i_{1},i_{2}} \overline{v}_{2,i_{1}}[k] \overline{v}_{2,i_{1}}[k] \\ &+ \dots \end{split}$$





### Identification

- Apply a well-chosen identification sequence to the driver.
- $\circ$  Extract voltages( v<sub>1</sub>, v<sub>2</sub>) and output current (i<sub>2</sub>)
- By least squares find C coefficients that satisfied best the Volterra-Laguerre relation

$$i_{2}[k] = \sum_{m=1}^{M} \sum_{n_{1}=1}^{2} \dots \sum_{n_{m}=1}^{2} \sum_{i_{1}=0}^{I_{m}-1} \sum_{i_{m}=0}^{I_{m}-1} C_{m,n_{1},\dots,n_{m},i_{1},\dots,i_{m}} \prod_{l=1}^{m} \overline{v}_{n_{l},i_{l}}[k]$$





## Identification

 Variable identification load
 Allowing a good static exploration
 Dynamic exploration of (i<sub>2</sub>,v<sub>2</sub>) trajectories resulting from interconnects reactive elements









# **Recent developments**

o Piece-wise approach → reduce complexity
o Output relation







 Test vehicle: tunable synthetic system mimicking single ended non inverting driver



- $\circ$  f(v<sub>1</sub>,v) nonlinear current source
- o Dynamic by reactive components





#### Input/Output Characteristic





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- System is identified through the described procedure
- The Volterra-Laguerre model is implemented in SPICE
- o Validation
  - Input validation signal
  - On two load configurations





### Input validation signal





### o First Load





#### o Second Load





### Cascaded drivers





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### o First Load





#### o Second Load





# Conclusion

- A new approach to IC buffer modeling seeking more general, versatile models
- Ongoing research on more complex, recent buffers
- > Tuning the method on the needs of the industry

