Efficient Table-Based I-Q Behavioral Model for High-Speed Digital Buffers/Drivers

W. Dghais, H. M. Teixeira, T. R. Cunha and J. C. Pedro

E-mail: waeldghais@ua.pt

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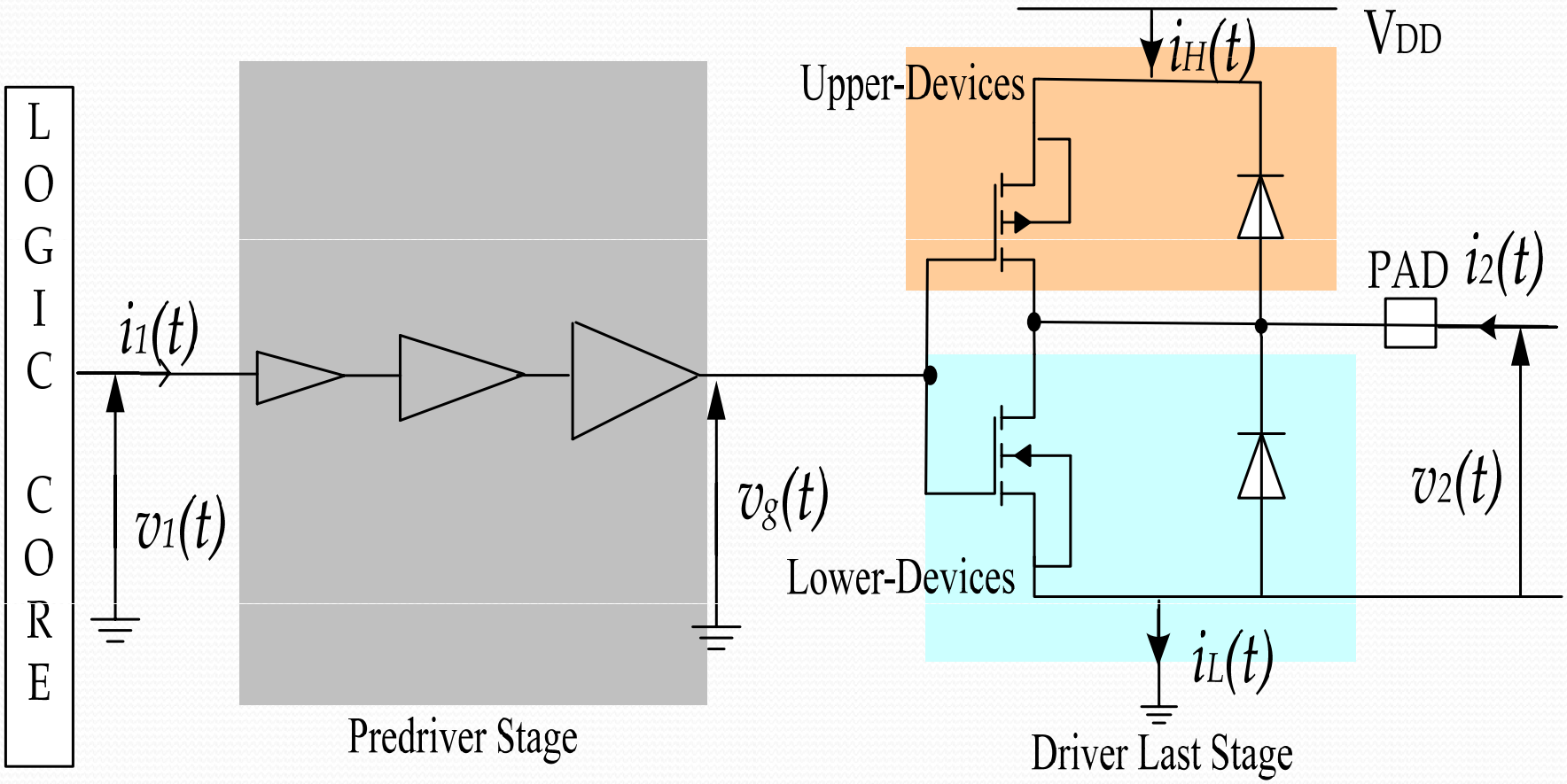
DETI.UA.PT
universidade de aveiro

instituto de telecomunicações

Presentation Outlines

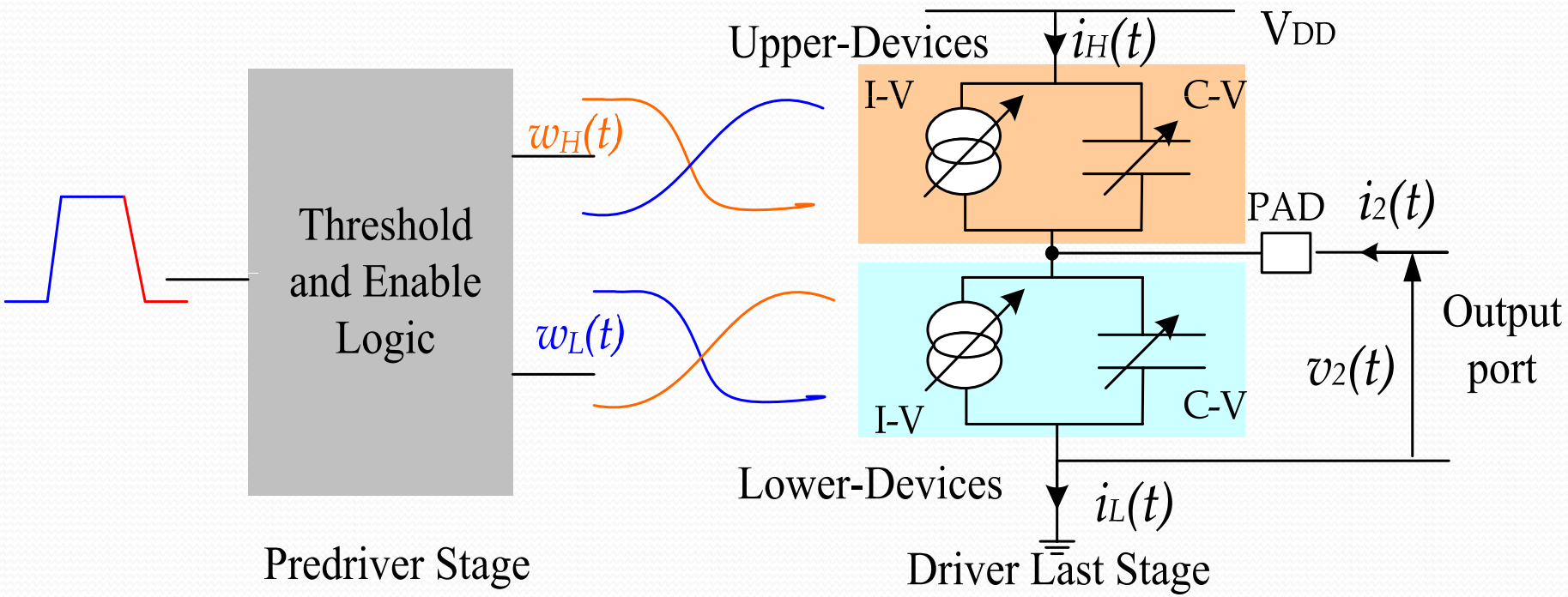
1. Behavioral Model Structure
2. Output Impedance
   - -Model Structure
   - -Extraction & Implementation
3. StIDF Extraction
4. Validation Results
5. Conclusions

Digital I/O buffer Structure



Basic structure of the two port digital output buffer and its main electrical variables

Driver's model Structure

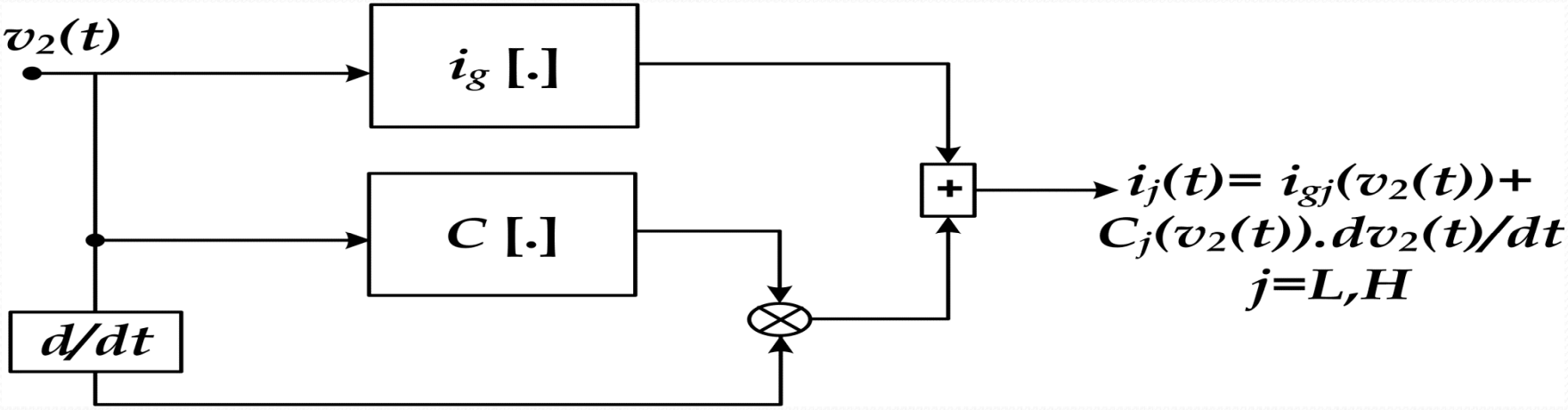


Basic elements of the digital I-Q output buffer behavioral model.

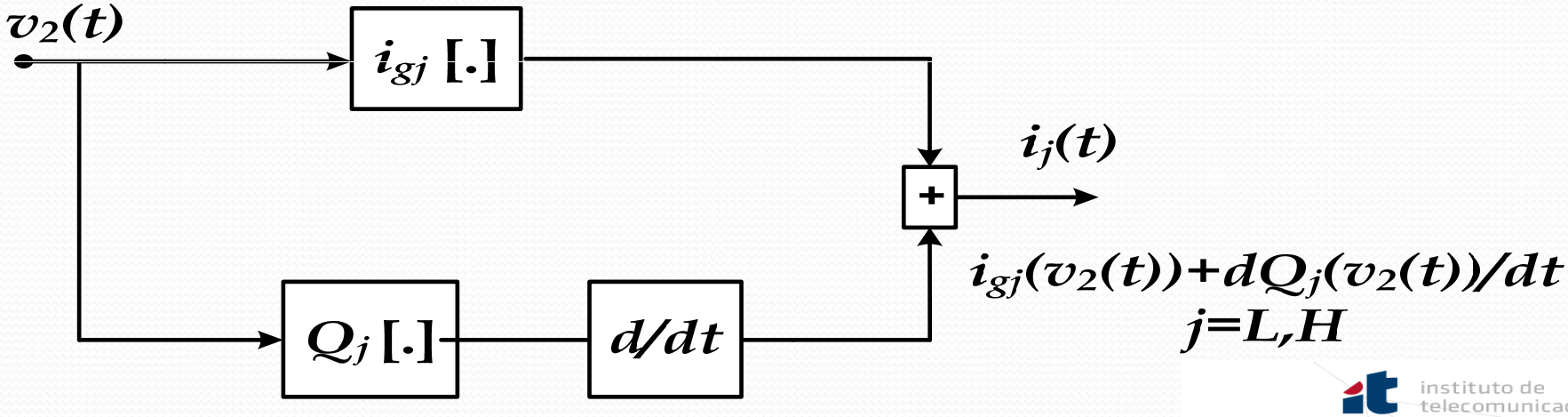
$$i_2(t) = w_L(t).\, i_L(v_2(t), d/dt) + w_H(t).\, i_H(v_2(t), d/dt)$$

Output impedance I-Q Model

I-V / C-V Extraction

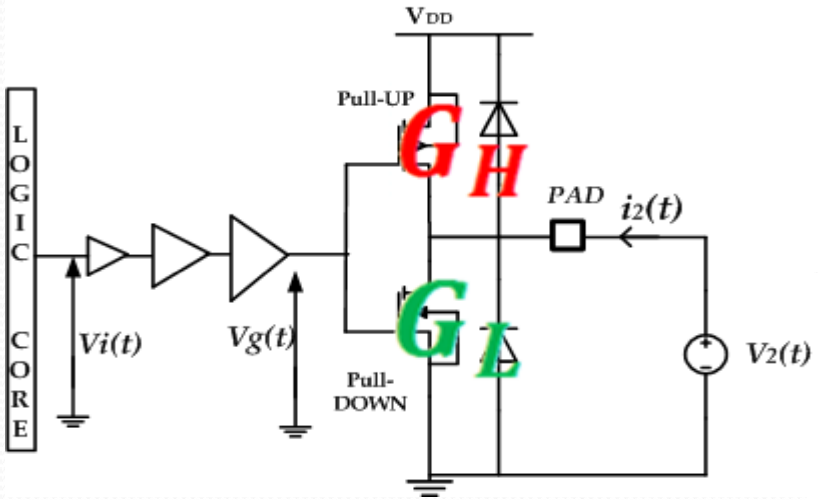


I-V / Q-V Implementation

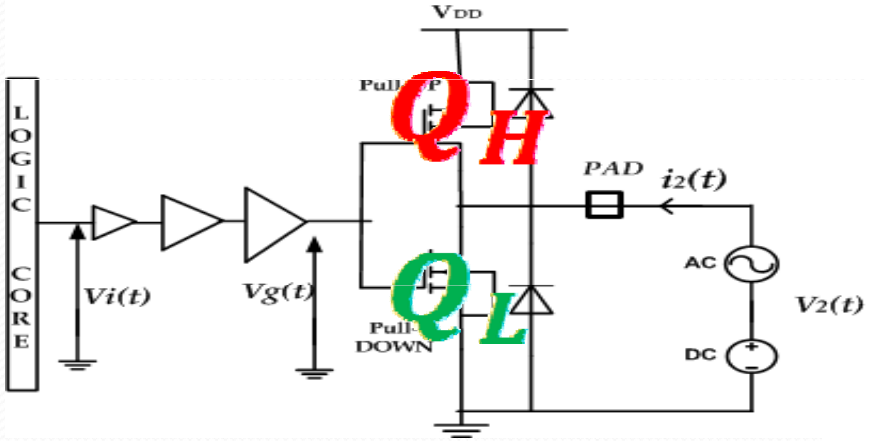


IQ Model Extraction

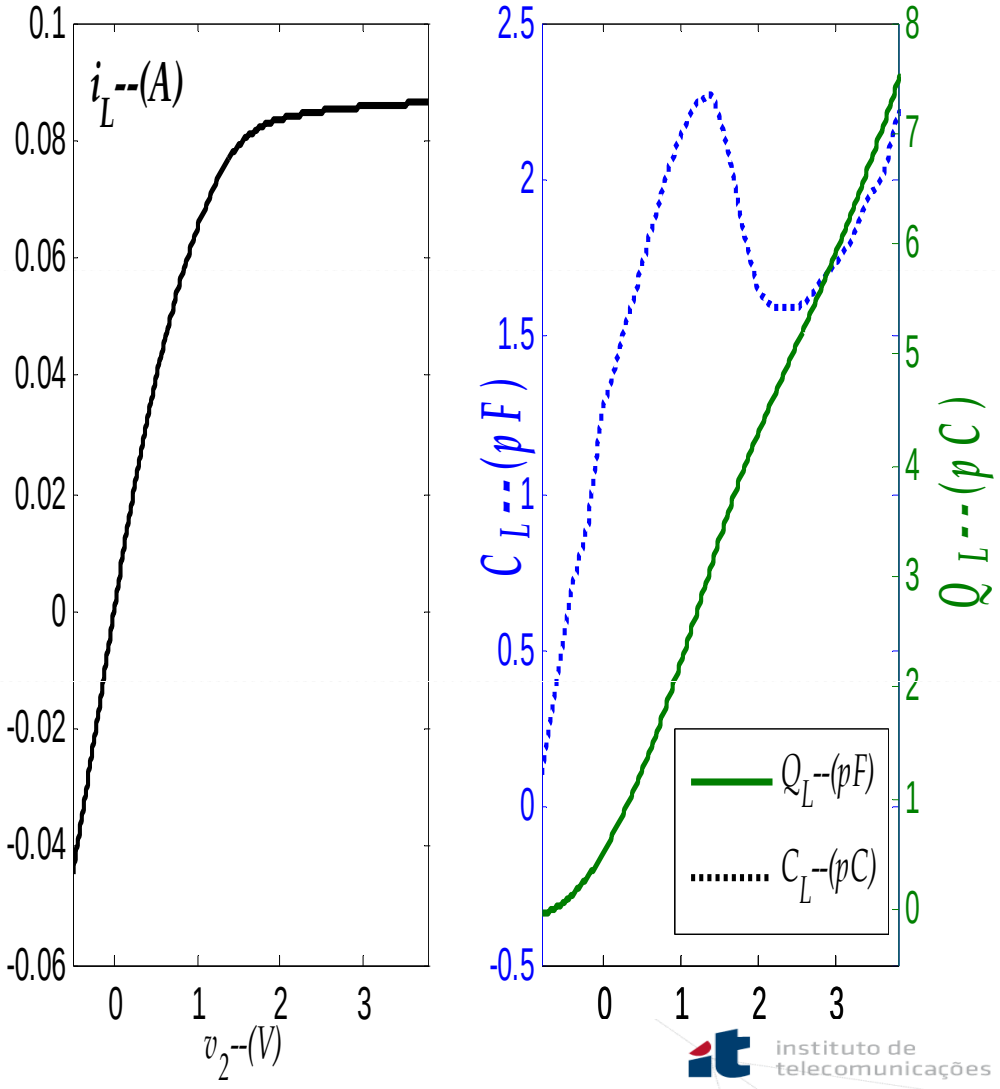
I-V Conduction Current



Q-V displacement Current



Extraction Example



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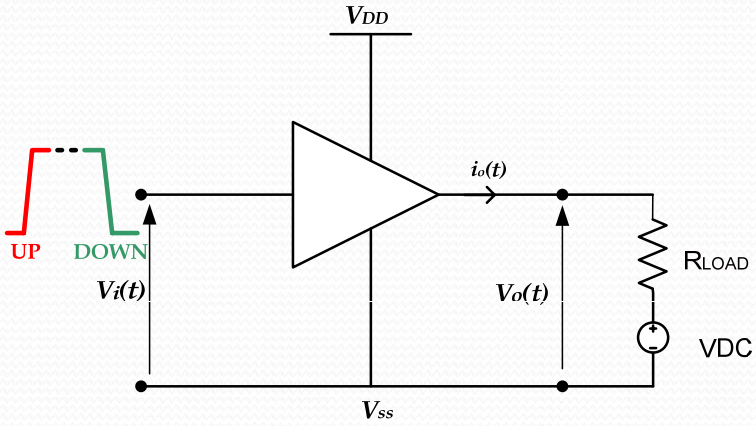
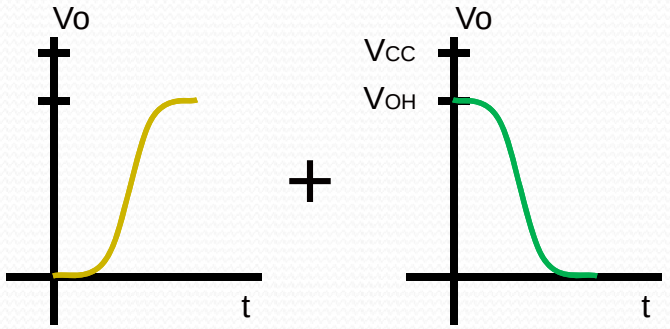
Step Input Describing Functions

The $w_L(.)$ and $w_H(.)$ give the transient information about the predriver's nonlinear dynamics (e.g. asymmetric gain, overshoot, rise/fall time, settling time and ringing) for up/down transitions.

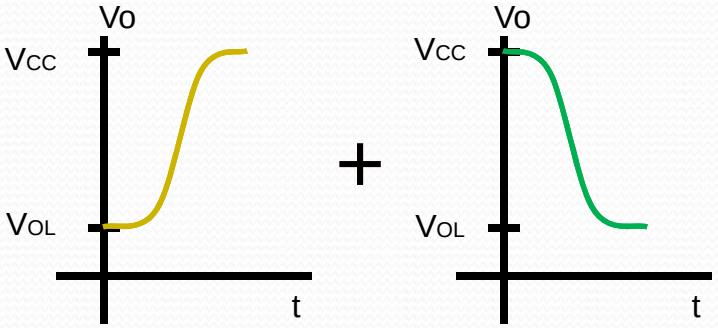
The transient identification signal data



- **VDC = GND**



- **VDC = VDD**



$$\begin{bmatrix} w_L(t) \\ w_H(t) \end{bmatrix} = \begin{bmatrix} i_{L,gnd}(t) & i_{H,gnd}(t) \\ i_{L,Vdd}(t) & i_{H,Vdd}(t) \end{bmatrix}^{-1} \begin{bmatrix} i_{2,gnd}(t) \\ i_{2,Vdd}(t) \end{bmatrix}$$

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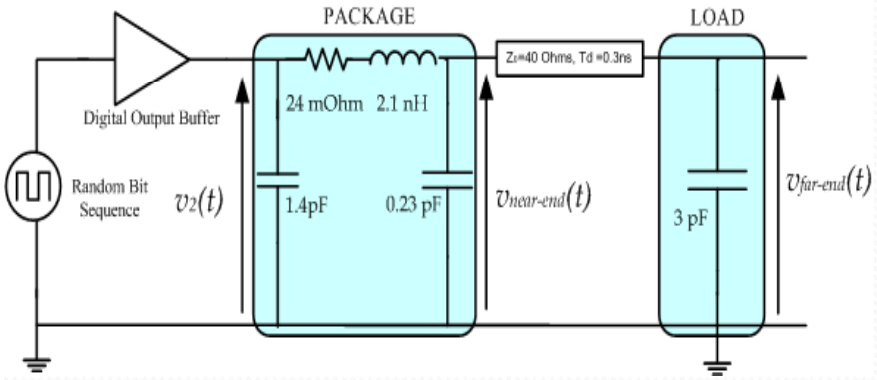
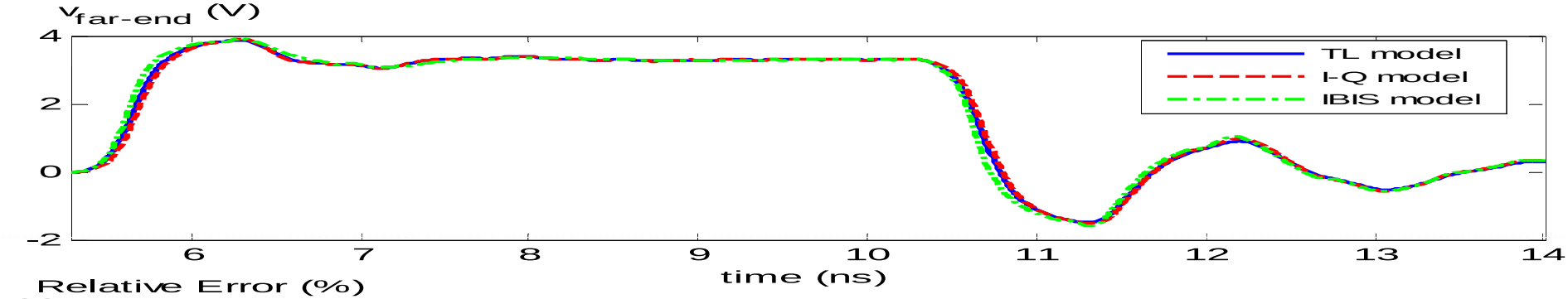
Validation Results

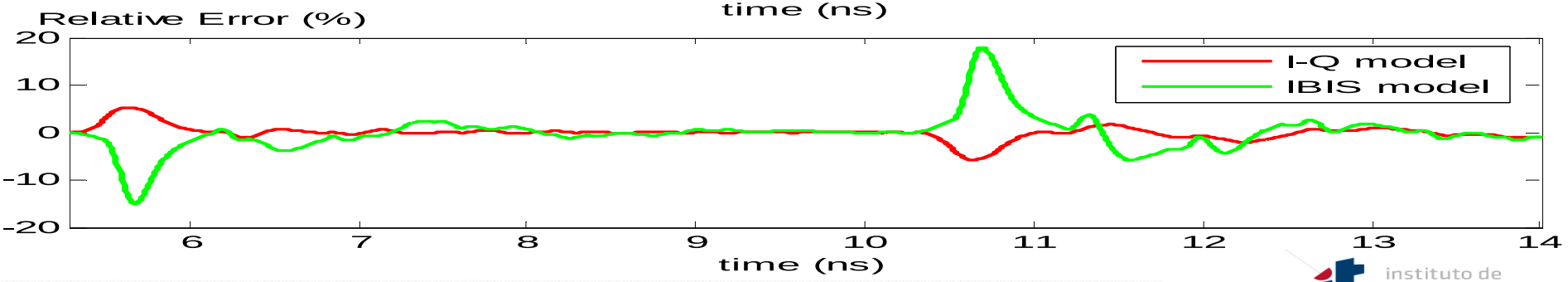
SI Validation Setup.



Performance of the TL and Behavioral Models.

Model	NMS E(dB)	Memory Used (KB)	CPU time (ms)
TL	-	$2*10^3$	$47*10^3$
IV/CV	-28.94	860	439
IV/QV	-28.94	661	321





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Conclusions

-The I-Q model can be directly implemented in SPICE-like simulators where the derivative in is implemented by the simulator core functions (in continuous-time).

-The output conduction current-voltage (I-V) static relation, and the displacement charge-voltage (Q-V) function, for the upper and lower devices of the driver's last stage are stored as lookup tables that capture.

-The C-V implementation requires one more floating point operation (FLOP) than the Q-V one, which corresponds to an increase of about 33% in simulation efficiency.

-The proposed implementation is directly applicable to the IBIS definition, extending it with the nonlinear dynamics of the buffer output impedance.

References

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