

AGENDA, EUROPEAN IBIS SUMMIT MEETING

Wednesday, May 16, 2012
Parco dei Principi - Sorrento Hotel
Sorrento, Italy
Room: Leonardo Room (Check at Entrance)

Sponsors: Micron Technology, Nokia Siemens Networks, Zuken, and
IEEE Workshop on Signal and Power Integrity

13:00 **REFRESHMENTS & SIGN IN**

13:15 **WELCOME AND INTRODUCTIONS**
Lance WANG, IO Methodology, IBIS Vice Chair, USA

13:25 **IBIS Modeling Using Latency Insertion Method (LIM)**
Jose SCHUTT-AINE*, Jilin TAN**, Ping LIU**, Feras AL-HAWARI**,
and Ambrish VARMA**,
*University of Illinois at Urbana-Champaign
**Cadence Design Systems, USA

14:00 **IBIS in Academia Update**
Bob ROSS, Teraspeed Consulting Group, USA

14:30 **Versatile Surrogate Models for IC Buffers**
Cherif DIOUF*, Mihai TELESU*, Igor STIEVANO**, Flavio CANAVERO**,
P. CLOSTRE*, and N. TANGUY*,
*Universite Europeenne de Bretagne, Universite de Brest, France;
**Politecnico di Torino, Italy

15:00 **Towards Real-time S-parameter Qualification and Macromodeling**
Stefano GRIVET-TALOCIA, Politecnico di Torino, Italy

15:30 **BREAK** (15 Minutes)

AGENDA, EUROPEAN IBIS SUMMIT MEETING (Continued)

- 15:45 **Impact of Accurate PDN Model on IBIS SI and PI Simulations**
Antonio GIRARDI and Aniello VISCARDI,
Micron Semiconductor Italia S.r.l., Italy
- 16:15 **DDR4 IBIS Power Integrity Simulation**
Randy WOLFF* and Lance WANG**,
*Micron Technology and **IO Methodology, USA
- 16:45 **More Experiences With IBIS-AMI Models**
Eckhard LENSKE, Nokia Siemens Networks GmbH & Co KG, Germany
- 17:15 **SSO Noise and Conducted EMI: Modeling, Analysis, and Design Solutions**
Patrice Joubert DORIOLE#, Aurora SANNA#, Akhilesh CHANDRA##,
Cristiano FORZAN#, and Davide PANDINI#
STMicroelectronics, #Italy, ##India
- 17:45 **CLOSING REMARKS**
Lance WANG, IO Methodology, USA
- 18:00 **END OF MEETING**