MOCHA (MOdelling and CHAracterization for SiP Signal and Power Integrity Analysis)

IC Power Delivery Modeling

MOCHA

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MOCHA (MOdelling and CHAracterization for SiP Signal and Power Integrity Analysis)

The MOCHA project was focused on developing accurate models and viable simulation and measurement solutions for SiP design verification.



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MOCHA is a STREP project funded by the European Community under the Seventh Framework Programme. It addresses the FP7 ICT-2007.3.1 call objectives.

The MOCHA project work plan is organized into four major work packages, WP1, WP2, WP3, WP4, which logically define the different fields that have to be addressed in order to achieve the expected technical goals.

WP1 - IC power integrity model
WP2 - IC buffers' innovative modelling approach
WP3 - SiP design and verification EDA platform
WP4 - SiP signal integrity measurement platform

Consortium Partners



- Numonyx Italy Srl (Italy) (now Micron) Project Coordinator
- Cadence (Germany) CAD Vendor
- Agilent (Belgium) CAD Vendor
- Politecnico di Torino (Italy) European University
- Instituto de Telecomunicacoes (Portugal) European University
- Microwave Characterization Center (France) SME





IC Power Integrity Model

Work Package 1



Motivation

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IC power supply model suggested by ICEM

How can we compute model parameters from measured data?
 Can we improve the model for a specific class of devices?

Contributions

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I/O Power Rail Modeling



□ **Model structure:** cascade connection of lumped RLC cells

- Detailed information on the internal structure
- On-chip measurements

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□ **Model structure:** Equivalent impedance of a Norton equivalent

- Detailed information on the internal structure
- On-chip measurements
- On-board measurements

Smooth – capacitive – behavior (i.e., Ze≅1/sC)

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Model structure: Equivalent impedance, cont'd

-2000

 $1/s\tilde{C}$

SMA

 $Z_e(s)$

VSS

Ideal setup

IC (die+package)

 $Z_e(s) = 1/sC +$

 Z_e from S11 measurements with or without the IC mounted on the board

Detailed information on the internal

On-chip measurements

structure

[1] I.S. Stievano, L. Rigazio, F.G. Canavero, T.R. Cunha, J.C. Pedro, H.M. Teixeira, A. Girardi, R. Izzi, F. Vitale, "Behavioral modeling of IC memories from measured data," IEEE Transaction on Instrumentation and Measurements (in press).

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□ Model structure: Equivalent impedance, cont'd

... from on-board measurements

Test board (implementing the ideal setup)

Impedance seen from SMA₁

Model structure: <u>Current source</u>

– A(s) / a(t) from detailed information

A(s) / a(t) from measurements

a(t) either from numerical simulation or provided by the IC vendor

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Model structure: <u>Current source</u>, cont'd

A(s) / a(t) from detailed information
A(s) / a(t) from measurements

Ideal setup (the same for impedance estimation)

 SMA₁ for current measurement
 A(s) cannot be measured
 Post processing of I_{SS} required (see [1])

[1] I.S. Stievano, L. Rigazio, F.G. Canavero, T.R. Cunha, J.C. Pedro, H.M. Teixeira, A. Girardi, R. Izzi, F. Vitale, "Behavioral modeling of IC memories from measured data," IEEE Transaction on Instrumentation and Measurements (in press).

Model structure: <u>Current source</u>, cont'd

- Current measurement via the 1Ω probe method defined in the IEC 61967-4 [2]
- Effective solution among alternative methods [3]

 [2] "International Electro-technical Commission, IEC 61967 Part 4: Measurement of conducted emission - 1 /150 direct coupling method," 2006.

[3] F. Fiori, F. Musolino, "Comparison of IC Conducted Emission Measurement Methods," IEEE Trans. On Instrumentation and Measurement, Vol. 52, No. 3, pp. 839–845, June 2003

Model structure: <u>Current source</u>, cont'd

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Validation

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 Good agreement between measurements and simulations (switching activity current)

Validation

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1/0

VDDO

Good agreement between measurements and simulations (simultaneous switching output)

Simulation with swa pwl generator by measurements

Simulation without IC power supply distribution model

NOR Test-case

Measurements Simulation with swa pwl generator by simulation Simulation with swapwl generator by measurements

LPDDR Test-case @ 133MHz

[2] T.R. Cunha, J.C. Pedro, H.M. Teixeira, I.S. Stievano, L. Rigazio, F.G. Canavero, R. Izzi, F. Vitale, A. Girardi, "Validation by Measurements of a IC Modeling Approach for SiP Applications," submitted for possible publication in the IEEE Transactions of Advanced Packaging.

Conclusions

A methodology for extracting an IC power integrity model by simulation and measurement has been defined:

- Distributed model (cascade connection of lumped cells) for I/O power rail
- Lumped model for IC core power rail
- IC core switching activity model
- Every simulation model element was validated by measurement (good agreement)
- Whole power integrity model validated by actual SSO measurements

Contacts

MOCHA Project website: http://www.mocha.polito.it

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