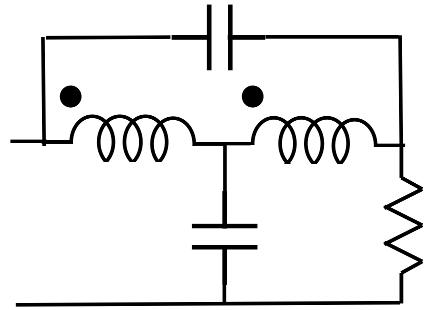

T-Coils and Bridged-T Networks

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European IBIS Summit
Naples Italy
May 11, 2011

(Portions presented earlier at IBIS Summit meetings September 11, 2007 and February 3, 2011)

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Topics and Goals

- Old technology, current applications
  - Historical overview
  - Some recent applications
  - Some extensions
- Introduce standard T-coils and features
- Relates to IBIS and IBIS-AMI and IBIS-ISS
  - Some Recent SerDes design methods use T-coils
  - SPICE subcircuit, Laplace transform, S-parameter representations

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Bridged T-coil Properties

- T-coil summary
  - Constant R provides ideal load or termination
  - Up to 2.82 bandwidth improvement (BWER or bandwidth extension ratio) over RC based bandwidth
  - 2.73 improvement for acceptable 0.4% overshoot to ideal step input (MFED or maximally flat envelope delay design)
  - Complexity reduction (poles/zero cancellation)
- Now used in high-speed buffer design
  - ESD (electrostatic discharge) compensation
  - Bandwidth improvement

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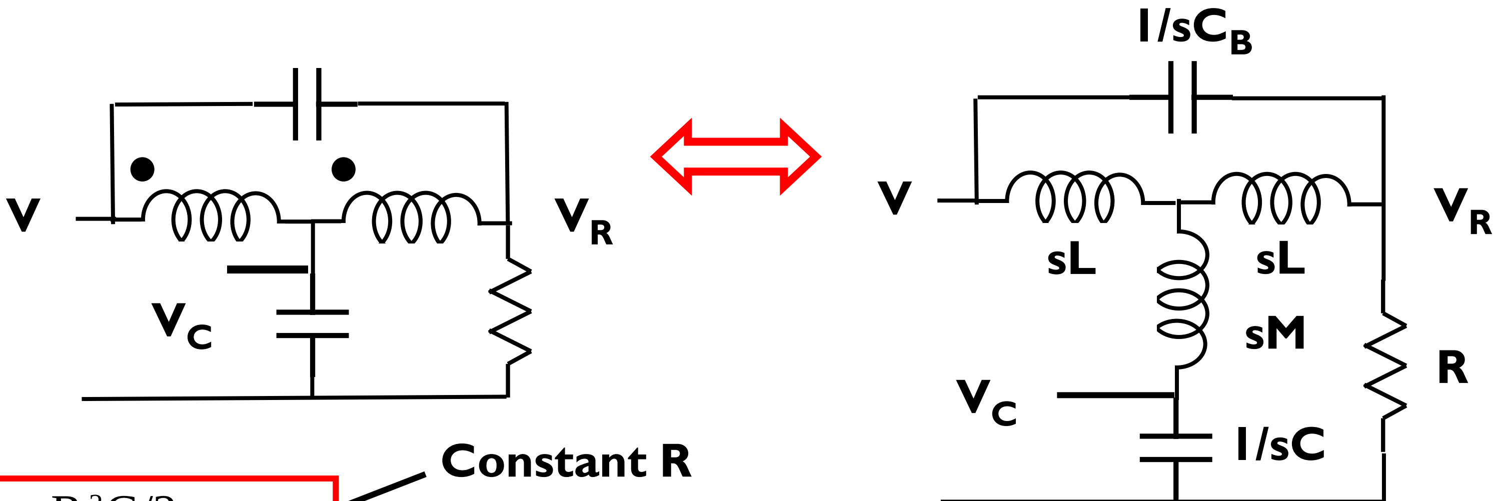
(Constant R) Bridged T-coil Example



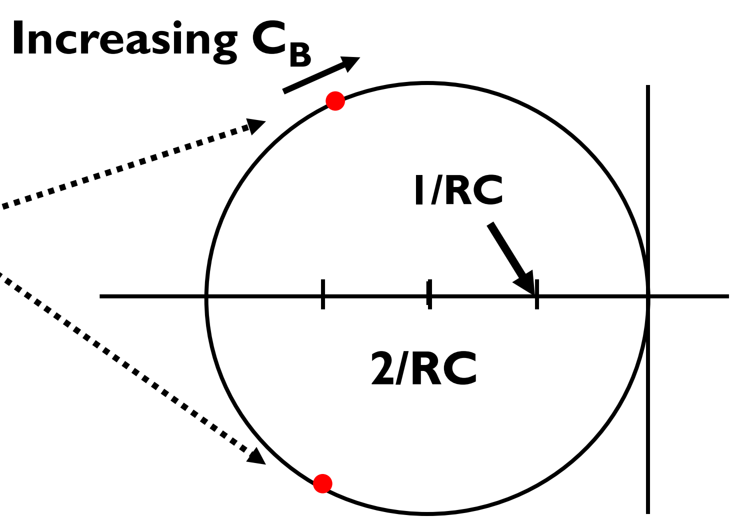
Constant R

$$L = R^2C/2$$

$$M = R^2C_B - L/2$$

$$\frac{V_C}{V} = \frac{1}{R^2CC_Bs^2 + \frac{RC}{2}s + 1}$$

$$\frac{V_R}{V} = \frac{R^2CC_Bs^2 - \frac{RC}{2}s + 1}{R^2CC_Bs^2 + \frac{RC}{2}s + 1}$$



Poles 30 degrees for maximally flat envelope delay (MFED)

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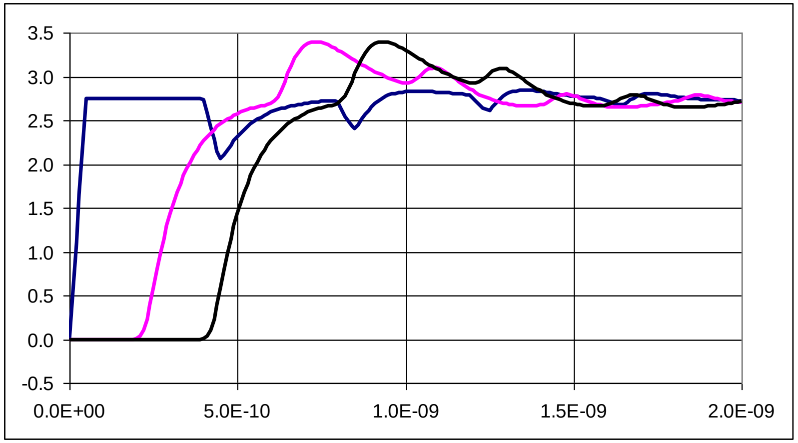
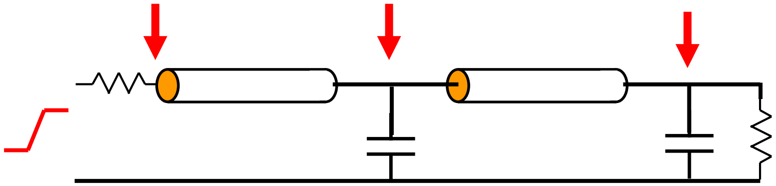
T-coil Improvement (terminated multi-drop Line)

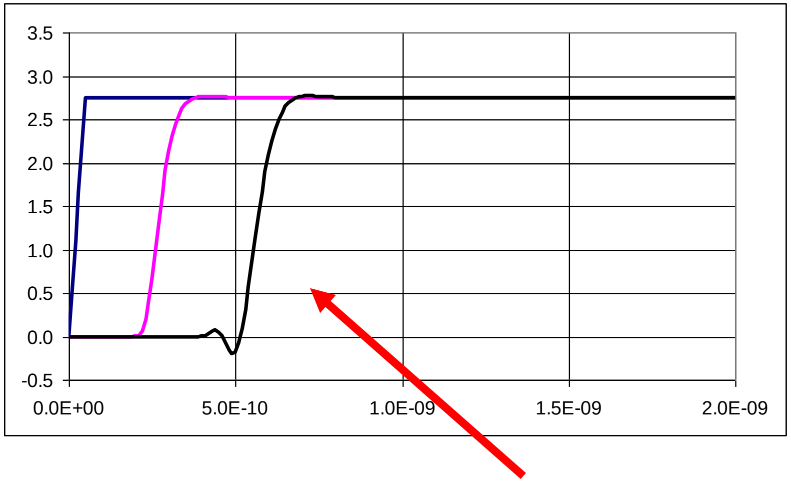


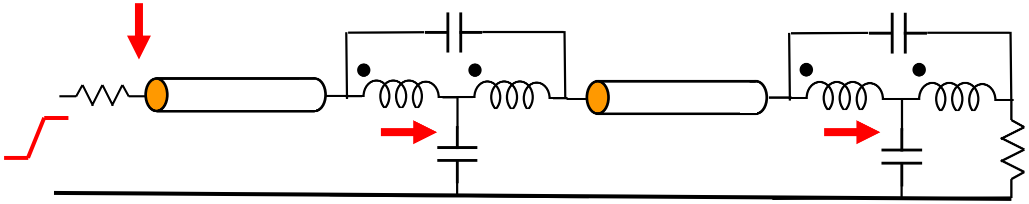


Rsource = 10 Ω, Rload = 50 Ω

C = 2 pF, TL = 50 Ω, 200 ps

Vin = 0 to 3.3 V, 50 ps ramp





Cleaner and faster responses, but with more delay

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Wang Algebra – 75+ Years Ago

K.T. Wang, "On a new method of analysis of electrical networks," in Memoirs 2, *Nat. Res. Inst. Eng. Academia Sinica*, pp. 1-11, 1934

S.L. Ting, "On the general properties of electrical network determinants," *Chinese J. Physics*, vol 1, pp. 18-40, 1935

C.T. Tsai, "Short cut methods of Wang algebra of network problems," *Chinese J. Physics*, vol. 3, pp. 141-181, 1939

R.J. Duffin and T.D. Morley, "Wang algebra and matriods," IEEE Trans Circuit and Systems, vol CAS-25, no 9, pp. 755-762, Sept., 1978

W.K. Chen, Graph Theory and Its Engineering Applications (ch. 5, sect. 4, "The Wang-algebra formulation"), World Scientific Publ., 1997

Wang Algebra:

$$XX = 0$$
$$X+X = 0$$
$$XY = YX$$

= *W*

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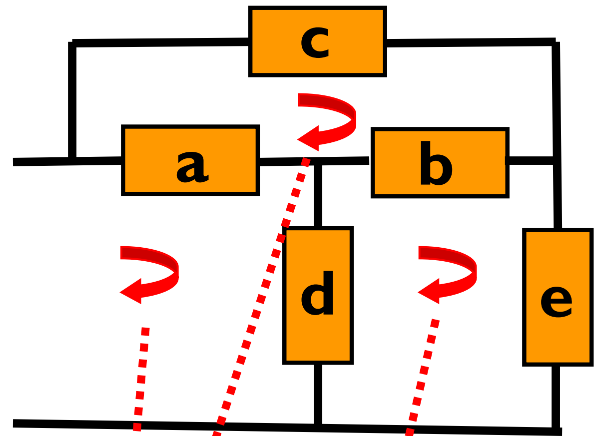
Solving [V]=[Z][I] for Zin= 1/Yin = R (Wang Algebra)

Yin=1/e →



Loop Equations:

a … e are impedances

e = R

$$\text{Yin} = \frac{\text{numerator}}{\text{denominator}} = \frac{(a+b+c)*\boxed{\text{W}}*(b+d+e)}{(a+d)*\boxed{\text{W}}*(\text{numerator})} = \boxed{\frac{1}{e}}$$

XX=0 →

X+X=0 → (after XX=0)

$$= \frac{ab+ad+ae+bb+bd+be+bc+cd+ce}{abd+abe+abc+acd+ace+abd+ade+bde+bcd+cde}$$

$$= \boxed{\frac{ab+ad+ae+bd+be+bc+cd+ce}{abc+abe+acd+ace+ade+bde+bcd+cde}}$$

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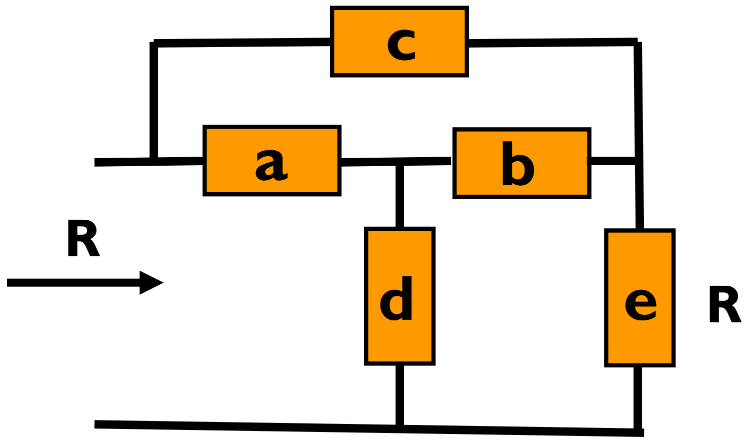
Constant R Constraint



General

$$d(a+b) + ab + R(a-b) - R^2 - \frac{R^2(a+b)}{c} = 0$$

Symmetric (a = b)

$$2da + a^2 - R^2 - \frac{2R^2 a}{c} = 0$$

Substitute impedances and equate powers of the Laplace variable "s" for constant R relationships

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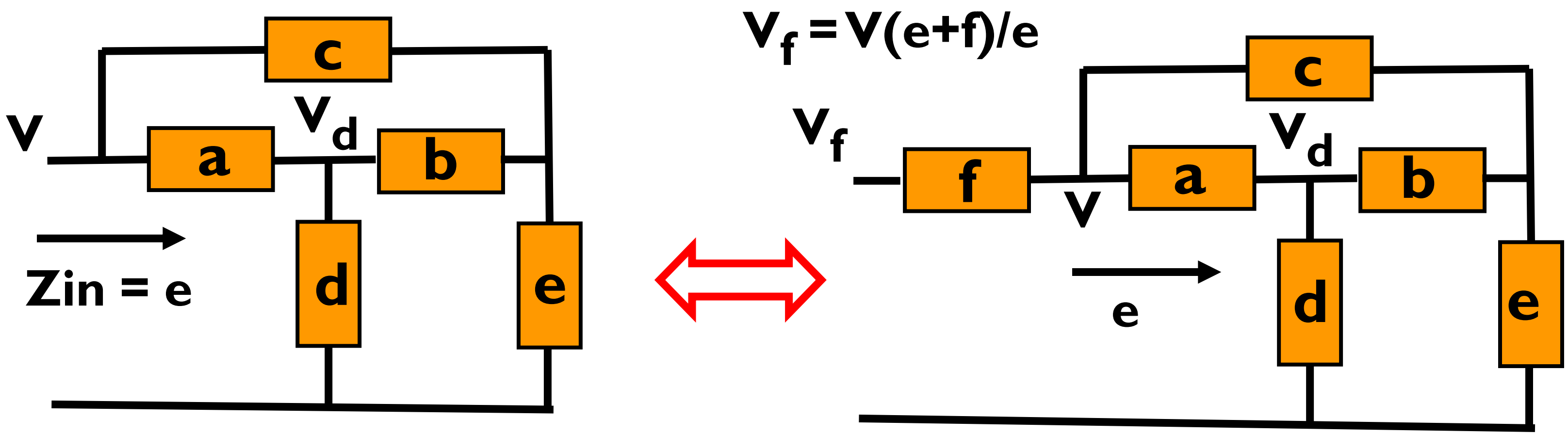
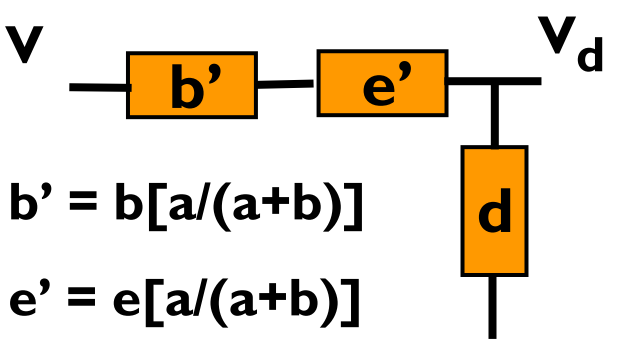
Constant Input Impedance Transfer Function Simplification



Thevenin Equivalent Circuit at V_d for Transfer Function



b' = b[a/(a+b)]

e' = e[a/(a+b)]

A constant impedance circuit plus "V_f" and "f" without loss of generality

The "f" is selected to null out "c" and reduce network complexity … next slide

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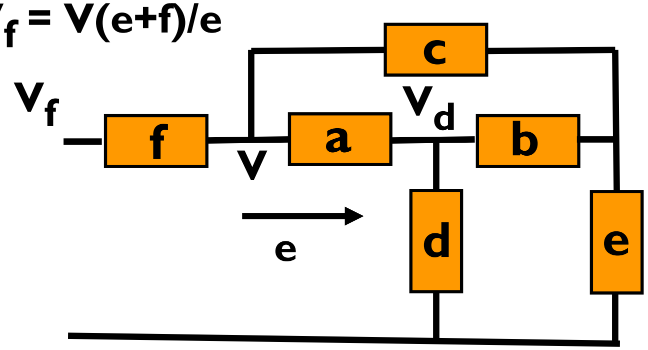
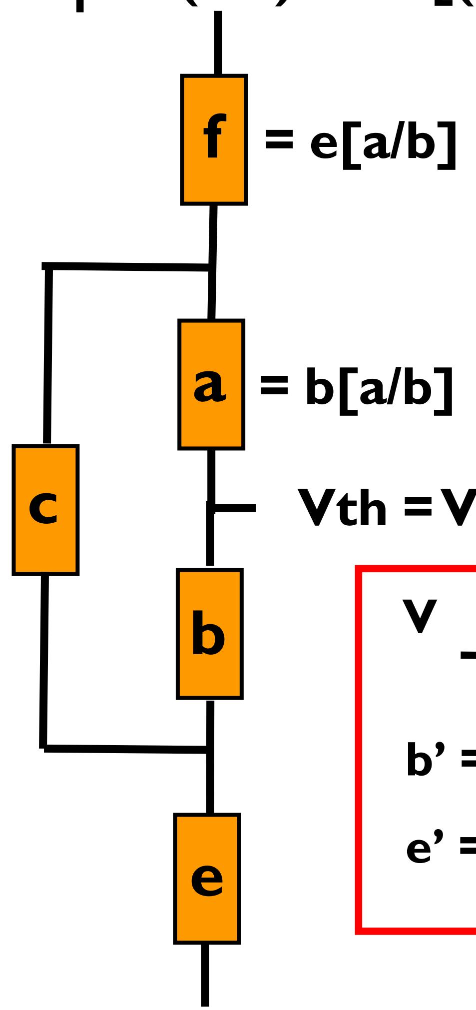
Thevenin Equivalent Derivation at Vd (for Vth and Zth)

$V_f = V(e+f)/e$

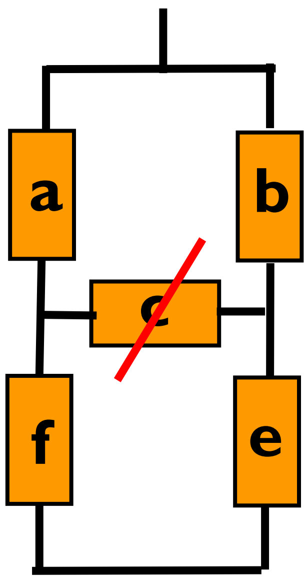


$V_f = V(e+f)/e = V[(a+b)/b]$



Relative values of f, a, b, and e imply Vth = V for any c

Zth

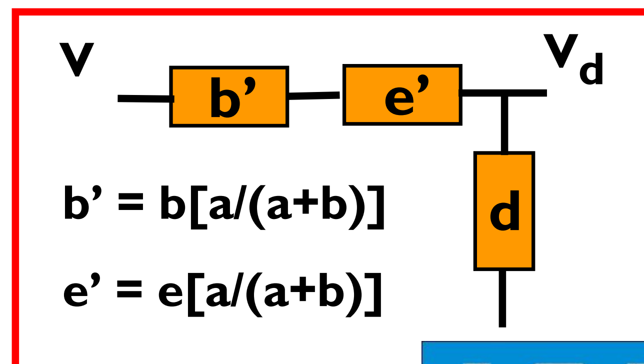


Set f = e[a/b] to null out c

Zth =

(b+e)||(a+f) =

(b+e)[a/(a+b)]



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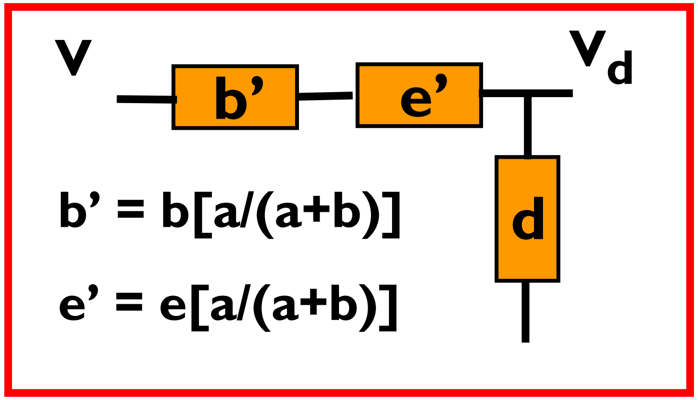
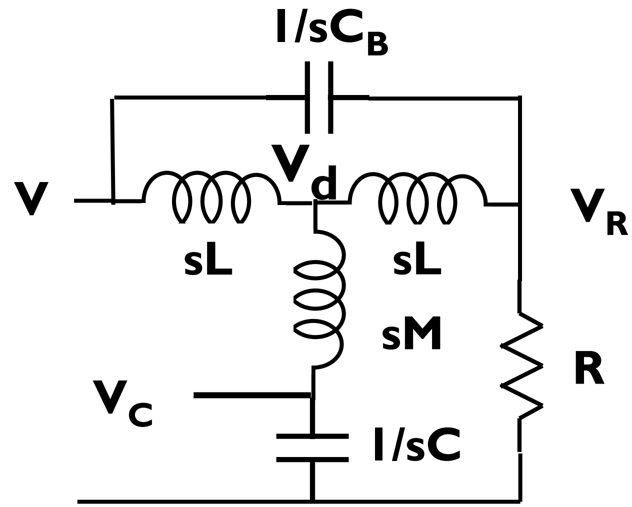
Simple Application (a=b)





b' = sL/2, e' = R/2, d = sM + 1/sC

$V_C/V = [1/s/C]/[(L/2 + M)s + R/2 + 1/sC]$

$V_C/V = 1/[R^2CC_Bs^2 + RCs/2 + 1]$

(from simplification and constant R constraint)

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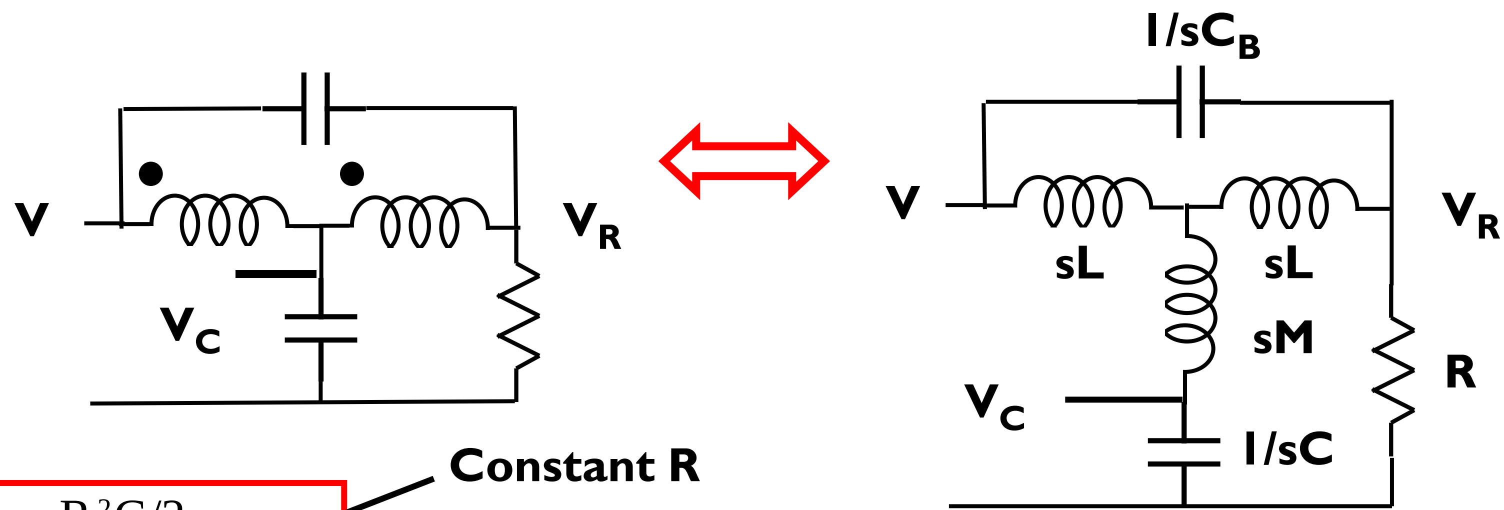
(Constant R) Bridged T-coil Example

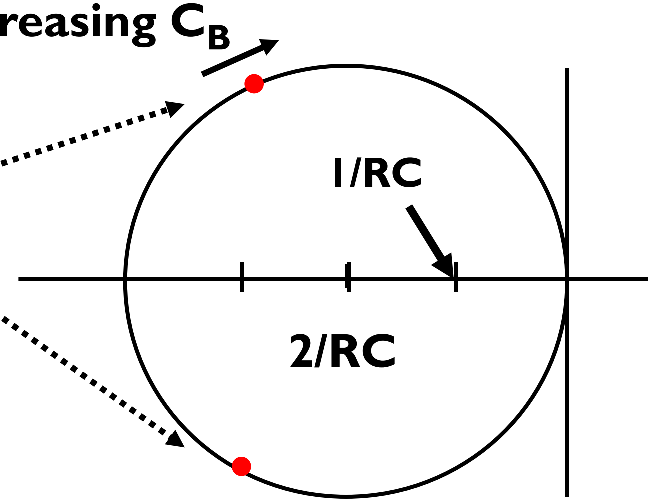


Constant R

$$L = R^2C/2$$
$$M = R^2C_B - L/2$$

$$\frac{V_C}{V} = \frac{1}{R^2CC_Bs^2 + \frac{RC}{2}s + 1}$$

$$\frac{V_R}{V} = \frac{R^2CC_Bs^2 - \frac{RC}{2}s + 1}{R^2CC_Bs^2 + \frac{RC}{2}s + 1}$$



Poles 30 degrees for maximally flat envelope delay (MFED)

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Historical Applications (1)

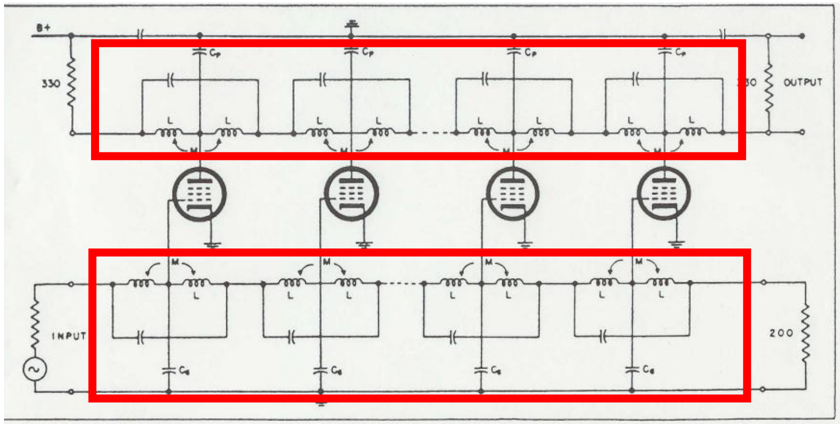
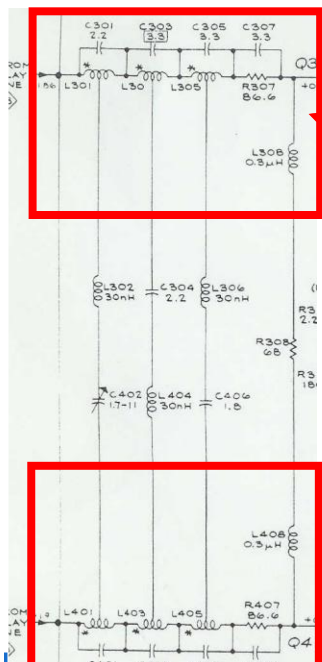
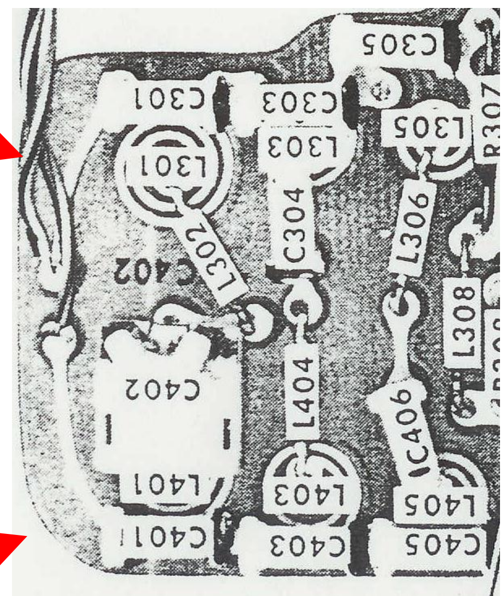


Figure 3. *Basic Amplifier Circuit Using Bridged-T Lines*

High speed (traveling wave) distributed amplifier in 1940's (Similar to GTL and source synchronous control)





Dual input delay line phase equalization using cascaded printed circuit board T-coils in 1960's

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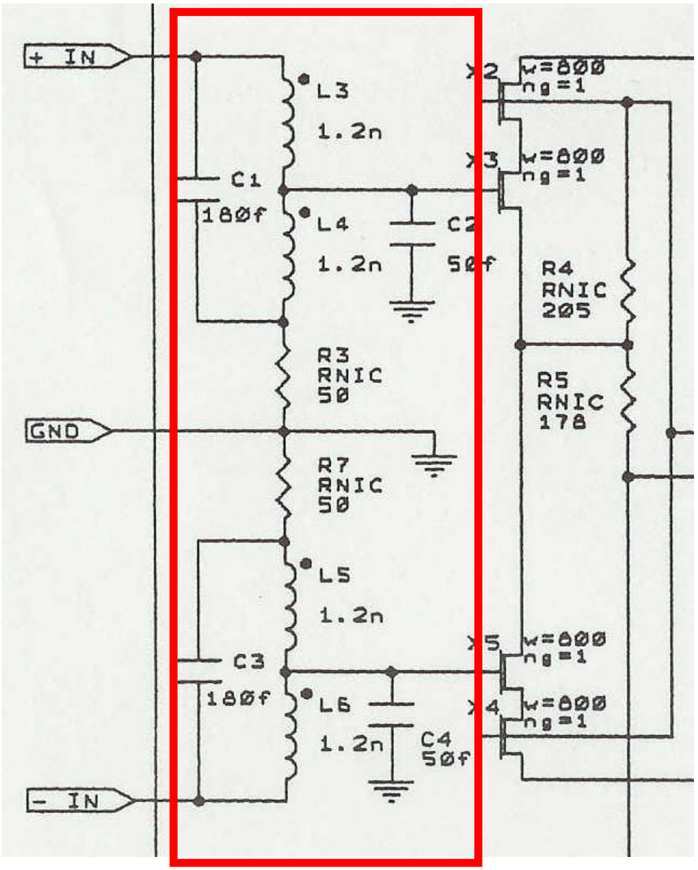
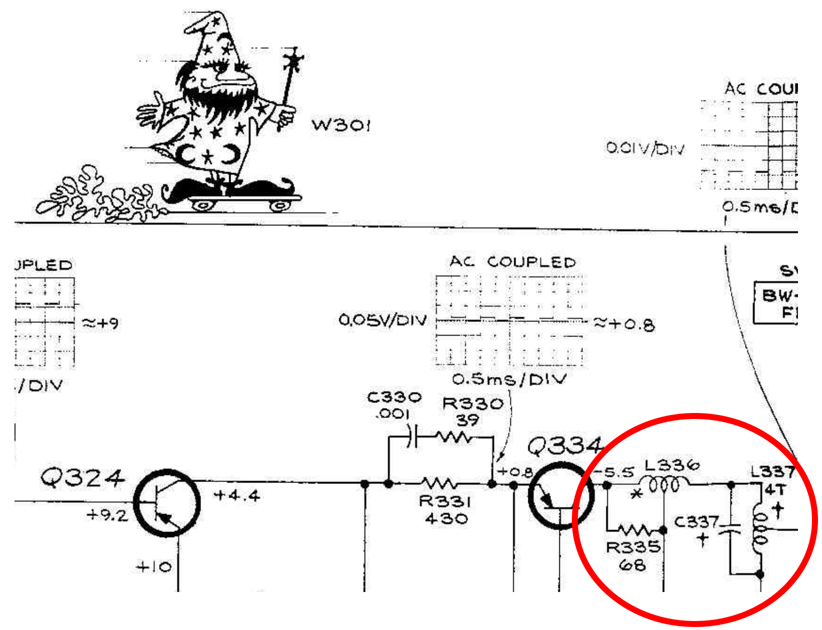
Historical Applications (2)



High speed 50 Ω input for FET hybrid IC and with metalization (not shown) for T-coils in 1990's



Parasitic bandwidth limit switch compensation and interstage peaking in 1960's (and W301)

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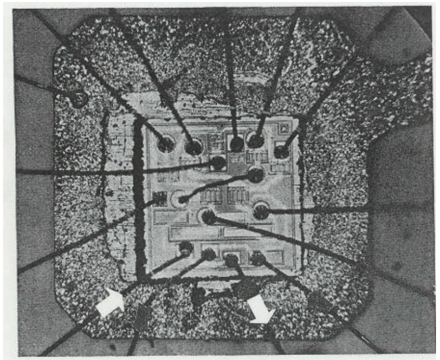
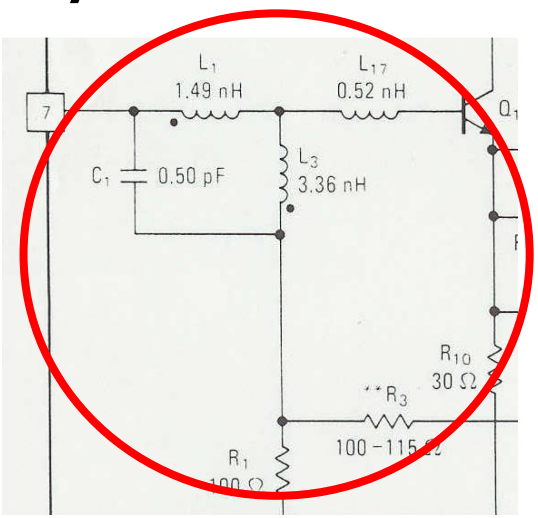
Historical Applications (3)

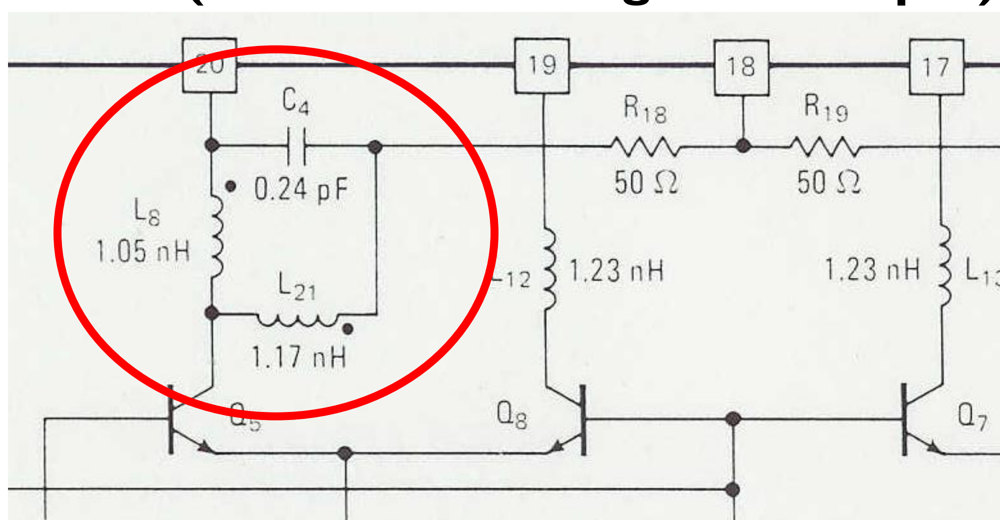


7. A chip trick. Tee-coil is realized by looping the input signals thrc

Package bond wire compensation with T-coil trick in 1970's

One-half of hybrid IC differential 50 Ω input and 50 Ω output with asymmetrical T-coils in 1970's (Current mode logic-like output)





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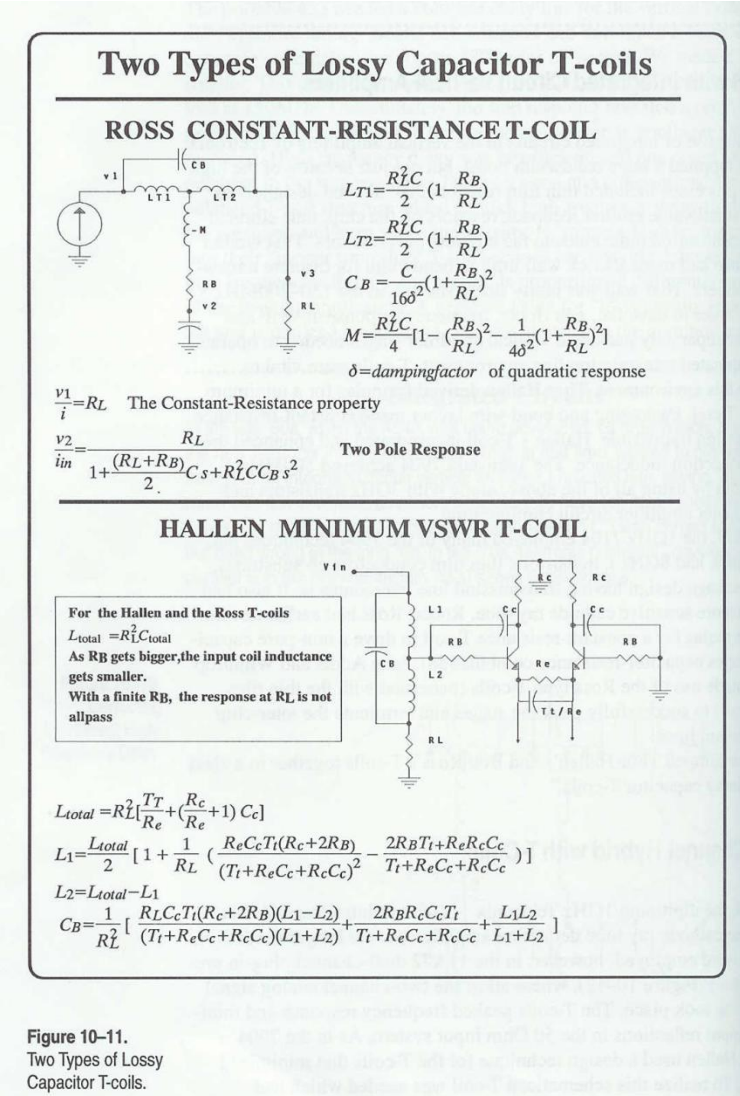
Early Asymmetrical Lossy T-coils



Two Types of Lossy Capacitor T-coils

ROSS CONSTANT-RESISTANCE T-COIL

$$L_{T1}=\frac{R_L^2C}{2}(1-\frac{R_B}{R_L})$$

$$L_{T2}=\frac{R_L^2C}{2}(1+\frac{R_B}{R_L})$$

$$C_B=\frac{C}{16\delta^2}(1+\frac{R_B}{R_L})^2$$

$$M=\frac{R_L^2C}{4}[1-(\frac{R_B}{R_L})^2-\frac{1}{4\delta^2}(1+\frac{R_B}{R_L})^2]$$

$\delta = dampingfactor$ of quadratic response

$\frac{v1}{i}=R_L$ The Constant-Resistance property

$$\frac{v2}{iin}=\frac{R_L}{1+\frac{(R_L+R_B)}{2}Cs+R_L^2CC_Bs^2}$$

Two Pole Response

HALLEN MINIMUM VSWR T-COIL

For the Hallen and the Ross T-coils
$L_{total}=R_L^2C_{total}$
As RB gets bigger, the input coil inductance gets smaller.
With a finite RB, the response at RL is not allpass

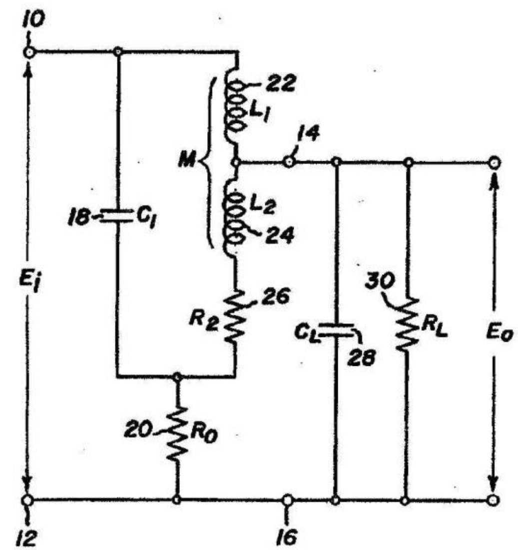
$$L_{total}=R_L^2[\frac{T_T}{R_e}+(\frac{R_c}{R_e}+1)C_c]$$

$$L_1=\frac{L_{total}}{2}[1+\frac{1}{R_L}(\frac{R_eC_cT_t(R_c+2R_B)}{(T_t+R_eC_c+R_cC_c)^2}-\frac{2R_BT_t+R_eR_cC_c}{T_t+R_eC_c+R_cC_c})]$$

$$L_2=L_{total}-L_1$$

$$C_B=\frac{1}{R_L^2}[\frac{R_LC_cT_t(R_c+2R_B)(L_1-L_2)}{(T_t+R_eC_c+R_cC_c)(L_1+L_2)}+\frac{2R_BR_cC_cT_t}{T_t+R_eC_c+R_cC_c}+\frac{L_1L_2}{L_1+L_2}]$$

Figure 10–11.
Two Types of Lossy Capacitor T-coils.



T.T. True patent (1964)

Tuned for bipolar transistor technology

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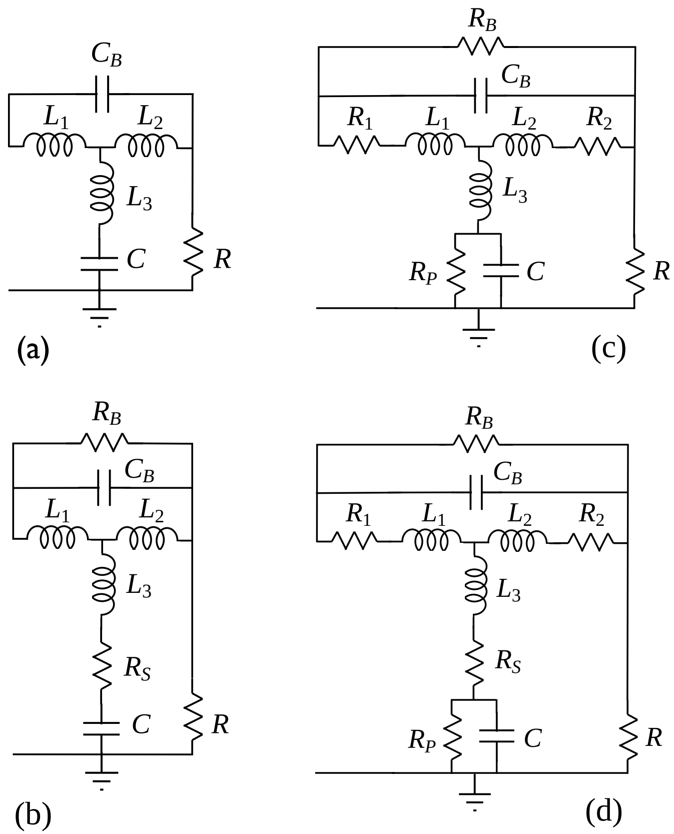
Constant Input-R, 2nd Order Extensions

Standard

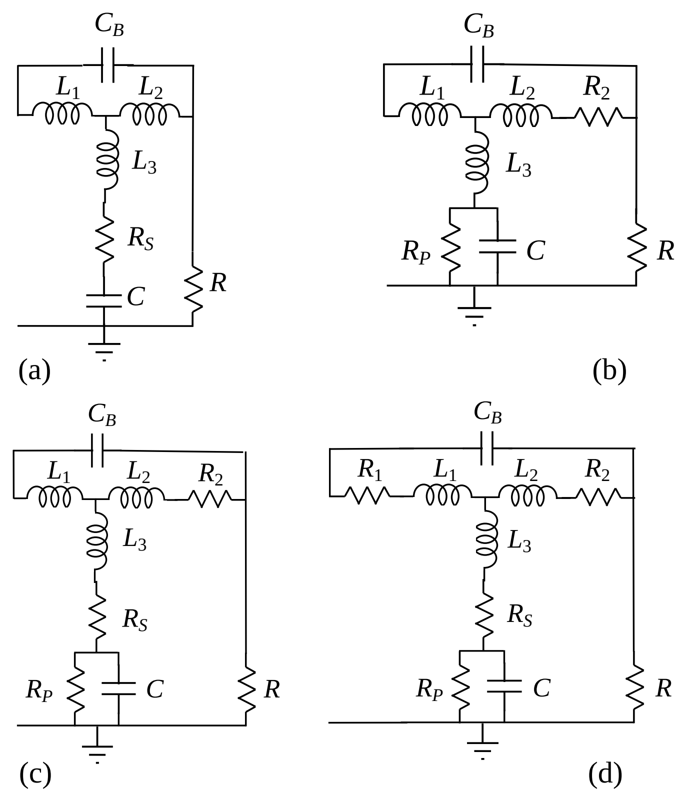


General

Fig. 1
Symmetrical (Z_1=Z_2),
R_B added

Series Rs

T.T. True



General

Fig. 2
Asymmetrical
(Z_1 not = Z_2)

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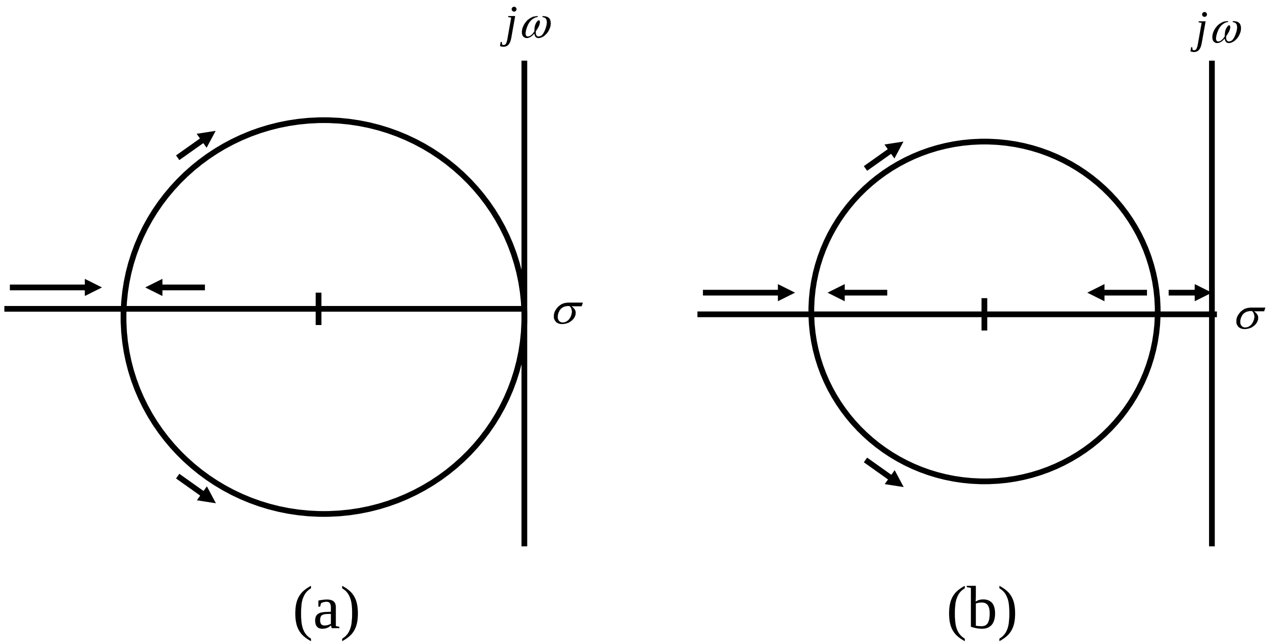
2^{nd} Order Root Loci for Increasing C_B: (a) without R_P, D_1=0 (b) with R_P



$$\frac{V_C}{V} = \frac{1}{B_0 + B_1 s + B_2 s^2} = \frac{1}{B_0 + (D_0 + D_1 C_B)s + D_2 C_B s^2}.$$

$$\text{center} = -\frac{B_0}{D_0}, \quad \text{radius} = \frac{B_0}{D_0}\sqrt{1 - \frac{D_0 D_1}{B_0 D_2}}.$$

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Examples for all Extensions

	$R = 50\ \Omega$, $C = 4$ pF, $R_S = 10\ \Omega$, $R_P = 500\ \Omega$, Pole Angle = 30^o & 45^o, R_1 selected for Fig. 2(d)							
	Symmetrical T-Coils				Asymmetrical T-Coils			
Load	Standard C	R_S-C	$R_P C$	R_S-$R_P C$	R_S-C	$R_P C$	R_S-$R_P C$	Gen. R_S-$R_P C$
Fig.	1(a)	1(b)	1(c)	1(d)	2(a)	2(b)	2(c)	2(d)
R_1			2.5 Ω	2.5 Ω				1.907 Ω
R_2			2.5 Ω	2.5 Ω		5.556 Ω	5.435 Ω	3.100 Ω
R_B		250 Ω	2000 Ω	222.2 Ω				
L_1	5 nH	5 nH	5.025 nH	5.025 nH	4 nH	5.409 nH	4.257 nH	3.888 nH
L_2	5 nH	5 nH	5.025 nH	5.025 nH	6 nH	5.702 nH	6.612 nH	6.127 nH
Gain	1	1	0.95	0.95	1	1	0.98	0.943
C_B (30^o)	0.333 pF	0.653 pF	0.362 pF	0.698 pF	0.480 pF	0.364 pF	0.504 pF	0.489 pF
L_3	(-1.667 nH)	(-0.867 nH)	(-1.609 nH)	(-0.767 nH)	(-1.200 nH)	(-1.867 nH)	(-1.330 nH)	(-1.154 nH)
BW	2.167 GHz	1.548 GHz	2.136 GHz	1.536 GHz	1.806 GHz	2.075 GHz	1.780 GHz	1.841 GHz
BWER	2.723	1.945	2.684	1.930	2.269	2.607	2.237	2.314
GBWER	2.723	1.945	2.550	1.834	2.269	2.607	2.193	2.182
C_B (45^o)	0.500 pF	0.980 pF	0.552 pF	1.074 pF	0.720 pF	0.556 pF	0.772 pF	0.750 pF
L_3	(-1.250 nH)	(-0.050 nH)	(-1.133 nH)	0.173 nH	(-0.600 nH)	(-1.387 nH)	(-0.659 nH)	(-0.504 nH)
BW	2.251 GHz	1.608 GHz	2.198 GHz	1.575 GHz	1.876 GHz	2.135 GHz	1.829 GHz	1.893 GHz
BWER	2.828	2.020	2.763	1.980	2.357	2.683	2.298	2.378
GBWER	2.828	2.020	2.625	1.881	2.357	2.683	2.253	2.243

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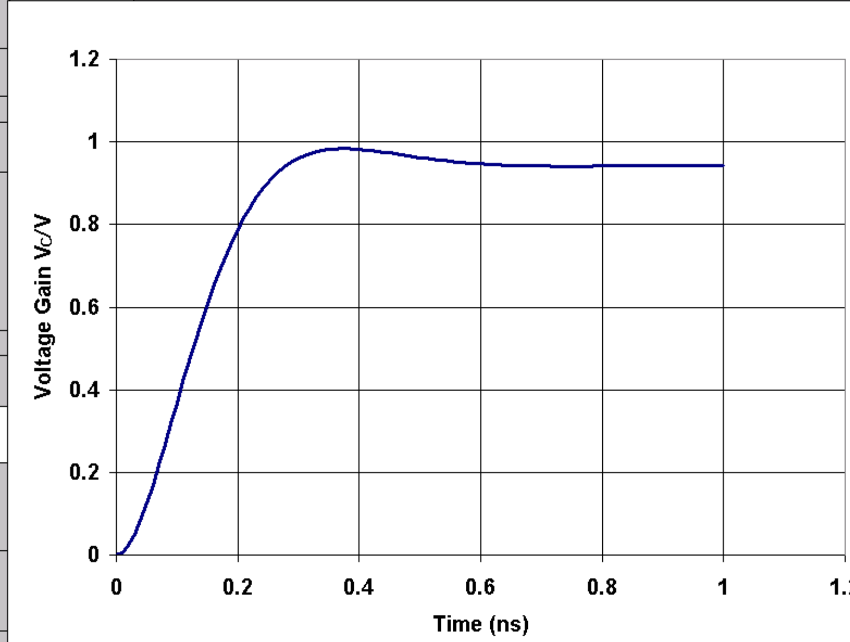
General Asymmetrical Calculations

Bridged T-Coil Input		
R	50	
C (pF)	4	C (nF) 0.004
R_S	10	
G_P $(1/R_P)$	0.002	R_P 500
R_1	1.9073	
T-step (ns)	0.01	
Theta (deg)	45	

Calculated Values		Value, Formulas
C_B (pF)	0.749874203	C_B (nF) 0.000749874
R_1	1.9073	Choose R_1 above so that R_2 >= 0
R_2 (Check R_2>=0)	3.099998636	$R_2=[R^2G_P-R_1(1+G_P(R_S+R)]/[1+G_P(R_1+R_S-R)]$
L_1+L_2 (nH)	10.01459727	$\{(R-R_1)^2/[1+G_P(R_1+R_S-R)]\}C$
L_1 (nH)	3.887559745	$(R_1-R)(R_1+R_S-R)/\{1+[(1+G_P(R_1+R_S-R)]+[1+G_P(R_1+R_S-R)]^{1/2}\}*C$
L_2 (nH)	6.127037527	
L_3 (nH)	-0.503765048	$R^2C_B-L_1L_2/(L_1+L_2)$



$V_C/V=1/(B_0+(D_0+D_1C_B)s+D_2C_Bs^2)$		
B_0	1.060452002	$1+RG_P+(RR_SG_P-R_2)/(R+R_2)$
D_0	0.122362135	$RCL_2/(L_1+L_2)$
D_1	5	R^2G_P
D_2	10	R^2C

Gain and BW Parameters	
0.942994118	Gain
1.892654898	3 dB BW (GHz)
2.37838029	BW Multiplier
0.795774715	Reference RC-BW GHz
2.242798623	GBW-Mulitplier

Pole Roots		
Center	-8.666504555	$-B_0/D_0$

Parameterized SPICE Automatic T-coil Design Subcircuit

```
****************************************************
*ASYMMETRICAL T-COIL WITH PARAMETERS
****************************************************

****************************************************
* PARAMETERS
****************************************************
** ENTER
.param R = 50                               $ Load Resistor
.param C = 4e-12                            $ Load Capacitance
.param RS = 10  $ set 'max(1e-10, 10)'      $ Series Resistor
.param RP = 500 $ set 'max(1e-10, 500)'     $ Parallel Resistor
.param CB = 0.653p
.param R1 = 2   $ set 'max(1e-10, 2)'       $ Select R1 with RP>0
** CALCULATED
.Param GP = '1/RP'                          $ Parallel Conductance
.param R2 = 'max(1e-10,(R*R*GP-R1*(1+(RS+R)*GP))/(1+(R1+RS-R)*GP))'
.param LT = '(R-R1)*(R-R1)*C/(1+(R1+RS-R)*GP)'
.param L1 = '(R1-R)*(R1+RS-R)*C/(1+(R1+RS-R)*GP+SQRT(1+(R1+RS-R)*GP))'
.param L2 = 'LT-L1'
.param L3 = 'R*R*CB-L1*L2/(L1+L2)'
*
****************************************************
* ASYMMETIRCAL T-COIL CIRCUIT (Ground = 0)
****************************************************
*
XCOIL1 in outc  outr TCOIL_ASM
RLOAD  0  outr  R='R'
*
****************************************************
* SUBCKT: TCOIL_CONSTANT RESISTANCE T-COIL (RL)
****************************************************
.SUBCKT TCOIL_ASM in outc outr
*
L1  1     d     L='L1'
L2  2     d     L='L2'
R1  in    1     R='R1'
R2  outr  2     R='R2'
CB  in    outr  C='CB'
*
L3  d     3     L='L3'  $ Negative L3 ok
RS  3     outc  R='RS'
C   outc  0     C='C'
RP  outc  0     R='RP'
.ENDS
*
****************************************************
```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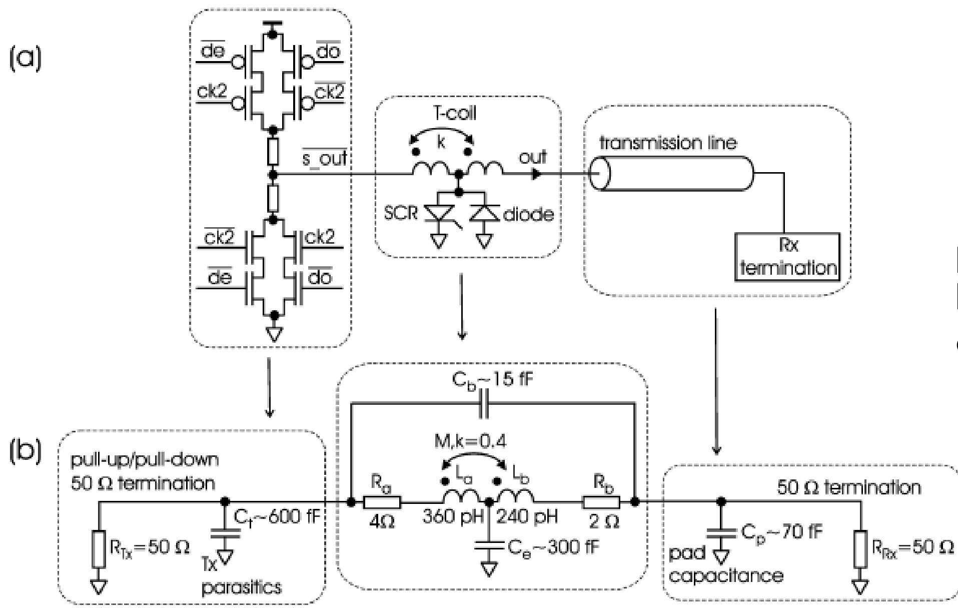
More Recent Work in Last 10 Years (dozens of contributions)

- Technical literature (journals, conferences, thesis, and patents) for up to 40 Gb/s designs
- T-coil types
  - Standard
  - Extended – multiple higher order with/without bridging capacitance
  - Sometimes with other C's and losses
- Part of high speed designs
  - ESD compensation
  - Acceptable (but not 0) S11 and extended (>4) S21 bandwidths
  - Up to 5th order to polynomials fitted by (Bessel coefficients, optimization or approximation equations)
- Inductance structure contributions
- Splitting the C load strategies for better performance

Example of a Recent IC T-Coil Application



Low S11 with a forth order polynomial extension and lossy fabrication for ESD compensation

M. Kossel, C. Menolfi, J. Weiss, P. Buchmann, G. von Bueren, L. Rodoni, T. Morf, T. Torifl, and M. Schmaltz, "A T-Coil-Enhanced 8.5 Gb/s High Swing SST Transmitter in 65 nm Bulk CMOS With < -16 dB Return Loss Over 10 GHz Bandwidth," IEEE J. Solid-State Circuits, Dec. 2008

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Summary

- Some T-coil background and history
- Second order extensions for lossy design applications
  - Due to more detailed load models
  - Due to inductor fabrication losses
  - Parameterized by C_B for greater solution space versus often used inductor coupling coefficient
  - Used in current IC buffer design including SerDes
- T-coils can be a factor in IBIS-AMI and IBIS-ISS applications

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