

Nokia Siemens Networks



IBIS [Driver Schedule] modeling

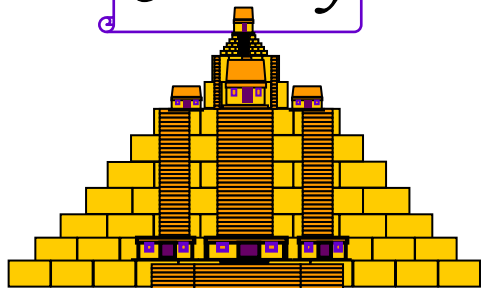
Eckhard Lenski

SPI , Hildesheim , Germany

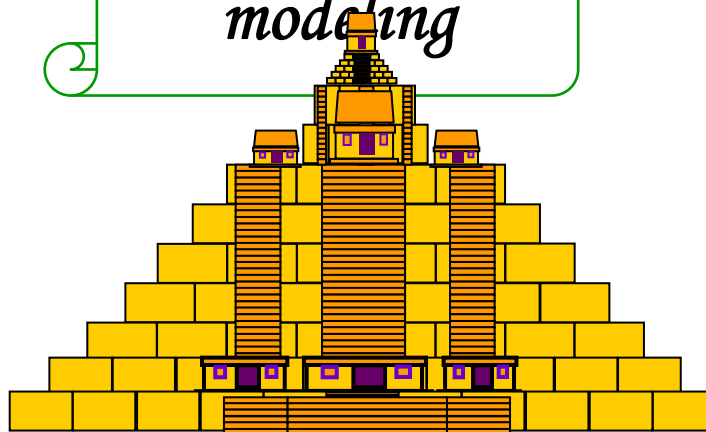
12th May 2010



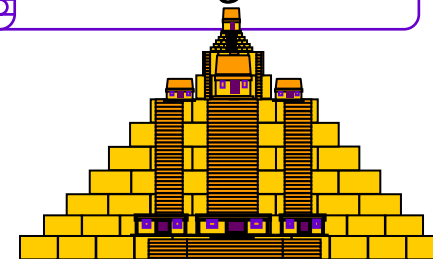
Summary



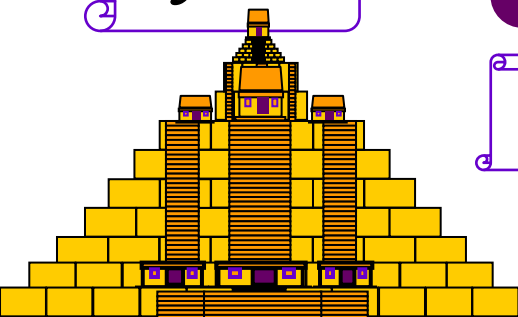
IBIS
driver schedule
modeling



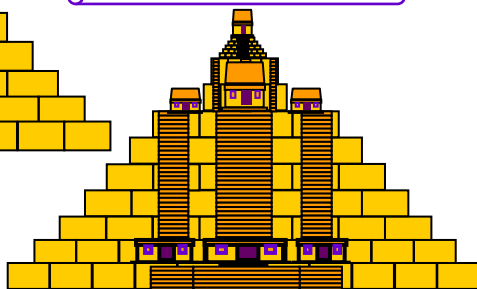
Driver schedule
Design 1



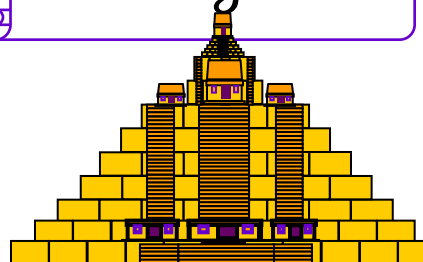
Package
influence



Static check



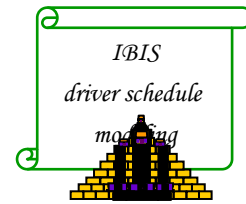
Driver schedule
Design 3



Driver schedule
Design 2



driver schedule static curves



[Model] 2-Driver-schedule

[Voltage Range] 3.30V 3.1350V 3.4650V

[GND Clamp]

[POWER Clamp]

[Pulldown]

[Pullup]

[Driver Schedule]

MODEL_1	0s	NA	0ns	NA
MODEL_2	0.5ns	NA	0ns	NA

[Model] Model_1

[GND Clamp]

[POWER Clamp]

[Pulldown]

[Pullup]

[Model] Model_2

[GND Clamp]

[POWER Clamp]

[Pulldown]

[Pullup]

Top level model tables

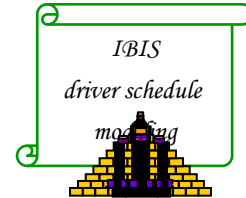
Driver schedule timing

Scheduled model tables

General timing schedule

[Driver Schedule]

Model_name	Rise_on_dly	Rise_off_dly	Fall_on_dly	Fall_off_dly
MODEL_1	0.5ns	NA	0ns	NA
MODEL_2	1.0ns	NA	0ns	NA
MODEL_3	1.5ns	2.5ns	NA	NA



Model_name	Rise_on_dly	Rise_off_dly	Fall_on_dly	Fall_off_dly
------------	-------------	--------------	-------------	--------------



turn on pullup-
structure

turn off pullup-
structure

turn on pulldown-
structure

turn off pulldown-
structure





turn off pulldown-
structure

turn on pulldown-
structure

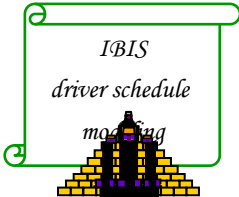
turn off pullup-
structure

turn on pullup-
structure

scheduled models timing parameter

	rising edge (L->H)		falling edge (H->L)	
Model_name	Rise_on_dly	Rise_off_dly	Fall_on_dly	Fall_off_dly
MODEL_1	1.0ns	2.5ns	0ns	NA
				
	turn on pullup- structure	turn off pullup- structure	turn on pulldown- structure	turn off pulldown- structure
	turn off pulldown- structure	turn on pulldown- structure	turn off pullup- structure	turn on pullup- structure

timing schedule vs datarate



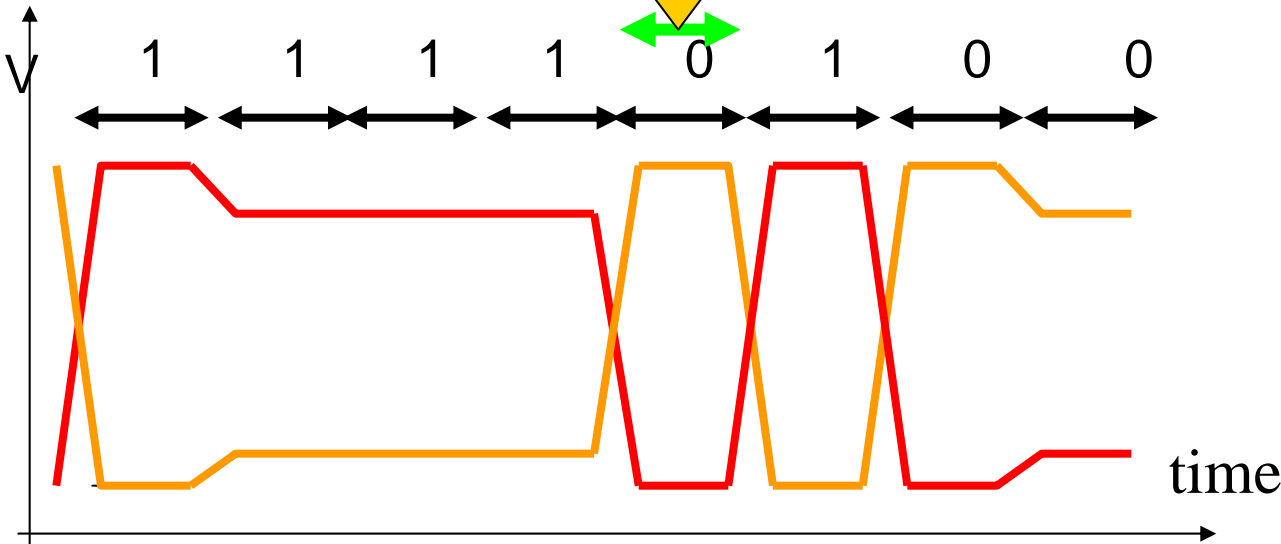
[Driver Schedule]

Model_name	Rise_on_dly	Rise_off_dly	Fall_on_dly	Fall_off_dly
MODEL_1	0.0ns	NA	0ns	NA
MODEL_2	NA	0.4ns	NA	0.4ns

Model valid for one specific datarate

UI corresponds to Datarate

Eg.
UI 400ps
2.5 Gbps



data pattern
11110100



Driver schedule Design 1

Summary

IBIS
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modeling

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Design 1

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influence

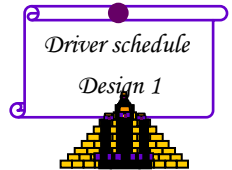
Static check

Driver schedule
Design 3

Driver schedule
Design 2

Example 1 timing schedule opsink plus opsink

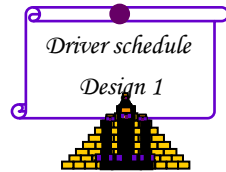
[Driver Schedule]



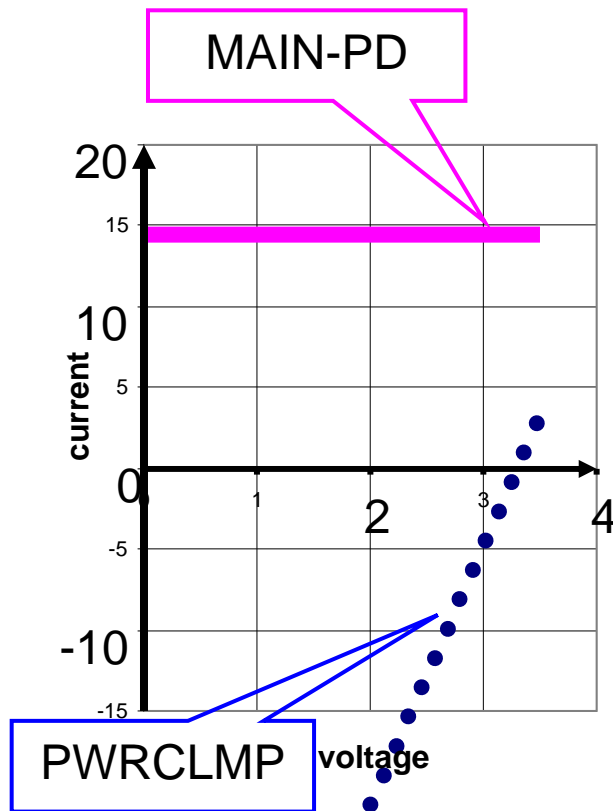
	Model_name	Rise_on_dly	Rise_off_dly	Fall_on_dly	Fall_off_dly
1	3P3V_DRI-NSN-1+3_OUT	0.000ns	NA	0.000ns	NA
2	3P3V_DRI-NSN-1+4_OUT	NA	0.800ns	NA	0.800ns
		↑	↑	↑	↑
1	turn on PU	turn off PU	turn on PD	turn off PD	turn on PU
	turn off PD	turn on PD	turn off PU	turn on PU	
		↑	↑	↑	↑
2	turn on PU	turn off PU	turn on PD	turn off PD	turn on PU
	turn off PD	turn on PD	turn off PU	turn on PU	

Don't forget the clamp currents from the top level model, if any

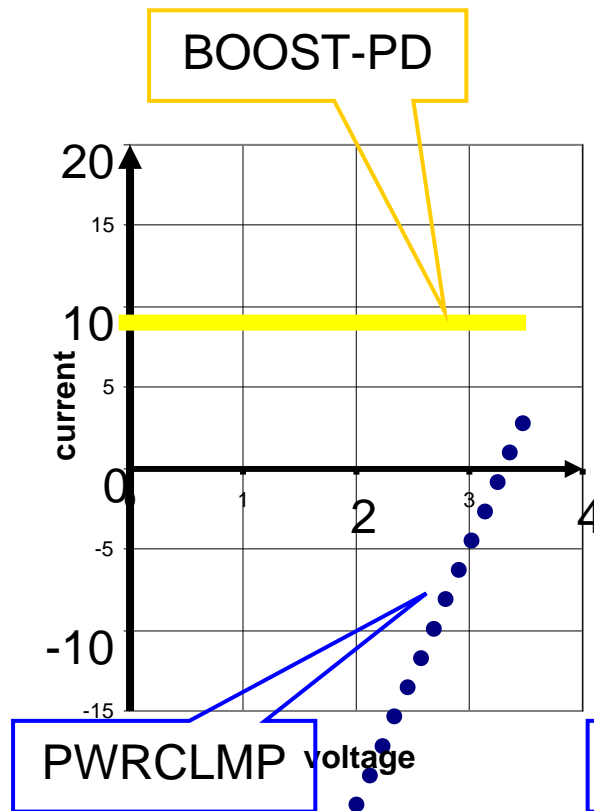
Example 1 static curves



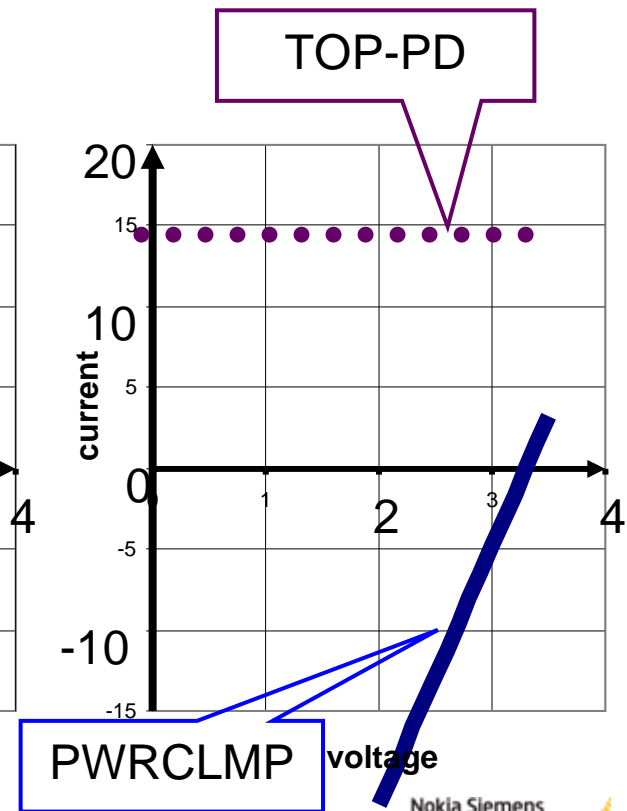
- Main Model open-sink



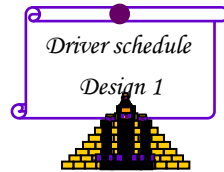
- Boost-1 Model open-sink



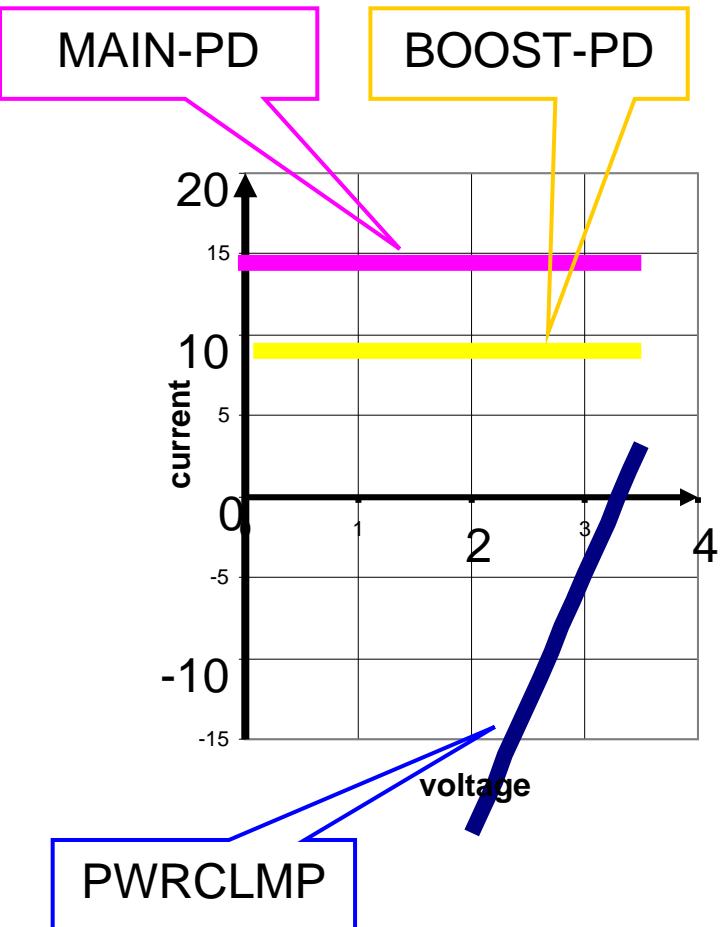
- Toplevel Model open-sink



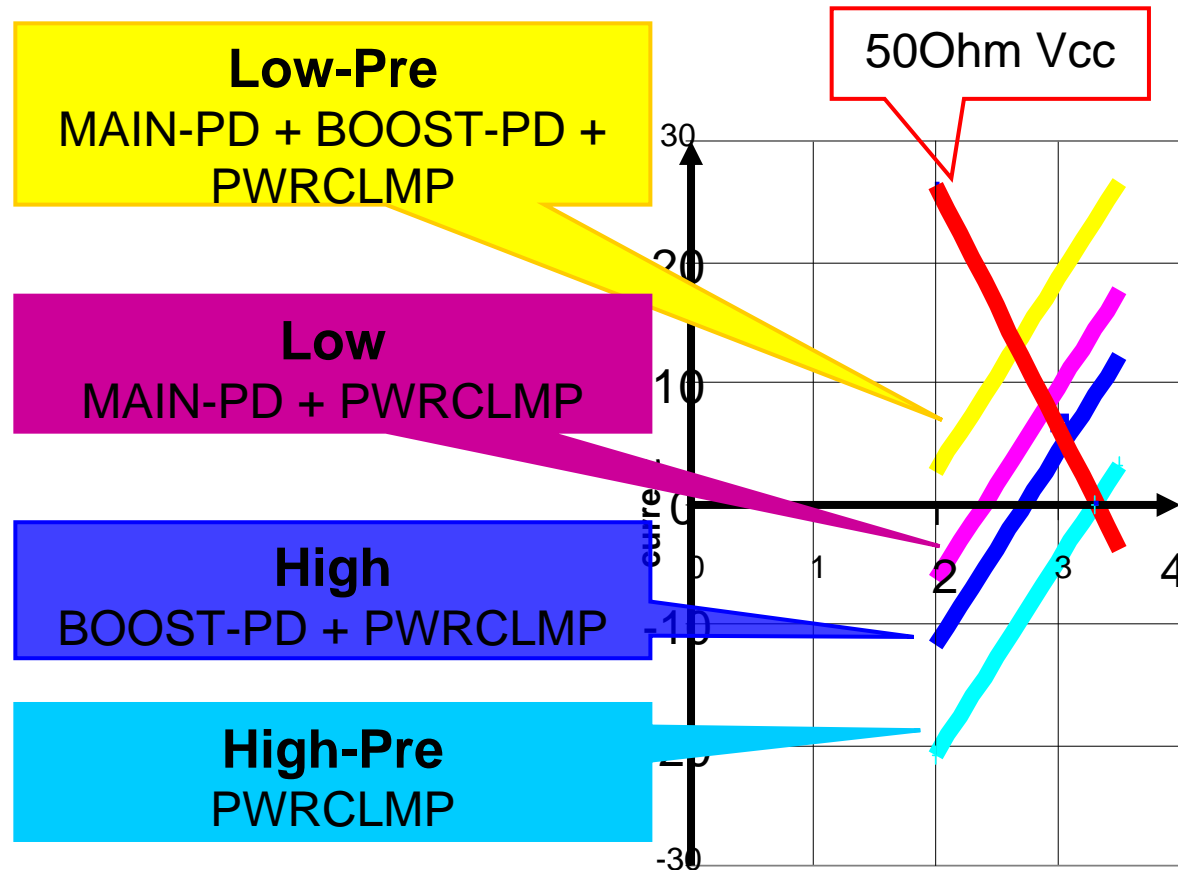
Example 1 combined static curves



- static curves
- In one diagram



- combined curves
- HIGH-Pre / HIGH / LOW / LOW-Pre



Driver schedule

Design 2

Summary

*IBIS
driver schedule
modeling*

*Driver schedule
Design 1*

*Package
influence*

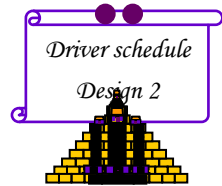
Static check

*Driver schedule
Design 3*

*Driver schedule
Design 2*

Example 2 timing schedule pu pd plus opsink & opsource

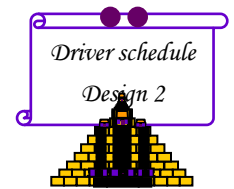
[Driver Schedule]



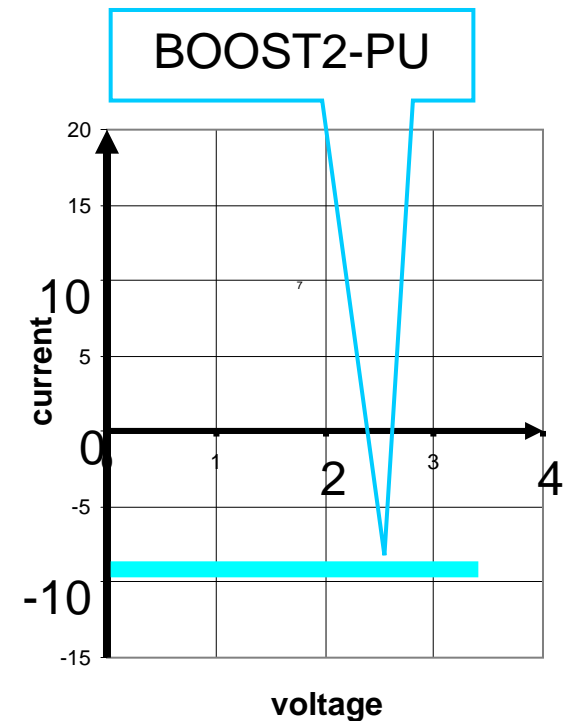
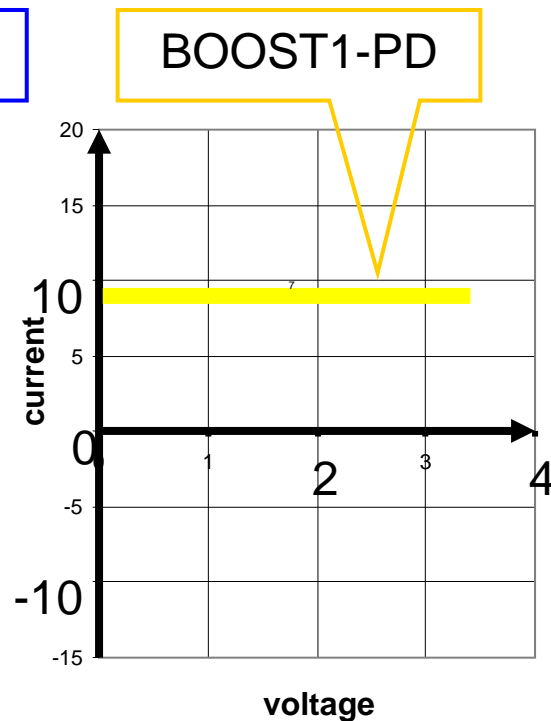
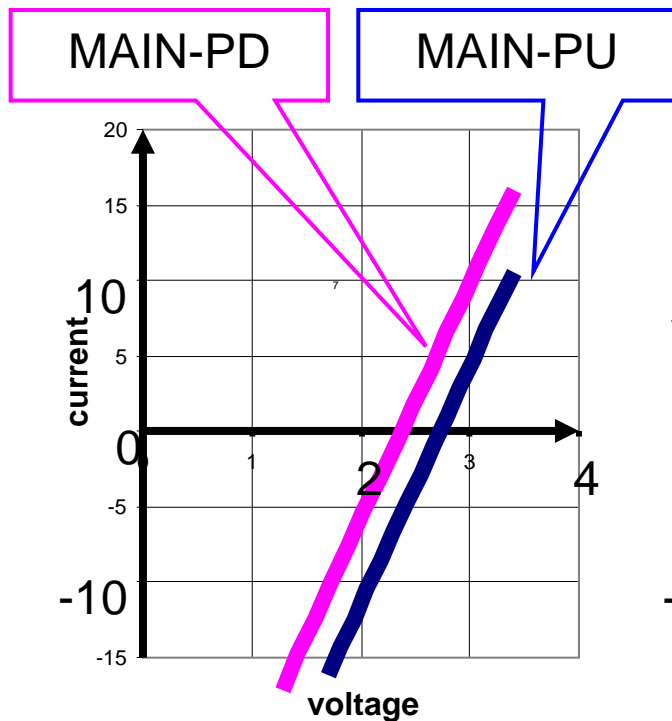
|Model_name Rise_on_dly Rise_off_dly Fall_on_dly Fall_off_dly

1	3P3V_DRI-NSN-CML-PREOFF_OUT	0.000ns	NA	0.000ns	NA
2	3P3V_DRI-NSN-CML-PRELO_OUT	NA	NA	0.000ns	2.000ns
3	3P3V_DRI-NSN-CML-PREHI_OUT	0.000ns	2.000ns	NA	NA
		↑	↑	↑	↑
	1	turn on PU turn off PD	turn off PU turn on PD	turn on PD turn off PU	turn off PD turn on PU
		↑	↑	↑	↑
	2	turn on PU turn off PD	turn off PU turn on PD	turn on PD turn off PU	turn off PD turn on PU
		↑	↑	↑	↑
	3	turn on PU turn off PD	turn off PU turn on PD	turn on PD turn off PU	turn off PD turn on PU

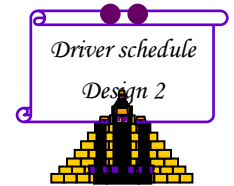
Example 2 static curves



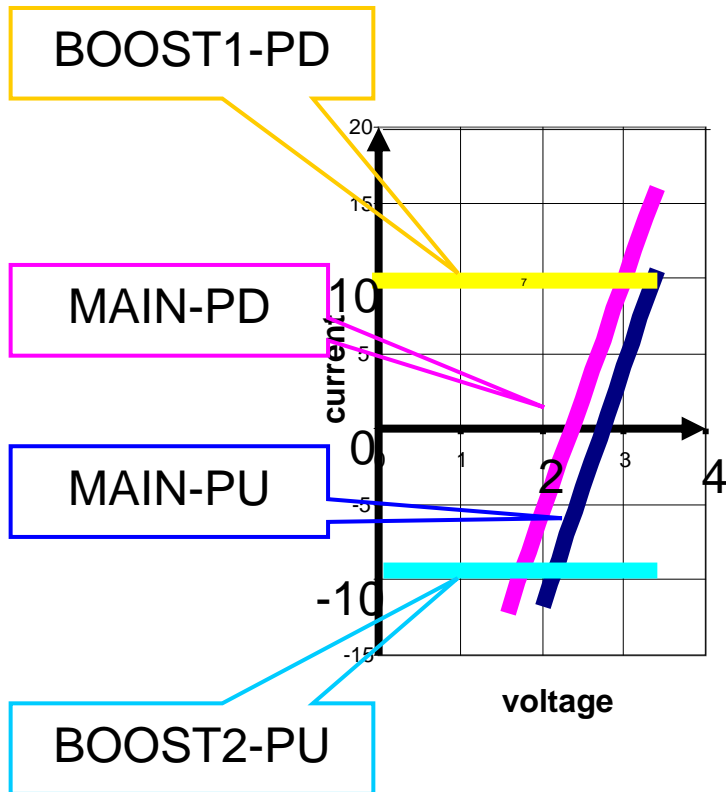
- Main Model with pullup and pulldown (*also Toplevel model*)
- Boost-1 Model open-sink
- Boost-2 Model open-source



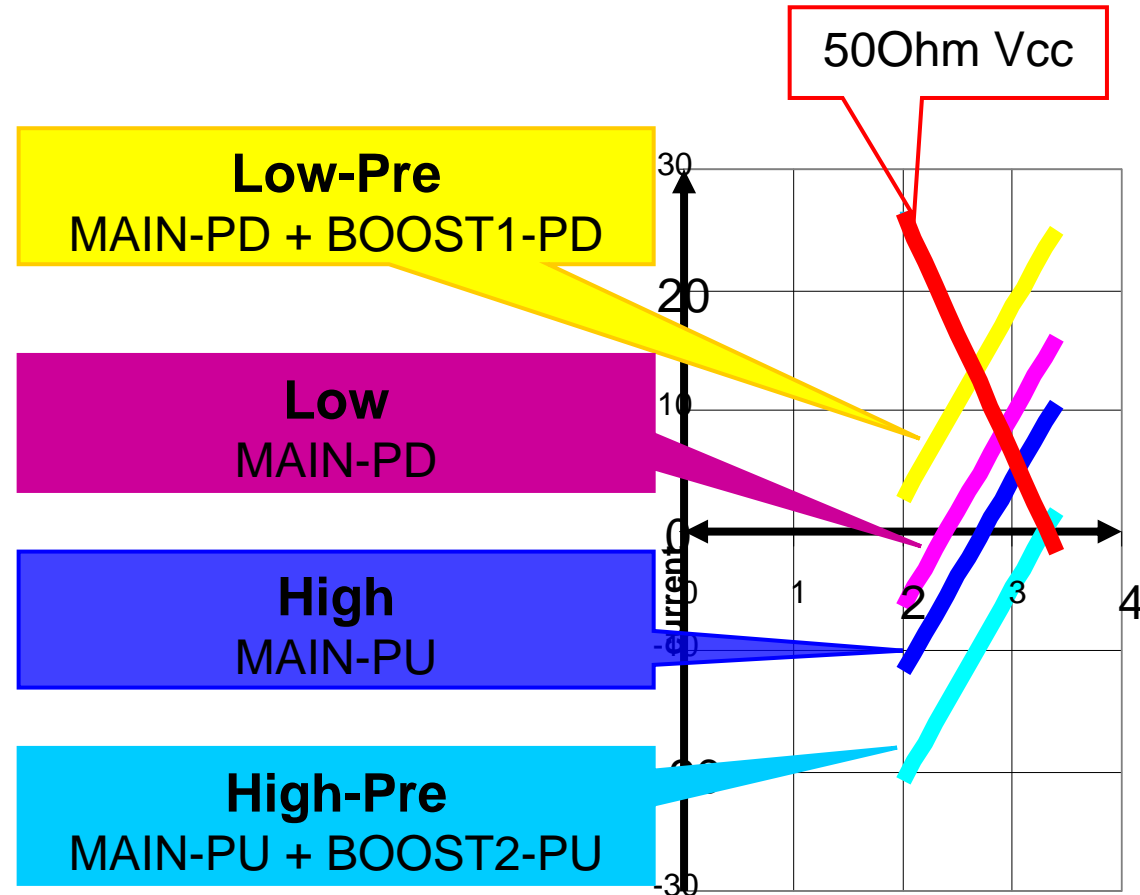
Example 2 combined static curves



- static curves in one diagram



- combined curves
- HIGH-Pre / HIGH / LOW / LOW-Pre



Driver schedule Design 3

Summary

IBIS
driver schedule
modeling

Driver schedule
Design 1

Package
influence

Static check

Driver schedule
Design 3

Driver schedule
Design 2

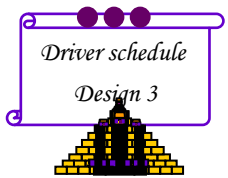
Example 3 timing schedule

pu pd plus pu pd

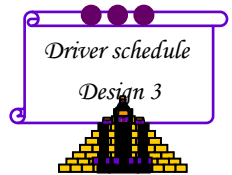
[Driver Schedule]

|Model_name Rise_on_dly Rise_off_dly Fall_on_dly Fall_off_dly

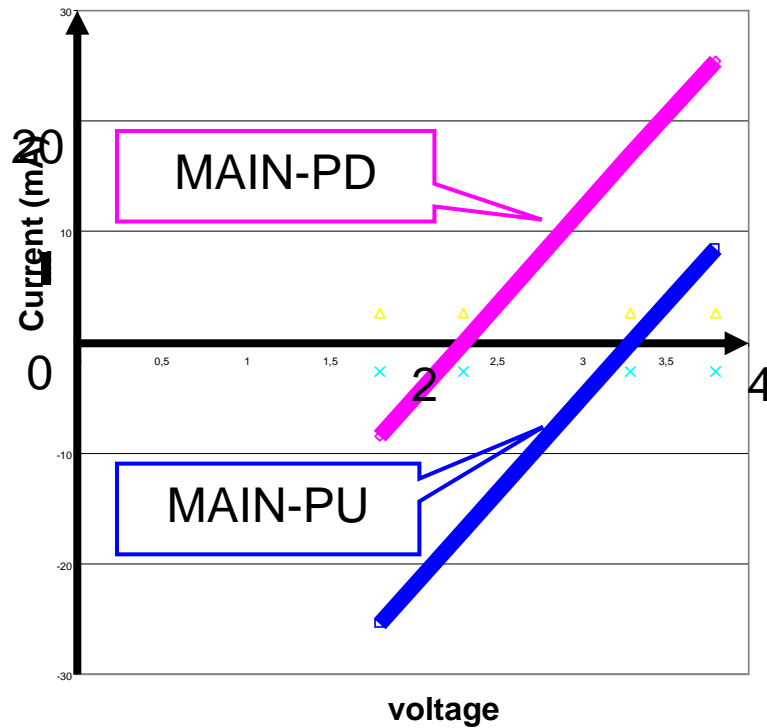
1	3P3V_DRI-NSN+MAIN_OUT	0.000ns	NA	0.000ns	NA
2	3P3V_DRI-NSN+BOOST_OUT	0.400ns	NA	0.400ns	NA
		↑	↑	↑	↑
	1	turn on PU turn off PD	turn off PU turn on PD	turn on PD turn off PU	turn off PD turn on PU
		↑	↑	↑	↑
	2	turn on PU turn off PD	turn off PU turn on PD	turn on PD turn off PU	turn off PD turn on PU



Example 3 static curves

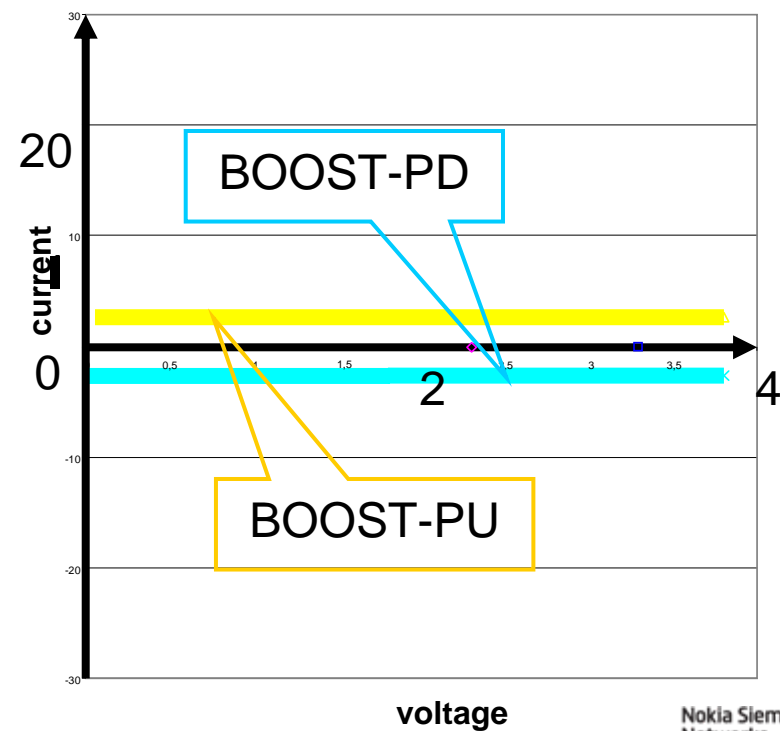


- Main Model
with pullup and pulldown
(also Toplevel model)

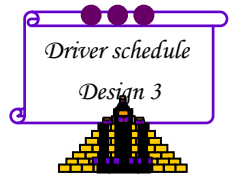


- Boost Model
with pullup and pulldown

but with „inverse currents“

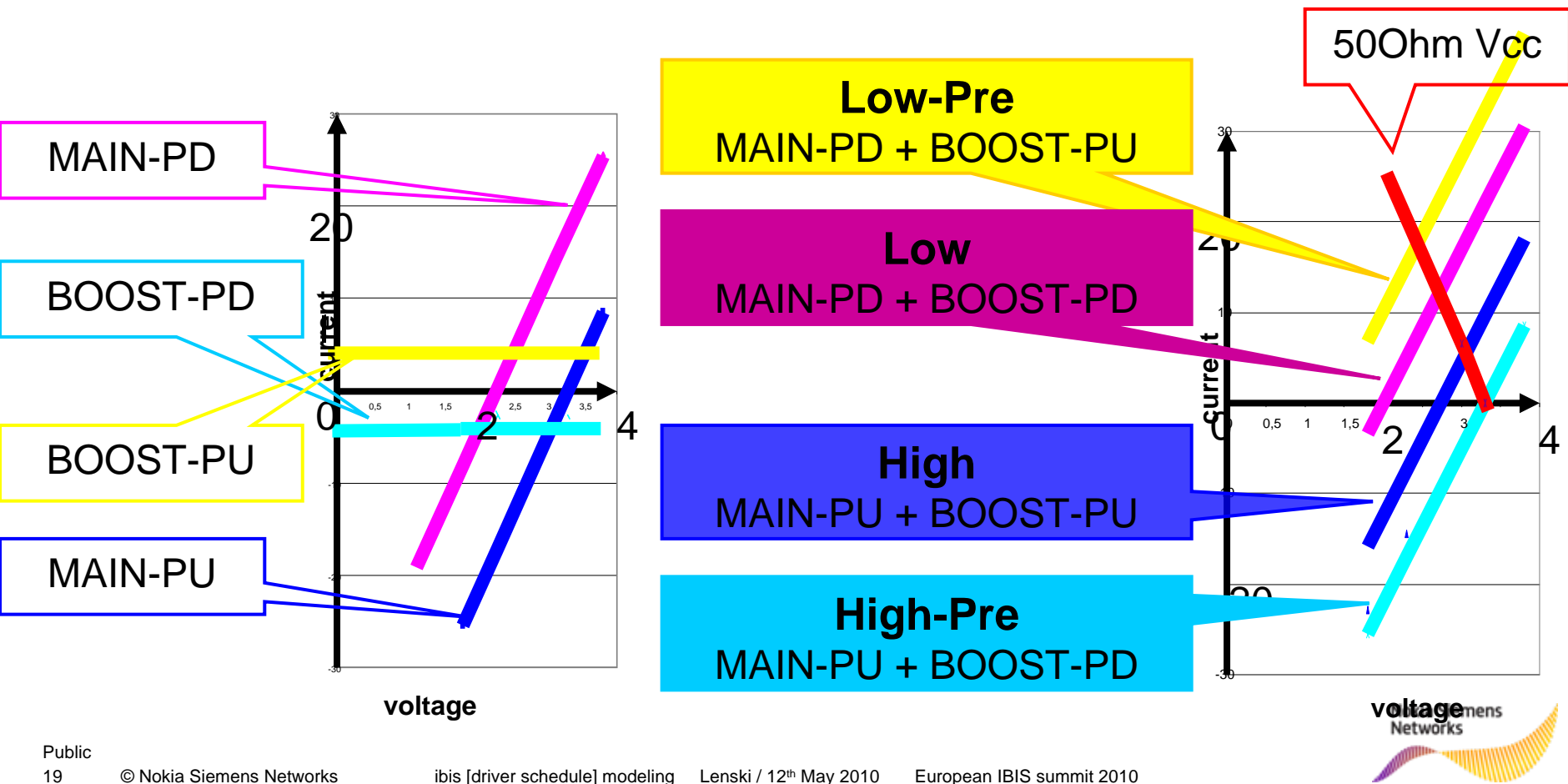


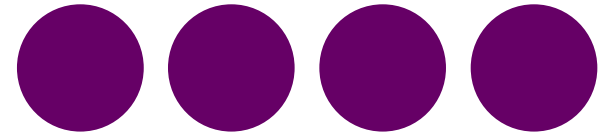
Example 3 combined static curves



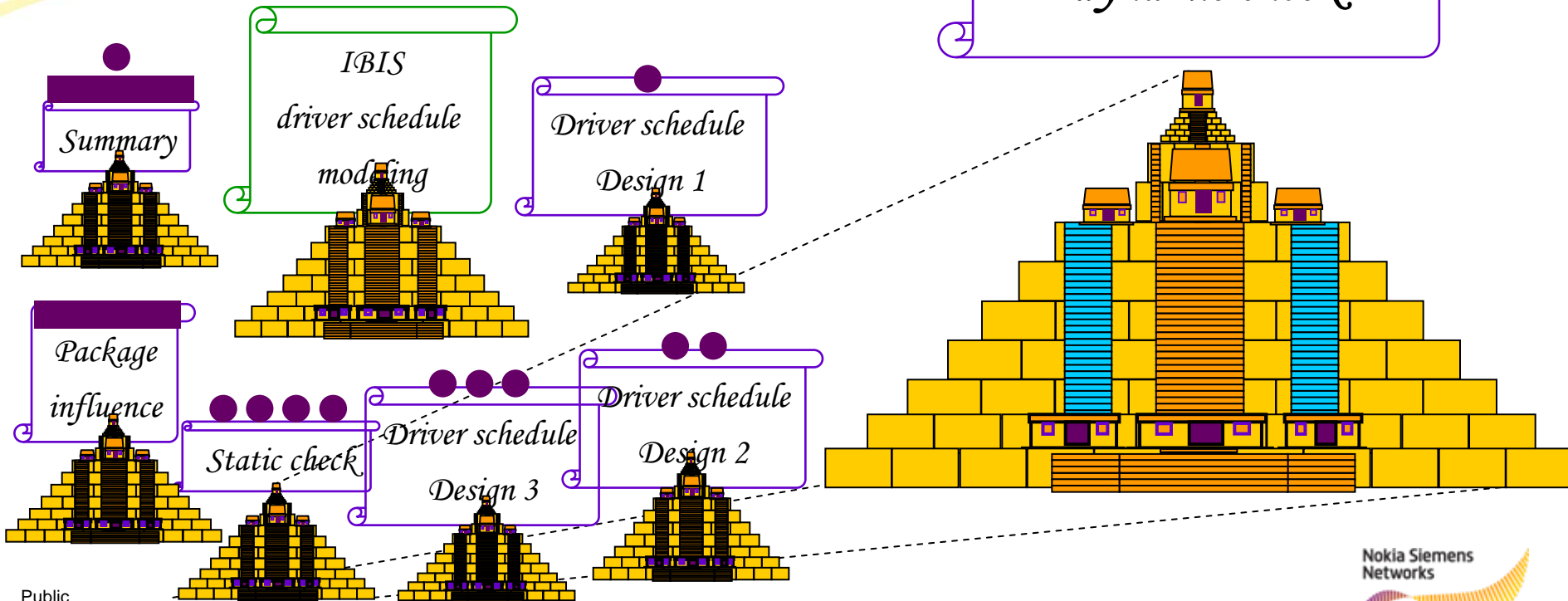
- static curves in one diagram

- combined curves :
- HIGH-Pre / HIGH / LOW / LOW-Pre

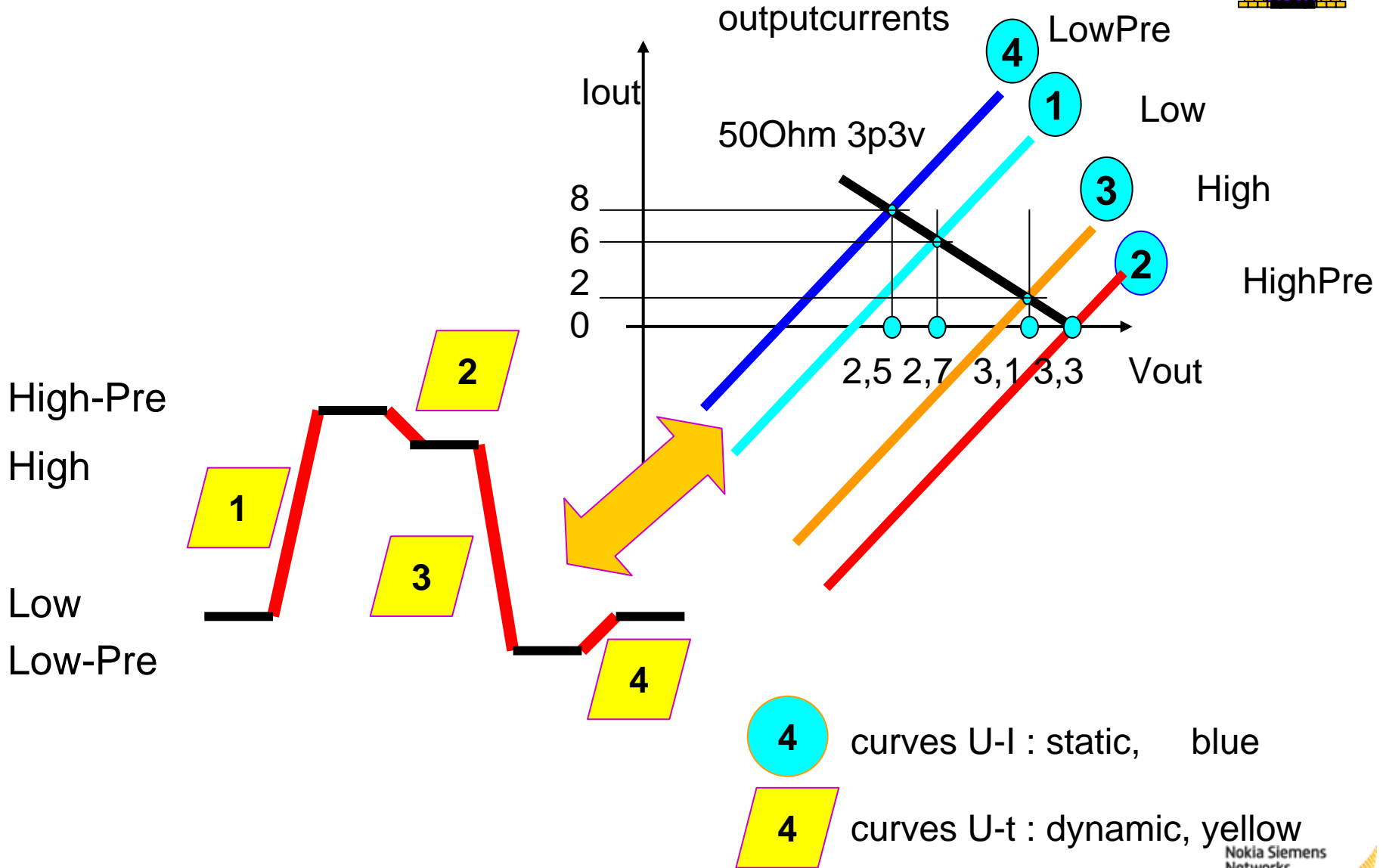
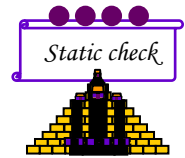




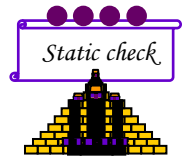
Static check & dynamic check



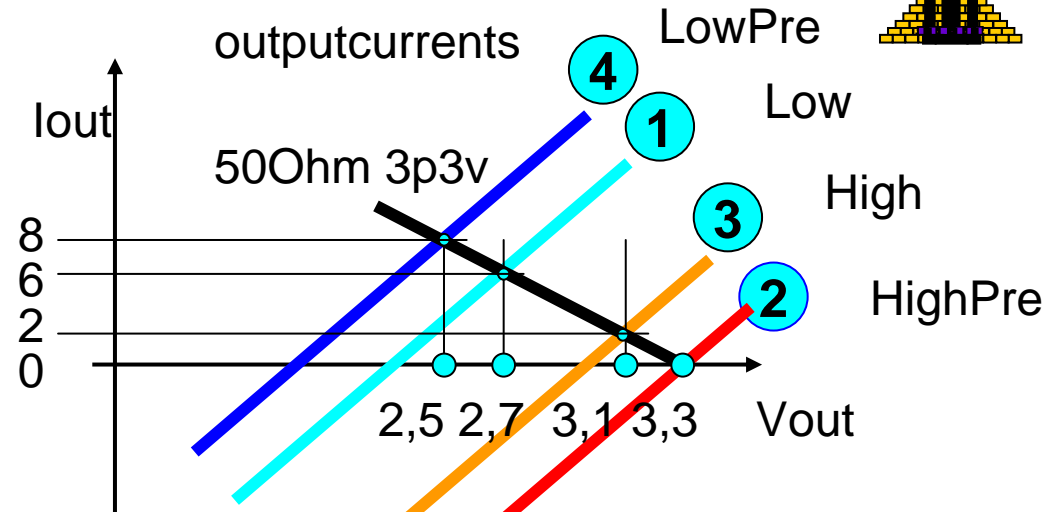
compare dyn. levels – stat. levels



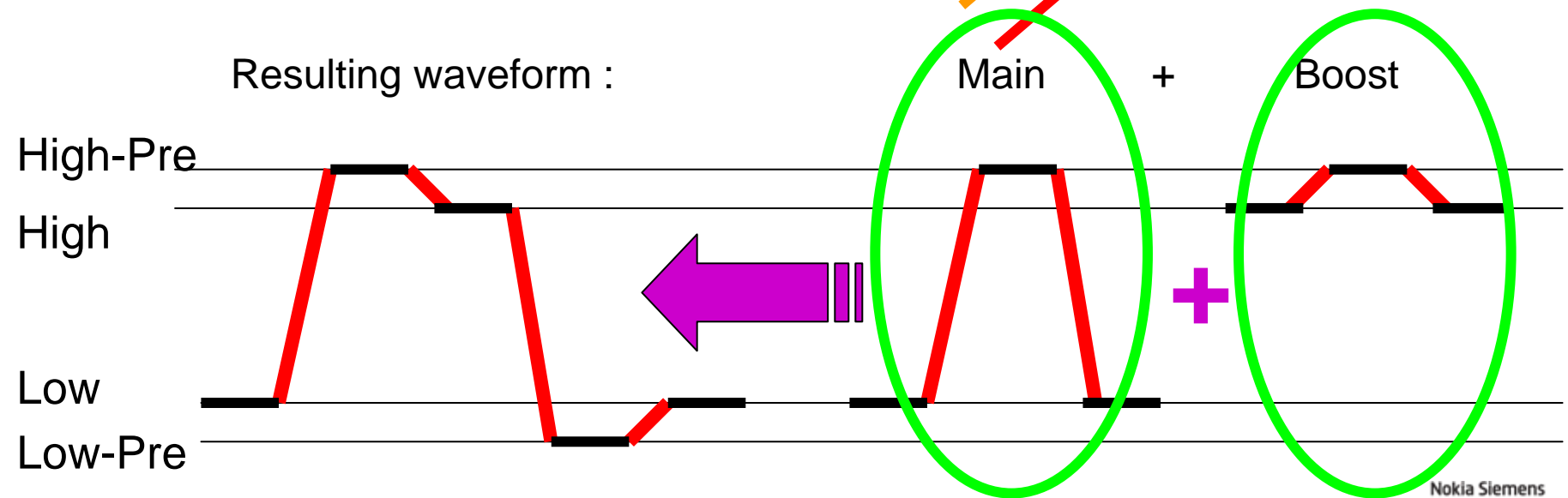
stat. Levels of scheduled models



Each scheduled model will/can be checked as a single model with ibischk5



Resulting waveform :



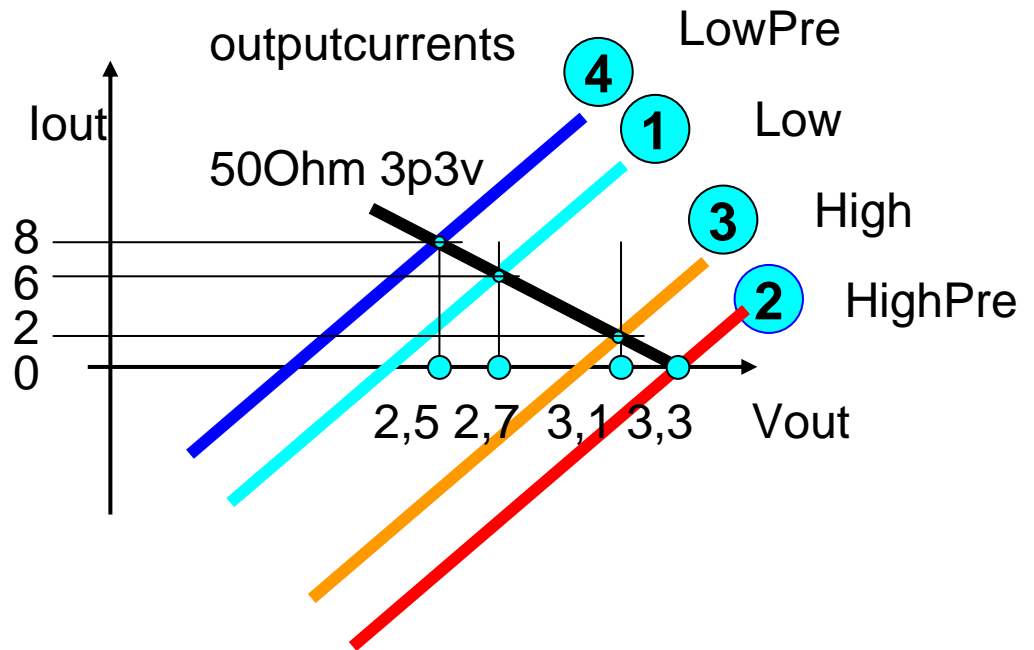
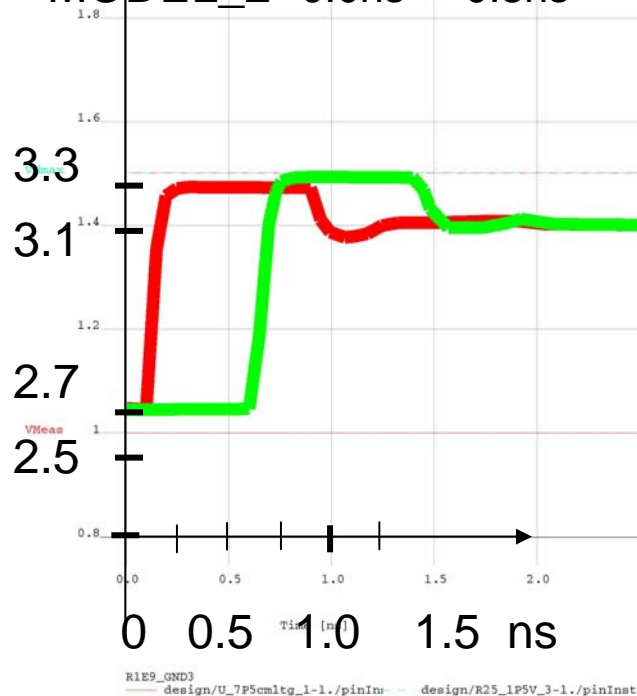
compare golden waveform vs. stat. levels



|Model_name Rise_on_dly Rise_off_dly

MODEL_1 0.0ns NA

MODEL_2 0.0ns 0.8ns





Checks for driver schedule models

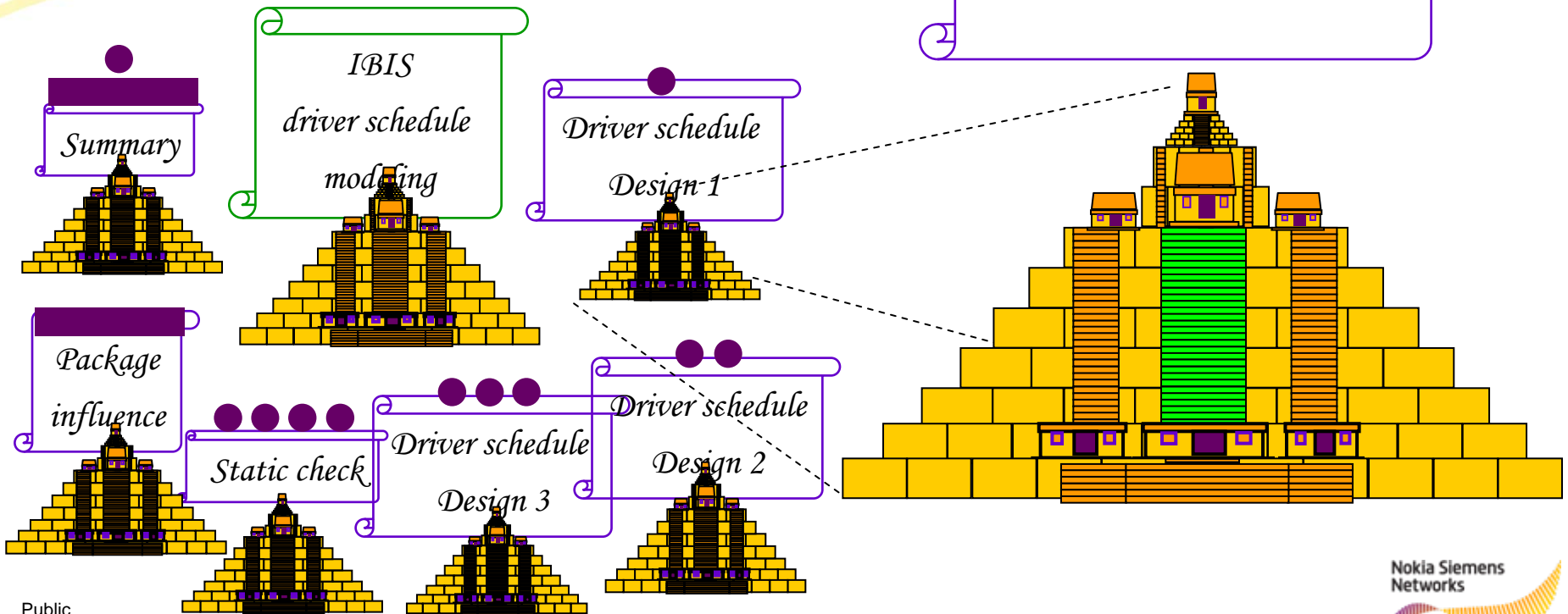
➤ Scheduled models :

- Check each model by itself for static vs. dynamic consistency (works with ibischk5)

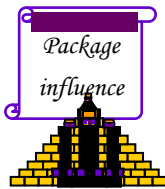
➤ Driver schedule :

- Create combined static curves corresponding timing schedule switching behavior
- Crossover with loadline should give corresponding voltage levels
- Compare with golden waveforms or by using the model in a simulator
- User has to take care that the „frequency“ corresponds to UI

Package influence



simulation max pkg at pin vs measurement



OSCILLOSCOPE

Design file : TEST 18-V5.FFS Designer : Lenski Eckhard

HyperLynx V 8.0

Comment : 5

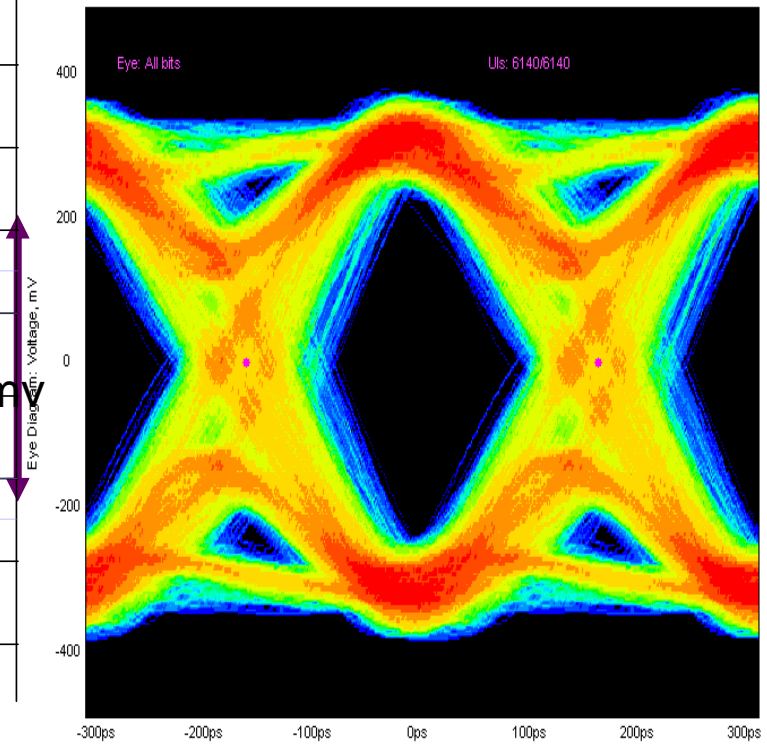
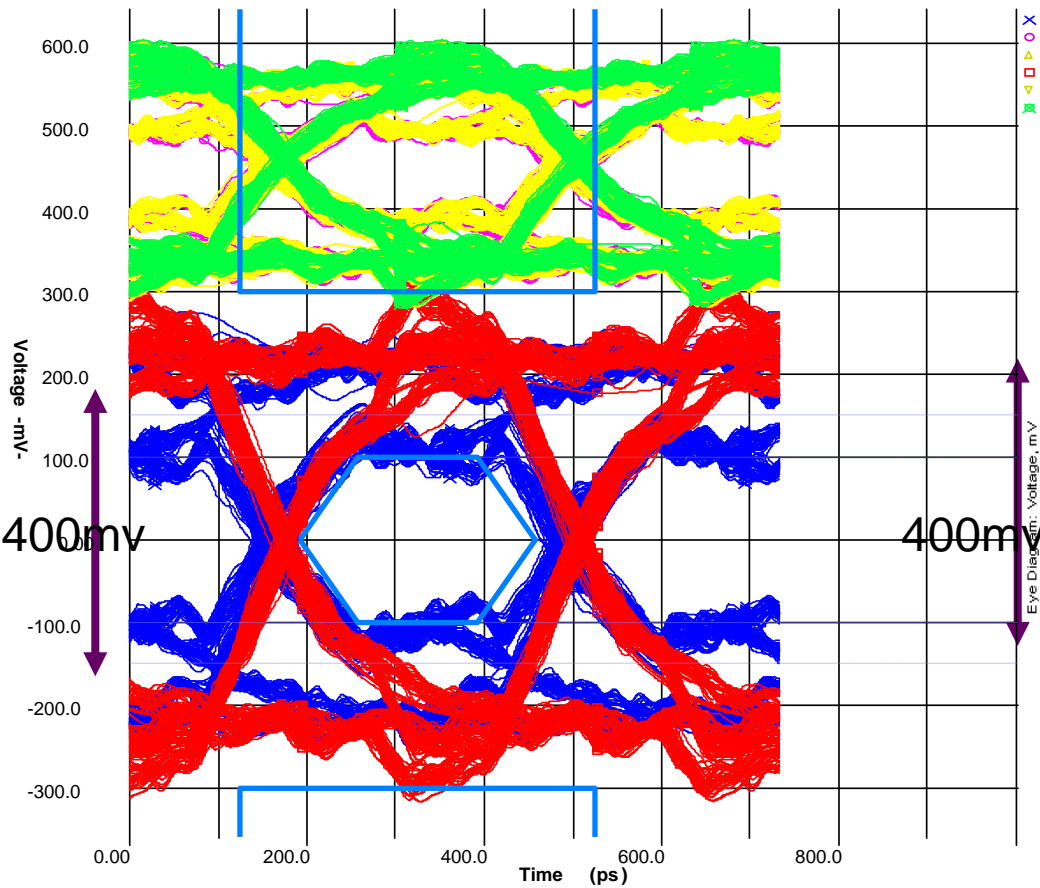
— Diff driver

— Diff receiver

×	V	U4 . H2	{ at pin }	/
○	V	U4 . H2	{ at pin }	/
△	V	U4 . H1	{ at pin }	/
▽	V	U3 . L4	{ at pin }	/
×	V	U3 . L4	{ at pin }	/
×	V	U3 . L3	{ at pin }	/

U4 . H1 (at pin)

U3 . L3 (at pin)

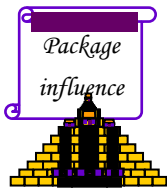


200ps

Date : Friday Jan . 22 , 2010 Time : 15:41:40

200ps

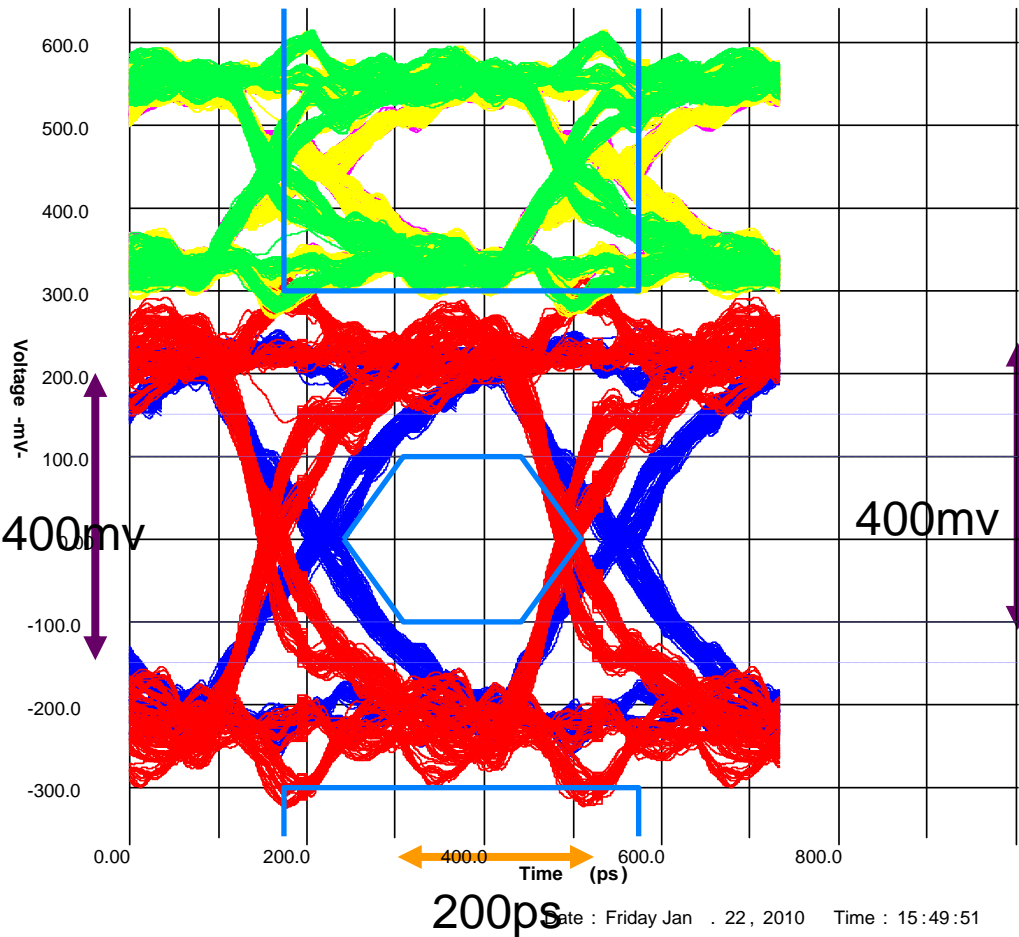
Simulation min pkg at pin vs measurement



— Diff driver
— Diff receiver

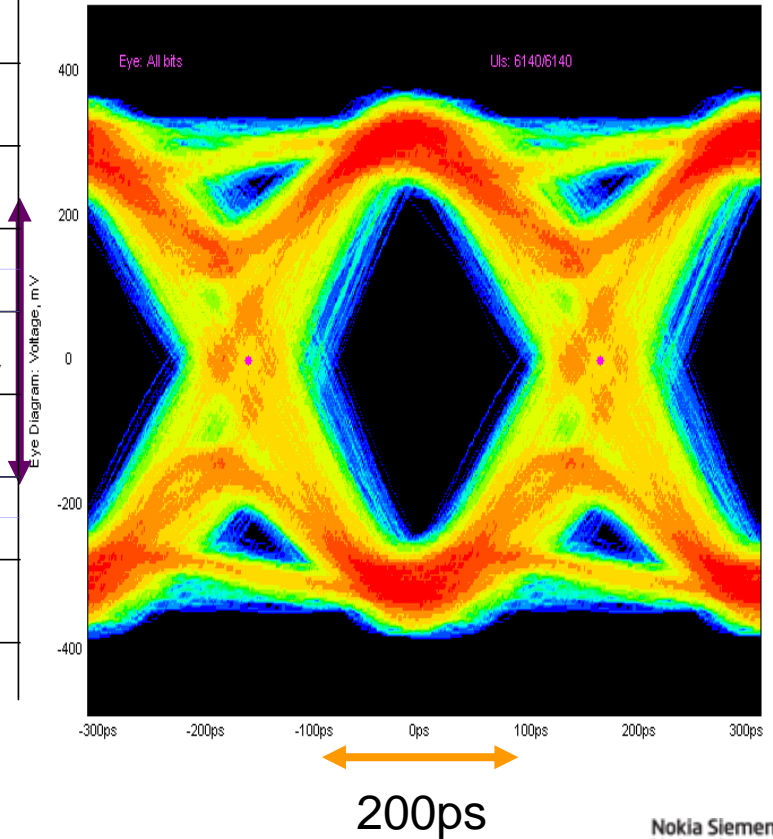
OSCILLOSCOPE

Design file : TEST 18-V5.FFS Designer : Lenski Eckhard
 Hyperlynx V 8.0
 Comment : 5

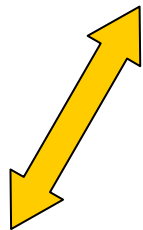
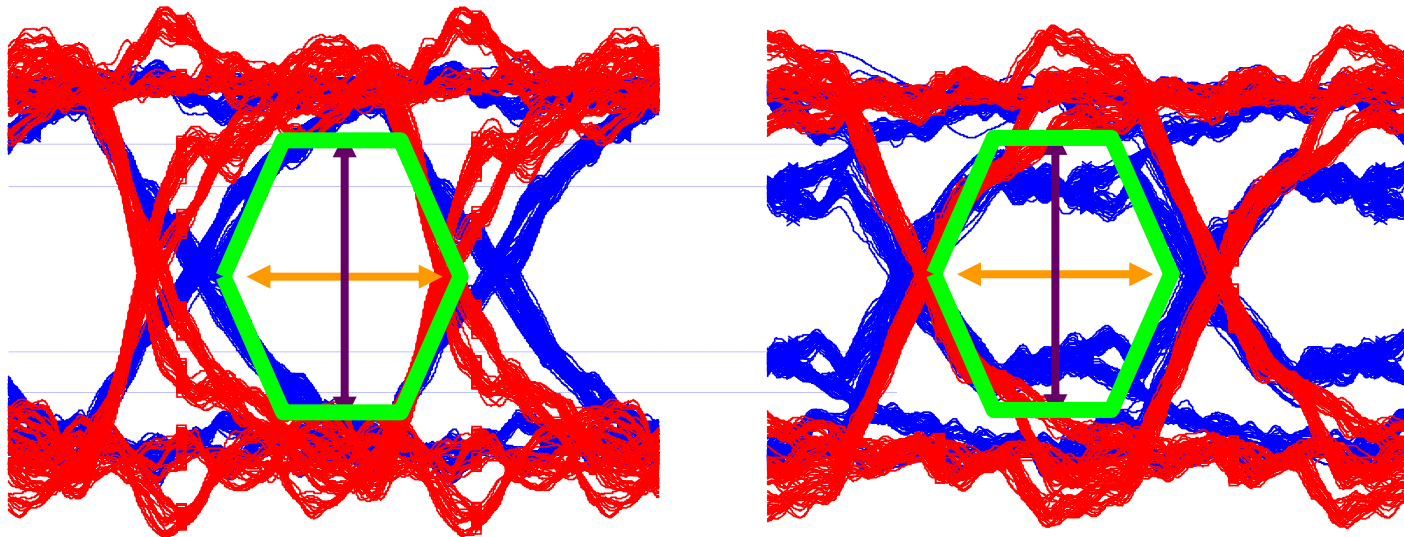


×	V	{	U4 . H2	{	(at pin)/
○	V	{	U4 . H2	{	(at pin	}}
△	V	{	U4 . H1	{	(at pin	}}
□	V	{	U3 . L4	{	(at pin)/
▽	V	{	U3 . L4	{	(at pin	}}
×	V	{	U3 . L3	{	(at pin	}}

U4 . H1 (at pin)]
 U3 . L3 (at pin)]

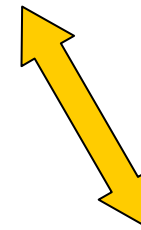
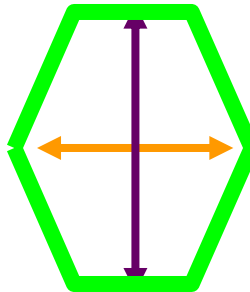


Comparison with min and max pkg at pin



400mv

200ps



Min pkg
Cpkg 0.8pF
Lpkg 2.26nH

— Diff driver
— Diff receiver

Max pkg
Cpkg 1.3pF
Lpkg 3.69nH

Summary



- Driver schedule timing can be used to determine the data rate/frequency of the model
- There are many ways to create pre-emphasis behavior
- Static levels can be checked manually
- Golden waveform should exist
- The quality of the package model is extremely important
- How to use an s-param-file to include as package model ?



Thank You

• **Questions ?**

