IBIS model verification

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Background

- Sintecs is a European electronics design engineering & services company
- Sintecs
  - Offices: Hengelo, The Netherlands, and Minsk, Belarus
  - High speed board design and analysis
- IBIS modeling experiences
  - Creation and verification of ibis models
  - Free IBIS model viewing and editing utility, "IBIS Development Studio“

IBIS model verification

- Step 1. IBIS golden parser
- Step 2. Graphical inspection
- Step 3. IBIS quality checks
- Step 4. Simulation with standard test load
- Step 5. Compare with measurement result

IBIS Quality levels

- **IQ0** - No check performed
- **IQ1** - Passes IBISCHK without Errors or unexplained Warnings
- **IQ2** - IQ1 + data for basic simulation checked
- **IQ3** - IQ2 + data for timing analysis checked
- **IQ4** - IQ3 + data for power analysis checked

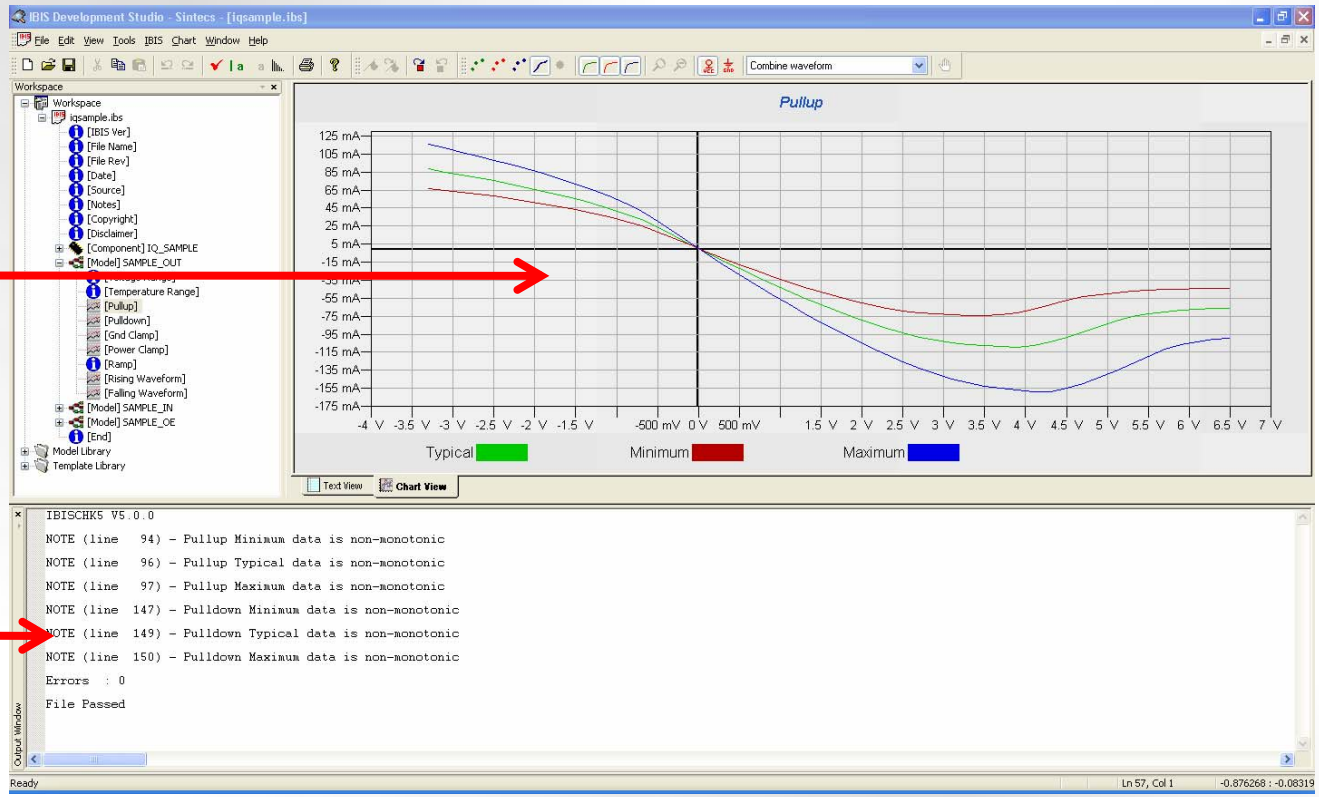
Special designators

- **IQ3M** - IQ3 + correlated against hardware measurements
- **IQ3MS** - IQ3 + correlated against measurements and simulation
- **IQ3GS** - IQ3 + golden waveforms + correlated against simulation
- **IQ4X** - IQ4, but exception(s) to check(s) commented in file

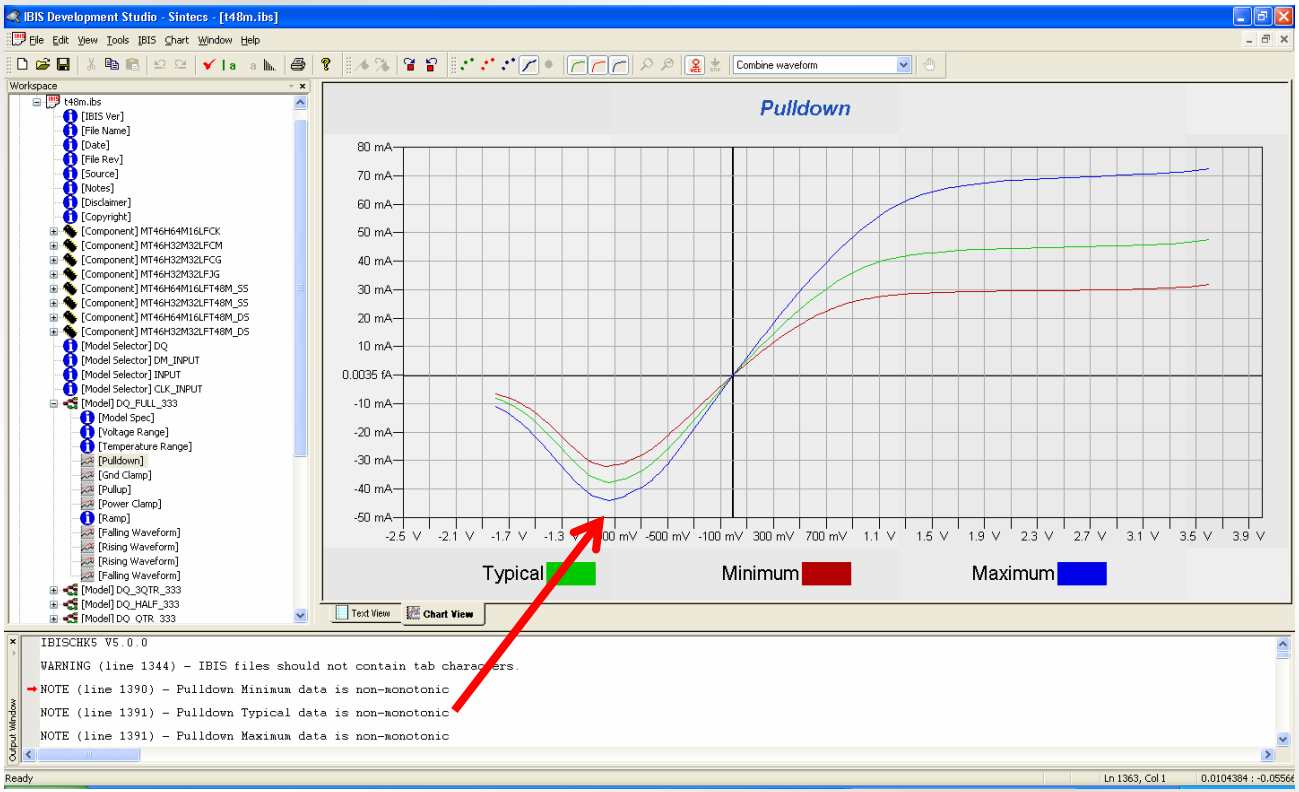
Golden Parser and graphical inspection

Graphical Inspection with an IBIS model viewer

IBIS Golden parser check



Non-monotonic waveform

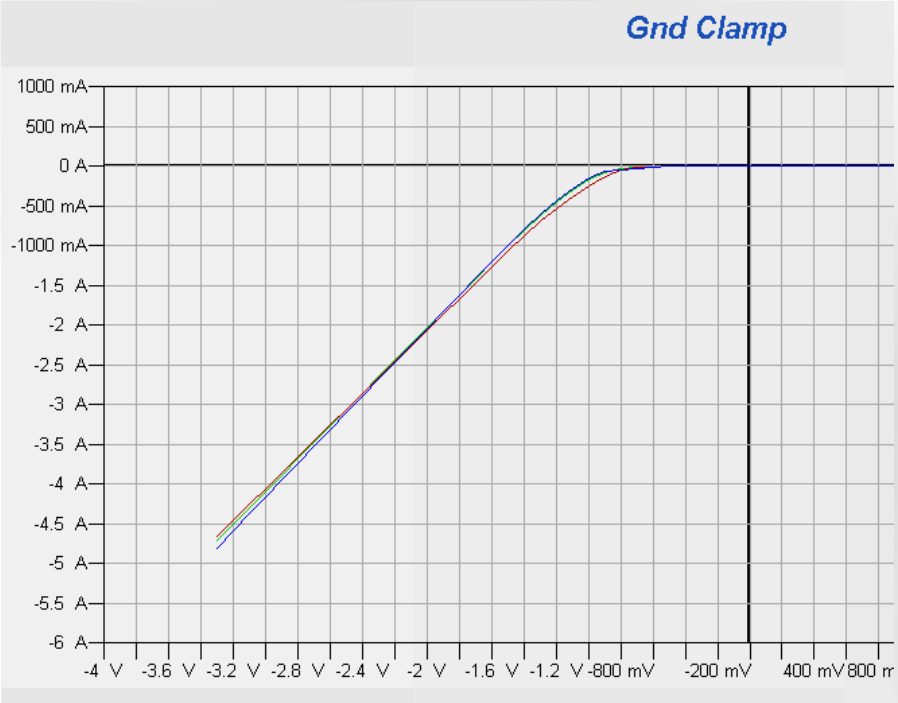


Pull-down data is non-monotonic, do I need to fix this and how???

Combine waveforms

When the pull-down and ground clamp IV curves are combined, the non-monotonic behavior is not present. Still fix pull-down ???

ESD clamping diodes



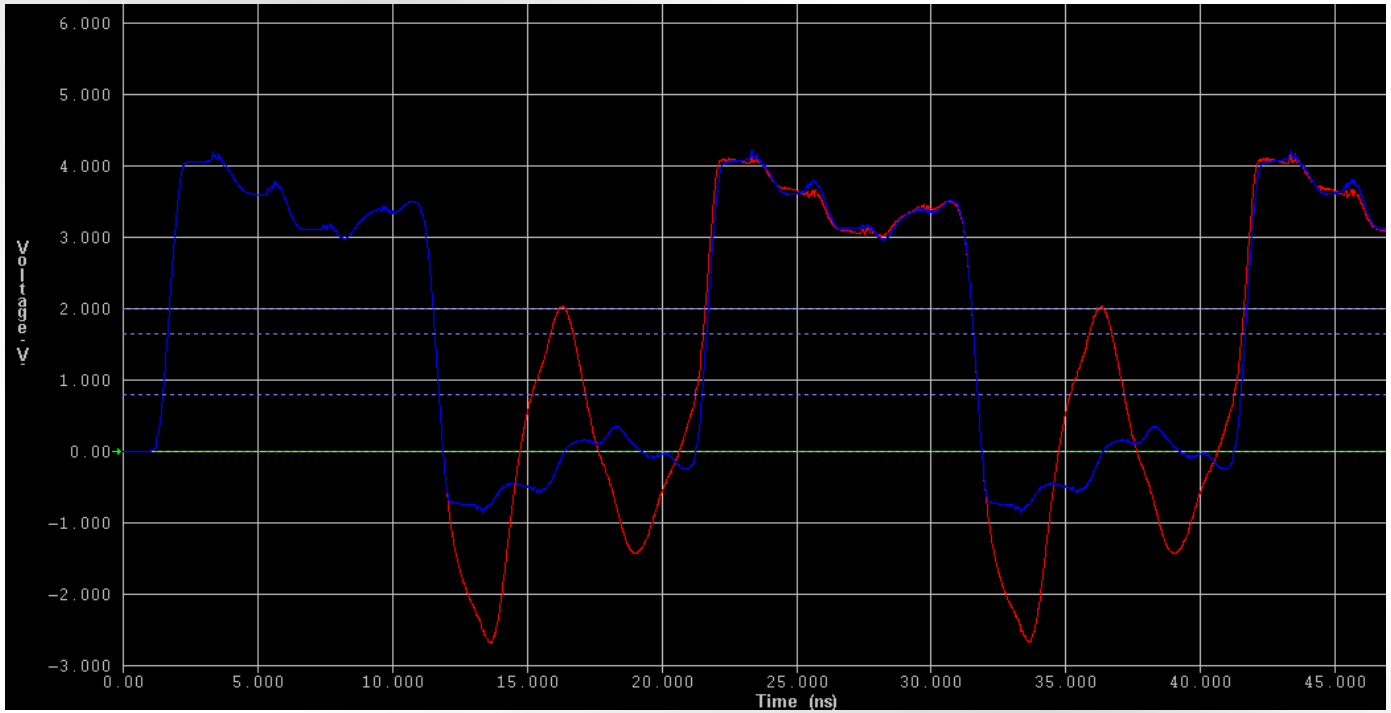
Example:

Standard CMOS device without signal clamping diodes.

The ground clamp of this CMOS buffer, clamps multiple Amps (ESD diode present).

Can you use this diode for signal clamping?

Effect of ESD clamping diodes in IBIS

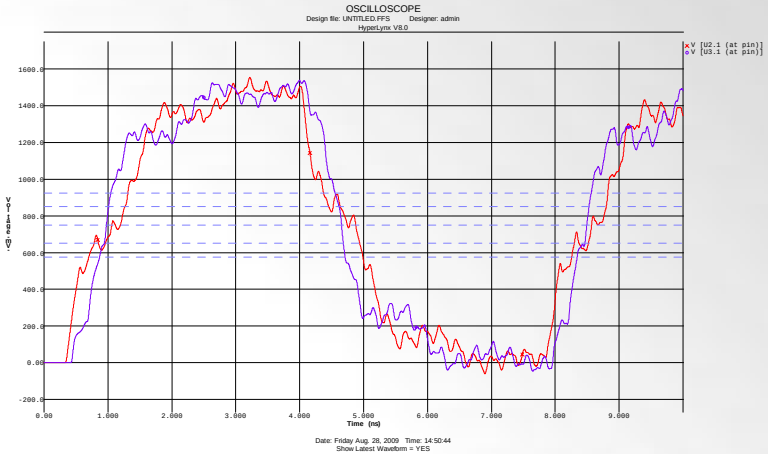


Blue waveform is with the ground-clamp and the red waveform, when the ground clamp is disabled.

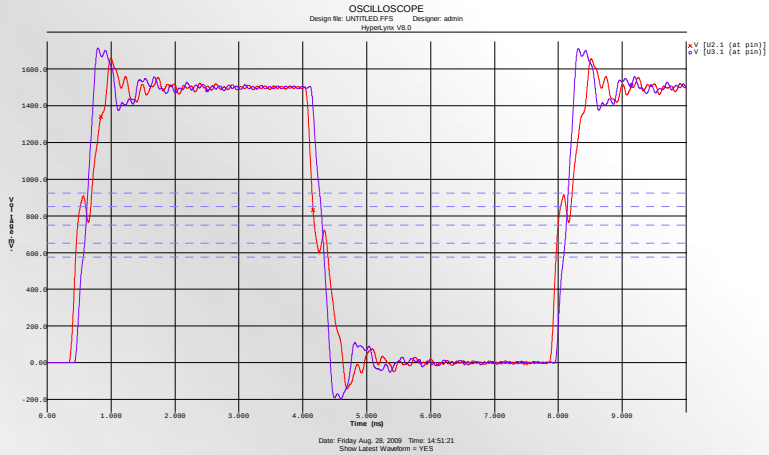
C_comp example

- C_comp value is 10x larger than in datasheet
  - IBIS golden parser doesn't complain.

C_comp = 10 pF



C_comp = 1 pF



IBIS Quality check

- Different level and type of checks
  - Components checks
  - Model checks

IQ Spec Reference	IQ LEVEL	Description	PASS/FAIL	Comments
3.1.1	LEVEL 2	[Package] must have typ/min/max values	---	
3.1.2	LEVEL 2	[Package] parasitics must be reasonable	---	
3.2.1	LEVEL 2	[Pin] section complete	---	
3.2.2	LEVEL 3	[Pin] RLC parasitics are present and reasonable	---	
3.3.1	LEVEL 2	[Diff Pin] referenced pin models matched	---	
3.3.2	LEVEL 3	[Diff Pin] Vdiff and Tdelay_* complete and reasonable	---	
4.1	LEVEL 2	[Model Selector] entries have reasonable descriptions	---	
4.2	LEVEL 2	Default [Model Selector] entries are consistent	---	

IQ Spec Reference	IQ LEVEL	Description	PASS/FAIL	Comments
5.1.1	LEVEL 2	[Model] parameters have correct typ/min/max order	---	
5.1.2	LEVEL 2	[Model] C_comp is reasonable	---	
5.1.3	LEVEL 2	[Temperature Range] is reasonable	---	
5.1.4	LEVEL 2	[Voltage Range] or [* Reference] is reasonable	---	
5.2.1	LEVEL 3	[Model] Vinl and Vinh reasonable	---	
5.2.2	LEVEL 3	[Model Spec] Vinl and Vinh reasonable	---	
5.2.3	LEVEL 3	[Model Spec] Vinl+/- and Vinh+/- complete and reasonable	---	
5.2.5	LEVEL 2	[Model Spec] S_Overshoot subparameters complete and match data sheet	---	

Model verification time

- Time spend for full verification (Level3) depends on the number of models available in the ibis model.

- Example Altera Stratix IV has more than 300 different buffer models. Verifying this ibis model with the IBIS Quality template will cost several weeks/months.

What will happen when you get a new version of the Stratix IV model ??

Other model types

- IBIS AMI
- Touchstone model
- IBIS ICM
- Package model
- EBD model

IBIS-AMI

What is IBIS-AMI

- The **IBIS Algorithmic Modeling Interface (IBIS-AMI)** is a modeling standard for SerDes transceivers that enables fast, accurate, statistically significant simulation of multi-gigabit serial links. IBIS-AMI was developed by a consortium of EDA, Semiconductor and Systems companies and was approved as part of the IBIS 5.0 specification in August 2008.

- IBIS-AMI models have two parts
  - Analog model
  - Algorithmic model

IBIS-AMI model verification

- Algorithmic model
- Supplied as binary code (.DLL) that gets linked into the Channel Simulator at runtime
- No verification can be done, comparison with measurement is needed.

Touchstone model

- A Touchstone file (also known as an SnP file) is an ASCII text file used for documenting the n-port network parameter data of an active device or passive interconnect network.

- Touchstone® File Format Specification Version 2.0 (April 2009)
- A Touchstone parser, tschk2, is available

```
tschk2, version 2.0.0
verification tool for Touchstone v2 files

Usage modes:

  tschk2 FILE                   Checks the file, sending error and warning
                                information to stderr.

  tschk2 -canonical    FILE     Shortcut for -canonical-v2.

  tschk2 -canonical-v2 FILE     Checks the file, sending error and warning
                                information to stderr, and writes a valid file
                                to stdout in Touchstone v2 format.

  tschk2 -canonical-v1 FILE     Checks the file, sending error and warning
                                information to stderr, and writes a valid file
                                to stdout in Touchstone v1 format, if possible.

  tschk2 -describe FILE         Checks the file, sending error and warning
                                information to stderr, and writes a valid file
                                to stdout in a long-form description.

  tschk2 -version               Displays the version number.

  tschk2 -help                  Displays this help message.
```

IBIS ICM

- The **IBIS Interconnect Modeling Specification** (ICM) is a behavioral, ASCII-based file format for distributing passive interconnect modeling information.
- An ICM parser, icmchk1vailable.

```
IBIS ICM Version 1.1.3 parser.

USAGE: icmchk1 [-vschp] [-f[<ver>]] [<file name>]
       -v --> (verbose, once)  Report additional informational messages.
       -v --> (verbose, twice) Report debug messages (caution: voluminous).
       -s --> (sort)           Sort diagnostic messages by line number.
       -c --> (copyright)      Display program copyright and exit.
       -h --> (help)           Display this message and exit.
       -p --> (pipe)           Read stdin pipeline instead of file.
       -f --> (force version)  If -f<ver>, parse as version '<ver>'.
                               If -f, honor the file's [ICM Ver] keyword.
                               If omitted, always parse as version '1.1'.
       <file name>             The input IBIS ICM Model file.
```

Package model

- Available in ibis model or in separate *.pkg file.
- More detailed package model than standard lumped R_pin, L_pin, C_pin or generic [Package] statement.
- .pkg models are transmission line models
  - RLC matrixes for coupling

EBD model

- EBD – Electrical Board Description
- A pure transmission line description without coupling
- All inductance and capacitance parameters listed in the file are derived with respect to well-defined reference plane (s) within the board
- Via in EBD is described as zero length with lumped RLC value
- EBD is good for transmission line effect investigation and timing analysis for first order consideration.

Conclusion

- Verification of IBIS models is needed for accurate SI analyses
- Different types of models are available
- Detailed verification of IBIS models costs a lot of time
- Automation needed for accurate and fast model verification

Questions ?