Enhanced MπIog Models for Power Integrity Analysis.

Modeling from simulation and measurement, IBIS data extraction, crossvalidation

A. Girardi[1], **I.S. Stievano**[2], R. Izzi[1], T. Lessio[1], F.G. Canavero[2], I. Maio[2], L. Rigazio[2]

[1] Numonyx Italy S.r.l., [2] Politecnico di Torino, Italy

Ref. contacts: {antonio.girardi@numonyx.com, igor.stievano@polito.it}

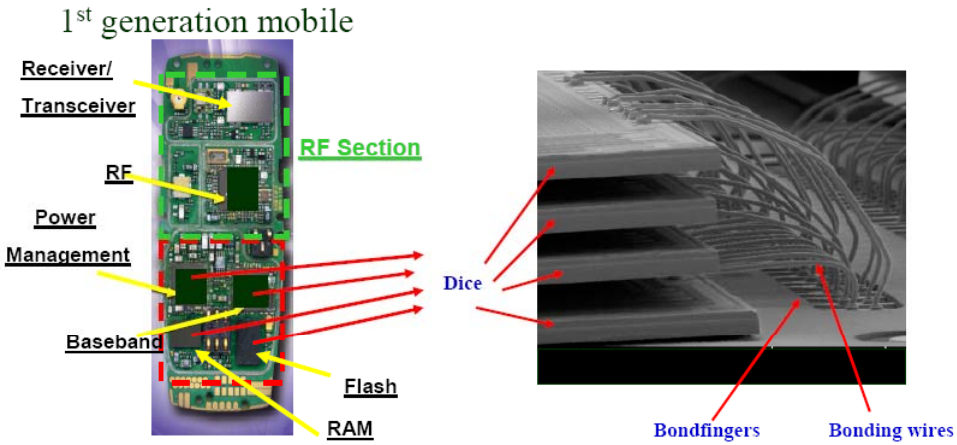
MOCHA, MOdelling and CHAracterization for SiP - Signal and Power Integrity Analysis

(www.mocha.polito.it)

- European Project FP7-ICT-2007-1* (Jan 2008 – Mar 2010)

  "Develop reliable modelling and simulation solutions for SiP design verification"

- Partecipants:
  - **Numonyx Italy Srl (Italy) [Coordinator]**
  - Politecnico di Torino (Italy)
  - Cadence Design Systems Gmbh (Germany)
  - Agilent Technologies (Belgium)
  - Universidade de Aveiro (Portugal),
  - Microwave Characterization Center (France)



- Work Packages
  - WP1, IC power integrity model
  - **WP2, IC buffers' innovative modelling approach**
  - WP3, SiP design and verification EDA platform
  - WP4, SiP signal integrity measurement platform

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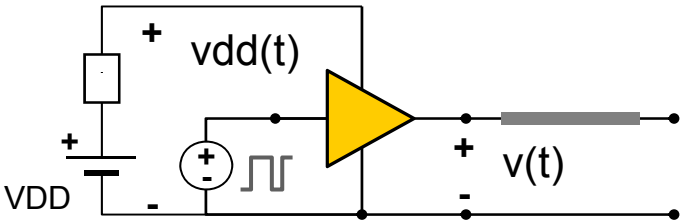
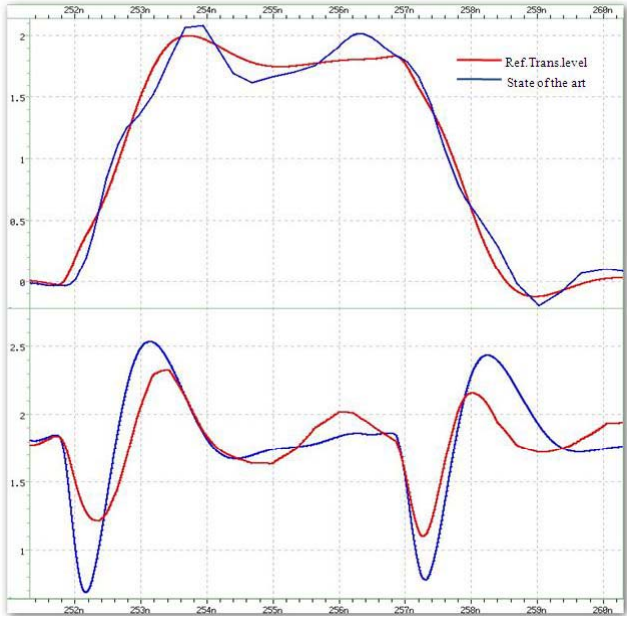
WP2 overview

Objective: Development of accurate and efficient models of digital ICs

- **Overcome current limitations of existing models**

  e.g., state-of-the art models allow only for limited power supply variations





Ref. trans. level State-of-the art

- **Generate models from measurements & simulations**

WP2 achievements (i)

TASK 2.1

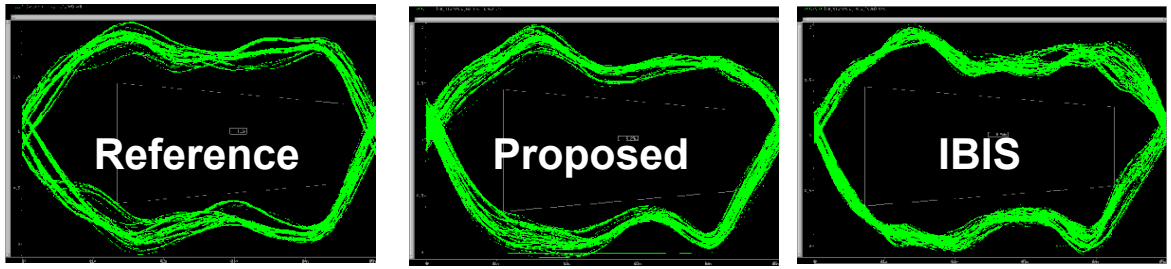
- Availability of the General structure of the extended model for digital buffers
- Procedure for parameter estimation from simulation / measurement

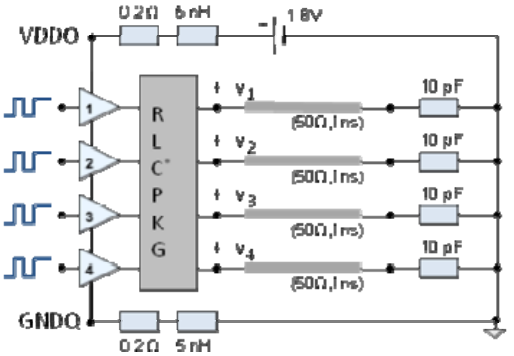
TASK 2.2

- Model implementation in different formats (HSPICE, ELDO, VERILOG-A,…)
- Application to test cases (proprietary and third party devices) from simulation

WP2 achievements (ii)

❑ **Model Accuracy, second test case (estimation from simulation)**





	Eye opening	Error	CPU
Reference (trans. level)	72%	-	773 s
IBIS	78.8 %	9.5 %	13 s (59x)
Proposed (MπLOG)	73.8 %	2.5 %	31 s (25x)

✓ **Improved Accuracy**

✓ **High efficiency**

WP2 achievements (iii)

TASK 2.3

- Design two **test boards** for the characterization of the IC ports of the MOCHA test cases

e.g., first test case, DQ0 I/O buffer

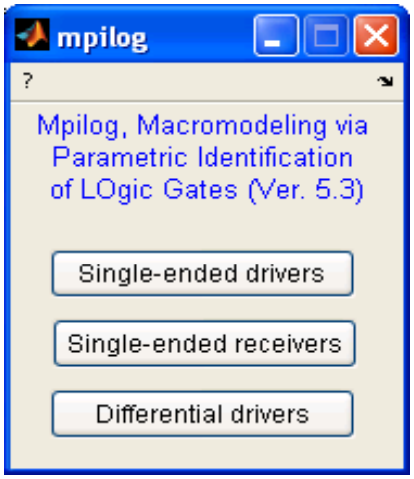
Device models from transient port voltage and current responses recorded during IC normal operation

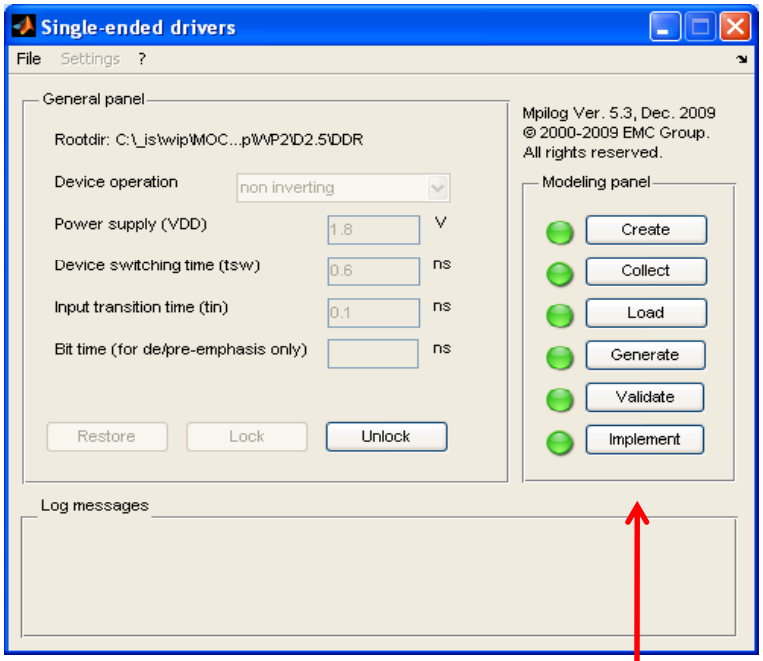
WP2 achievements (iv)

TASK 2.4

- **Tool for the interactive generation of IC models**

  → **Μπlog ver. 5.3**, available @ www.emc.polito.it



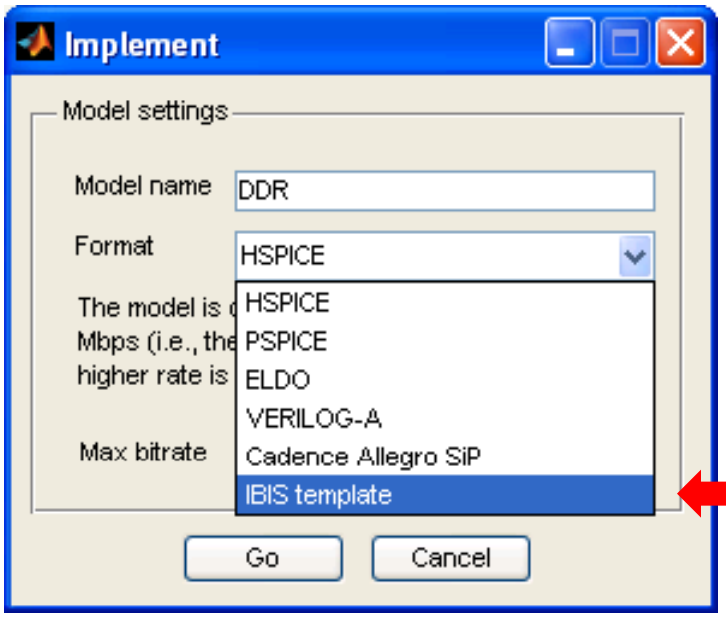


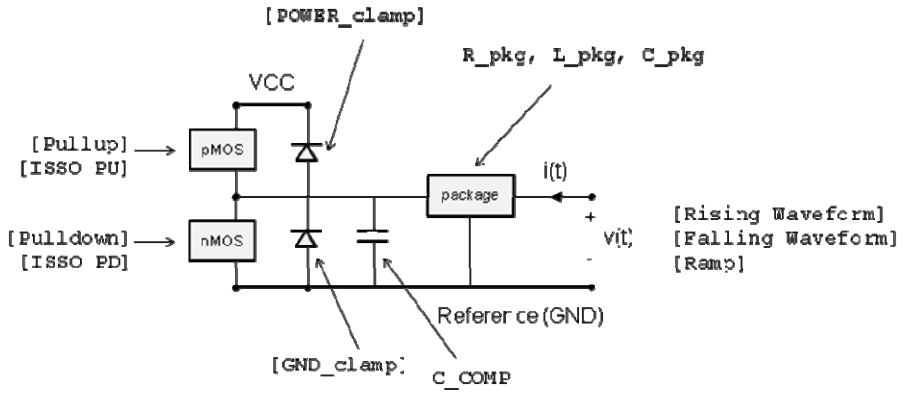
Guided step-by-step modeling procedure

WP2 achievements (v)

TASK 2.5

- procedure for the **extraction** of device characteristics suggested by **IBIS** from the **estimated models**





X-Validation (i)

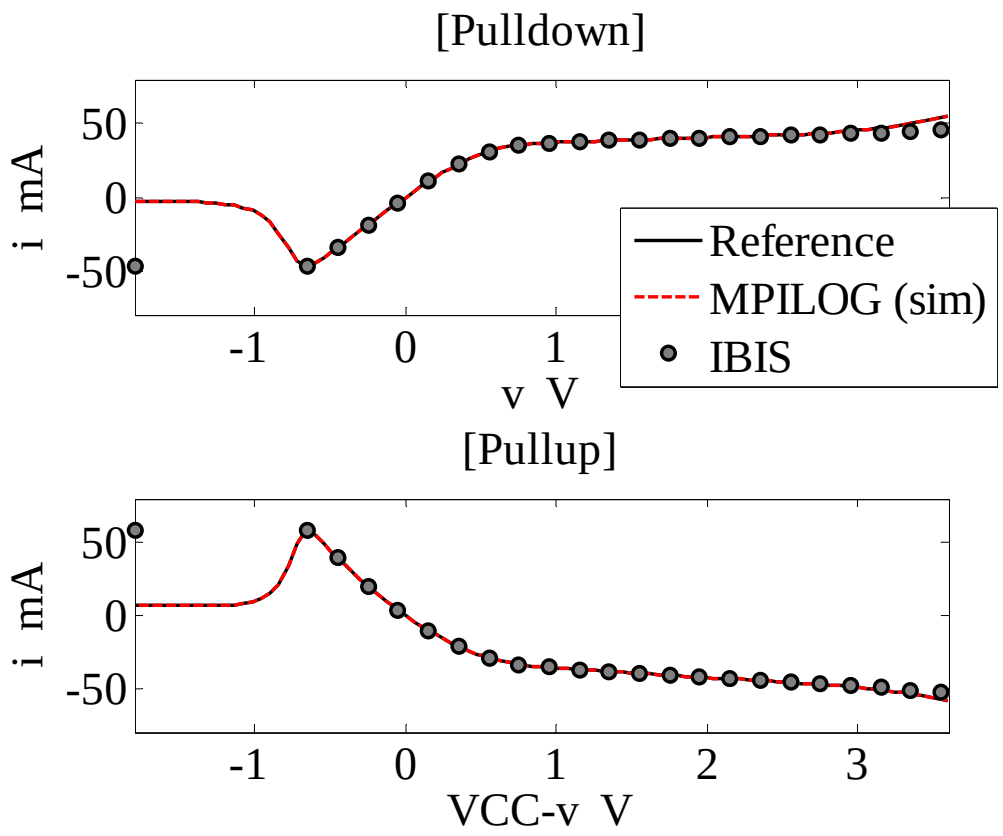
Test case: 512Mb LPDDR third party device, in 70nm technology and clock frequency of 133MHz.

Models:

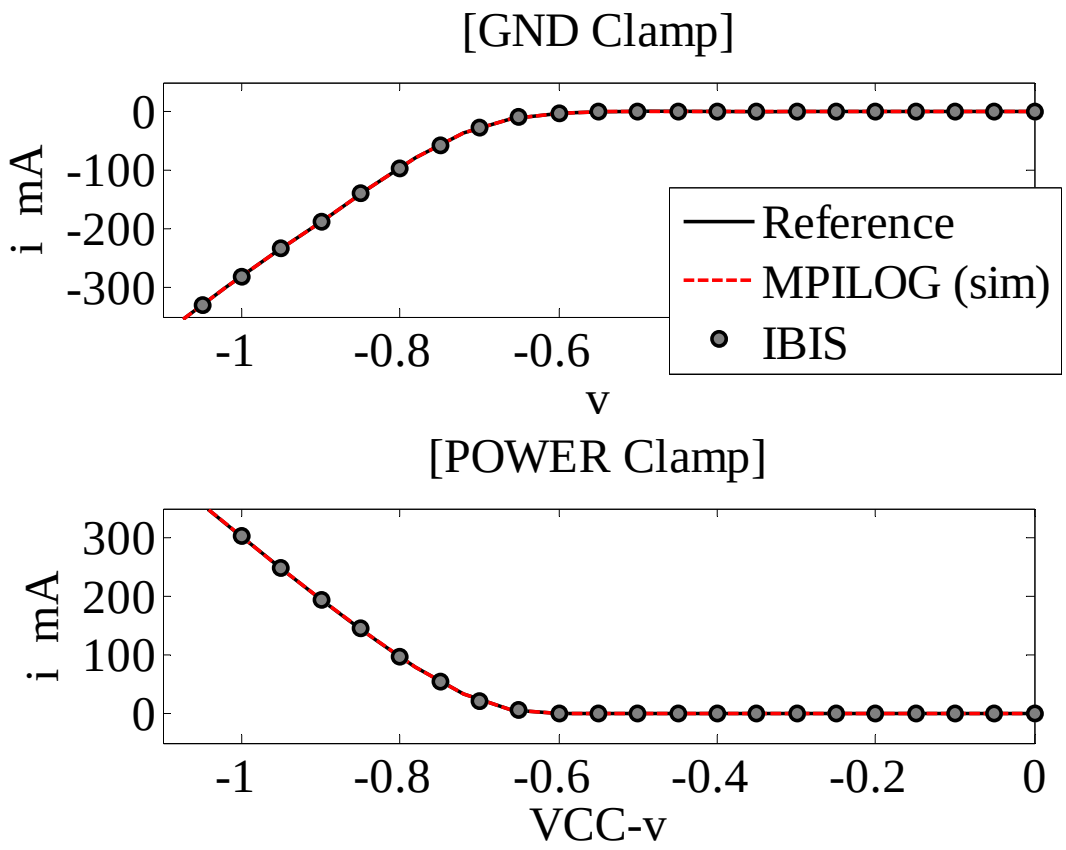
- Reference Transistor-level
- IBIS
- Mπlog (from simulation)
- Mπlog (from measurements)

	IBIS	**MPLOG** (sim)
C_COMP	**3.1pF**	**3.045 pF**

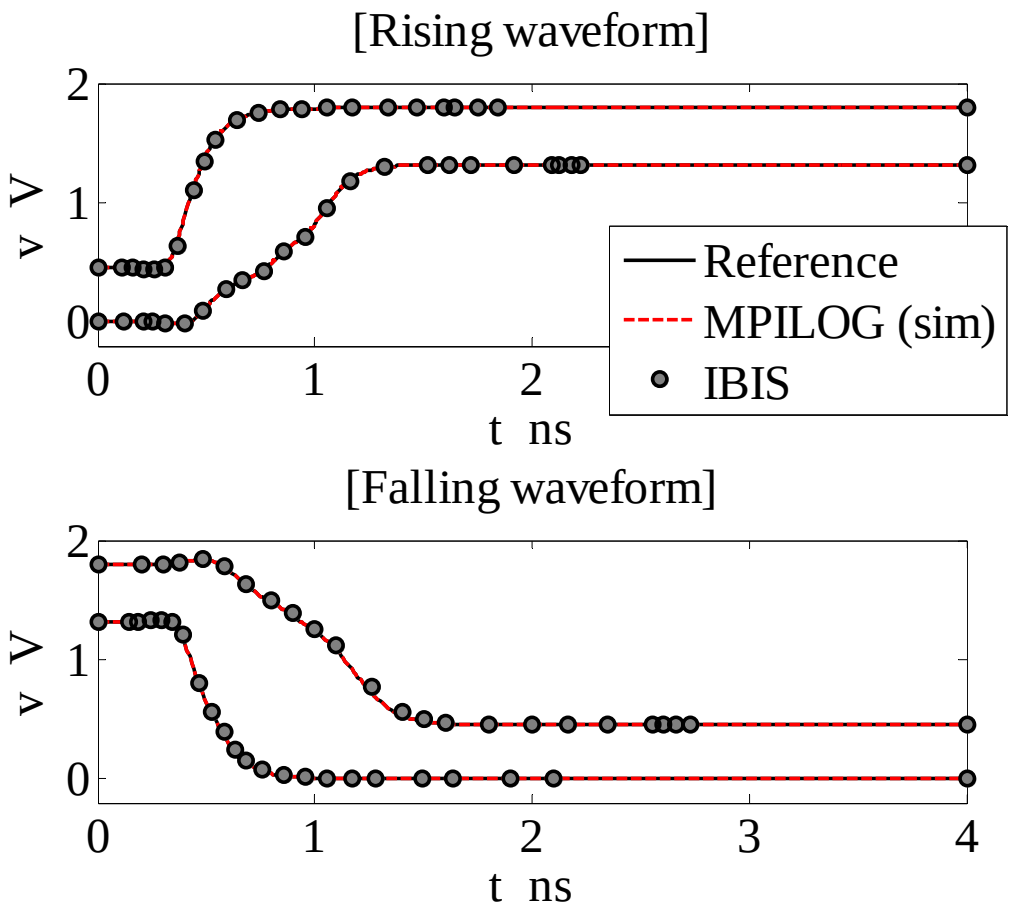
X-validation (ii)



X-validation (iii)

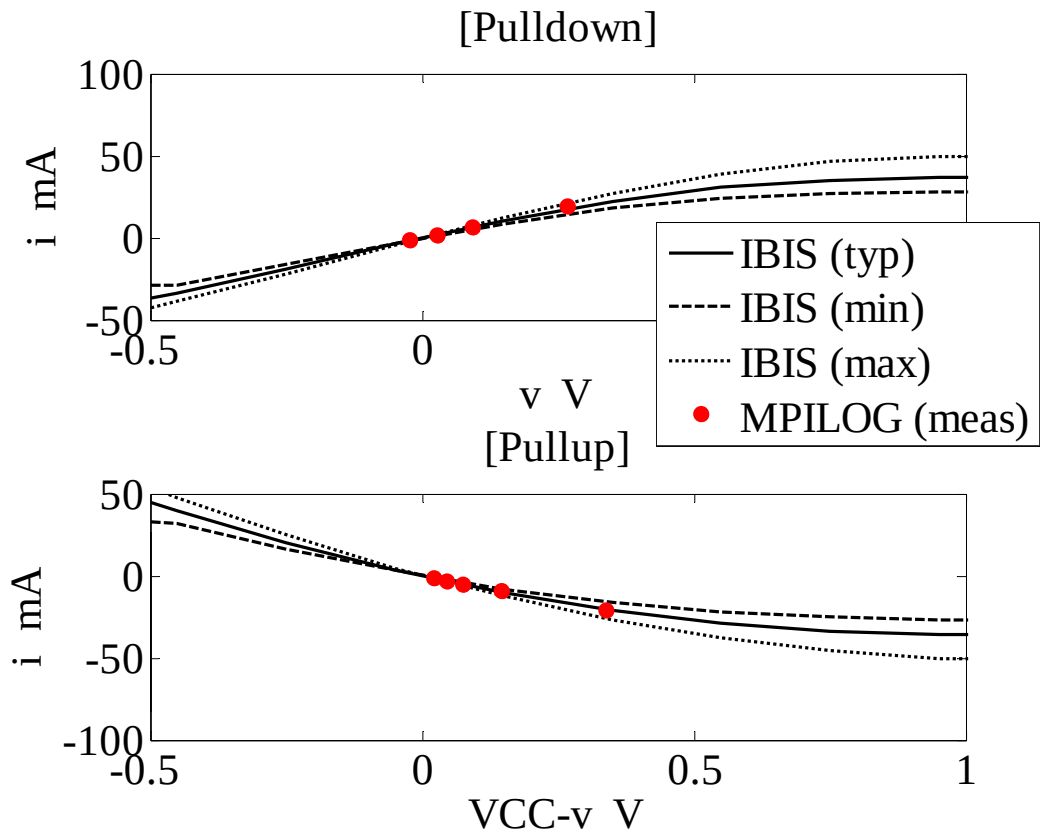


X-validation (iv)



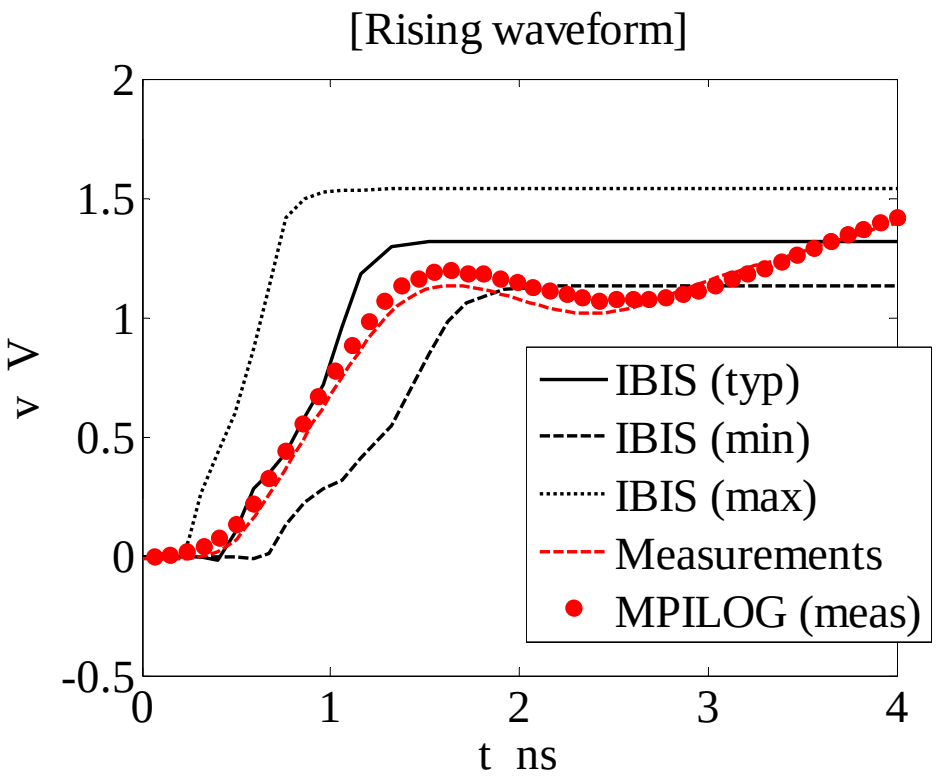
X-validation (v)

…model from real measured data



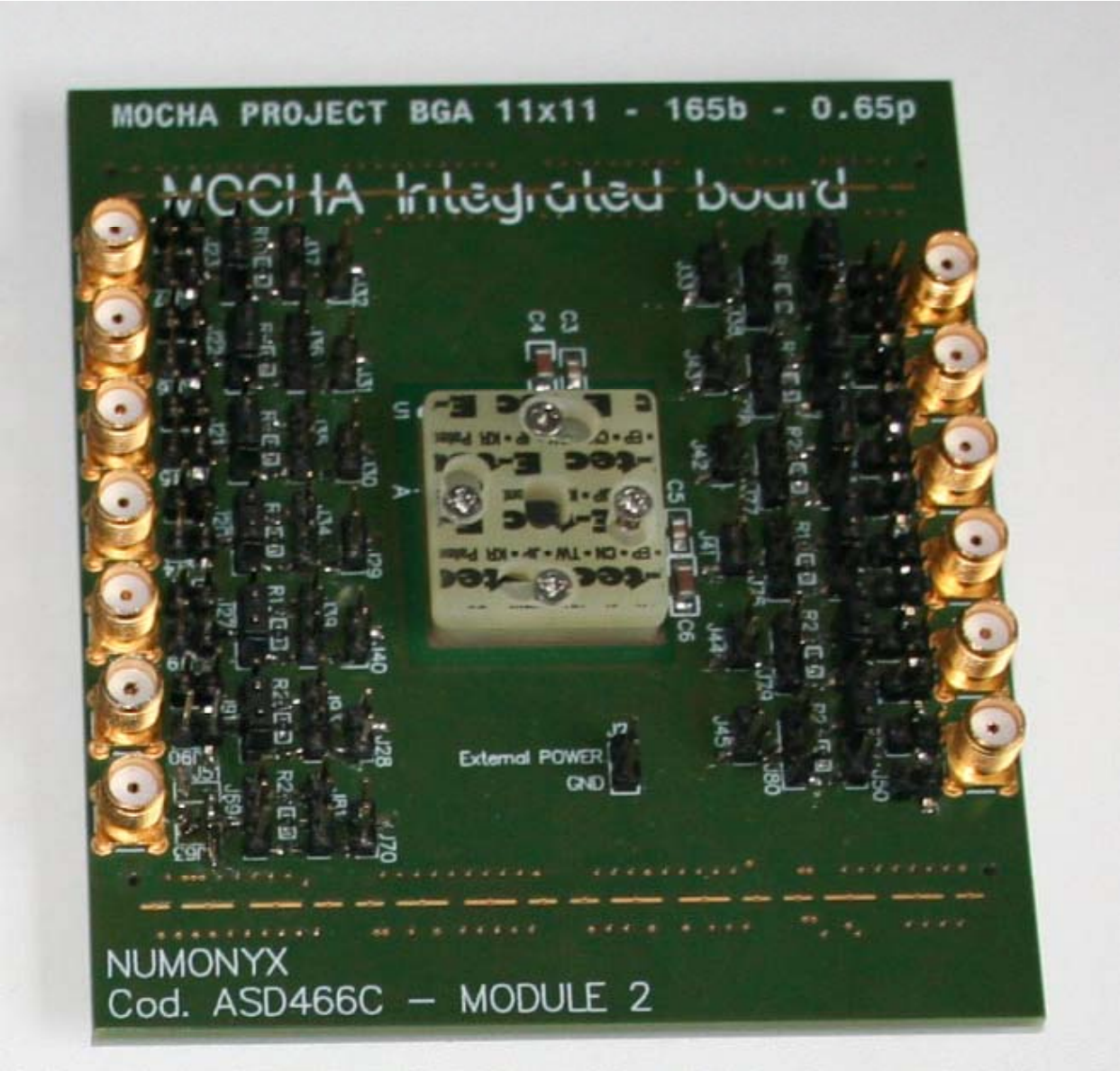
X-validation (vi)

…model from real measured data



R_fixture = 47 Ω
L_fixture = 18 nH
C_fixture = 7.4 pF
V_fixture = 0V

Q&A


MOCHA PROJECT BGA 11x11 - 165b - 0.65p
MOCHA Integrated board
External POWER
GND
NUMONYX
Cod. ASD466C – MODULE 2