Macromodels of IC Buffers Allowing for Large Power Supply Fluctuations

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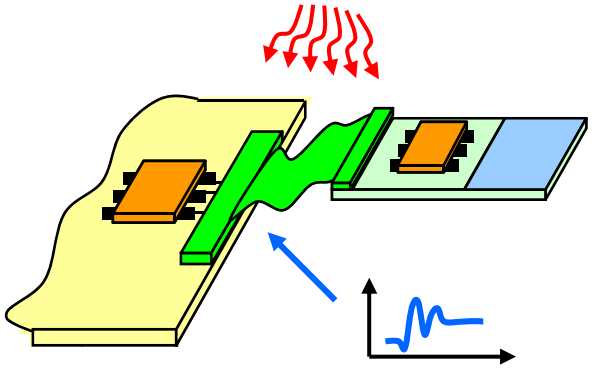
Introduction

Models of IC buffers required for the system-level assessment of **signal integrity** and **EMC** effects via numerical simulation

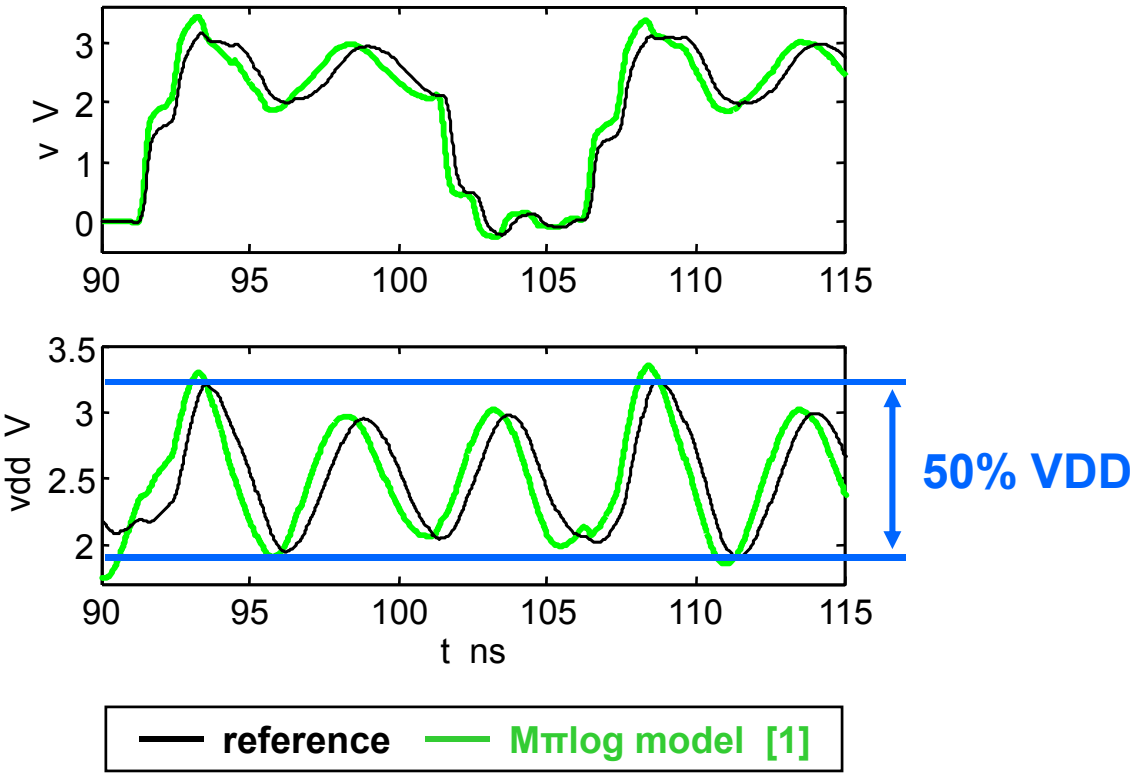


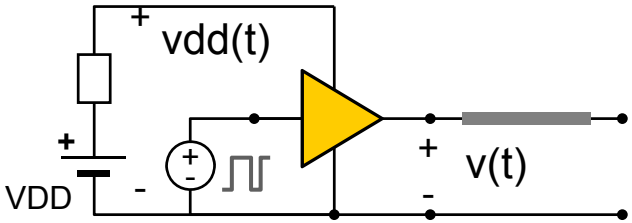
Include the effects of power supply variations

- **Recent applications** (e.g., stacked SiP devices, → memories) exhibit large variation (30÷40%)
- **State-of-the art models allow only for limited variations** (10÷15% of the nominal power supply voltage)

Improve existing models

Example





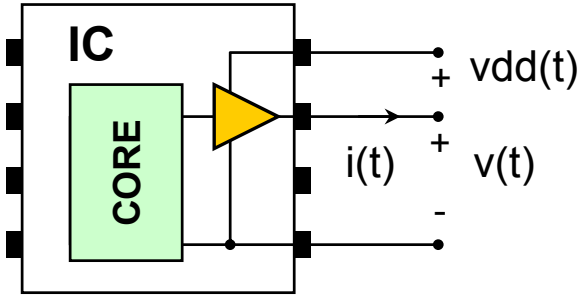
Waveform distortion produced by the state-of-the-art models

Where do these differences come from?

[1] I.S.Stievano et. Al., “M[pi]log, Macromodeling via parametric identification of logic gates”, TADVP 2004.

Mπlog model structure

e.g., IC output buffer (single-ended)



❑ **2-piece model representation**

$$i(t) = w_H(v,vdd,t)\, i_H(v,vdd,d/dt) + w_L(v,vdd,t)\, i_L(v,vdd,d/t)$$

$i_{H,L}$: submodels accounting for buffer behavior @ fixed logic H and L state

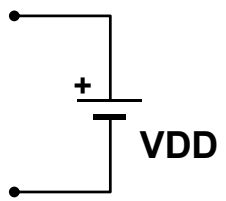
$w_{H,L}$: weighting signals for state switchings

❑ **Underlying (simplifying) assumptions**

Model parameters computed for the **nominal power supply VDD**

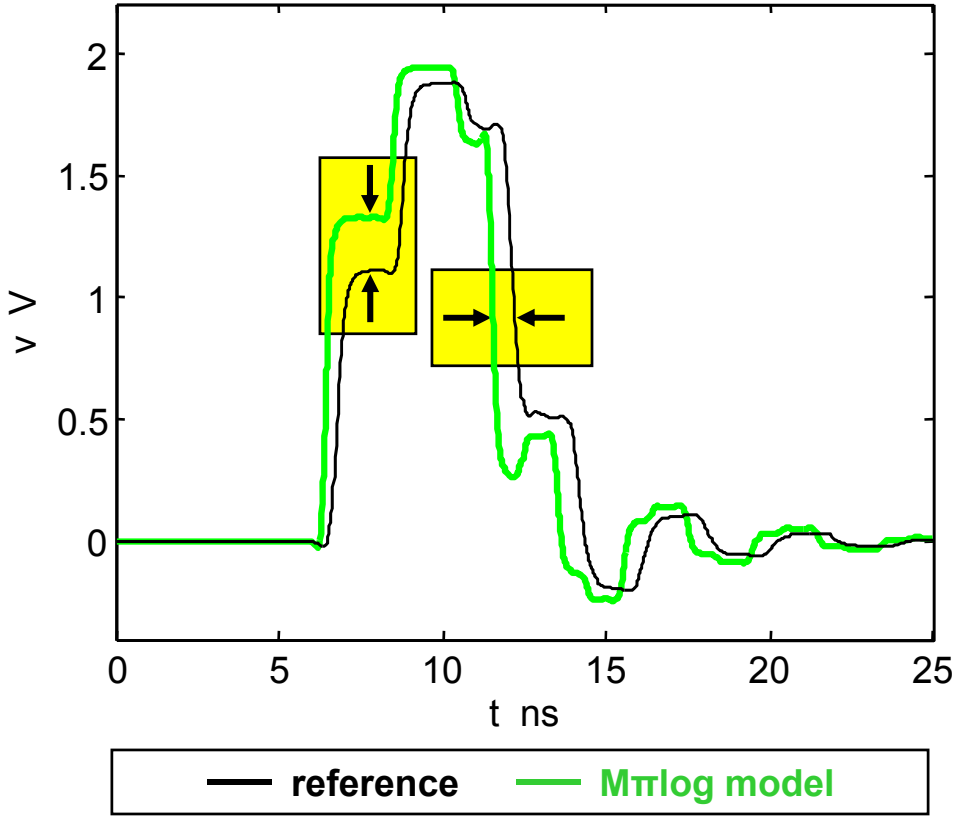
Weighting signals → $\mathbf{w_{H,L}(t)}$

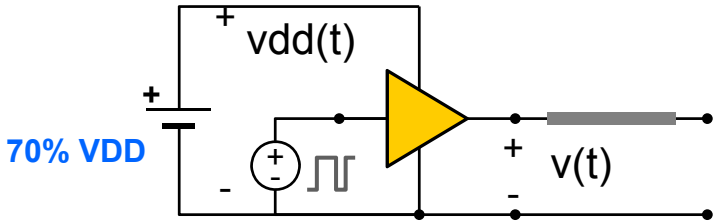
Submodels $i_{H,L}$ → $\mathbf{i_H = i_H(vdd\text{-}v,d/dt)}$, $\mathbf{i_L = i_L(v,d/dt)}$



Mπlog model structure, cont'd

- Ideal power supply @ 70% VDD

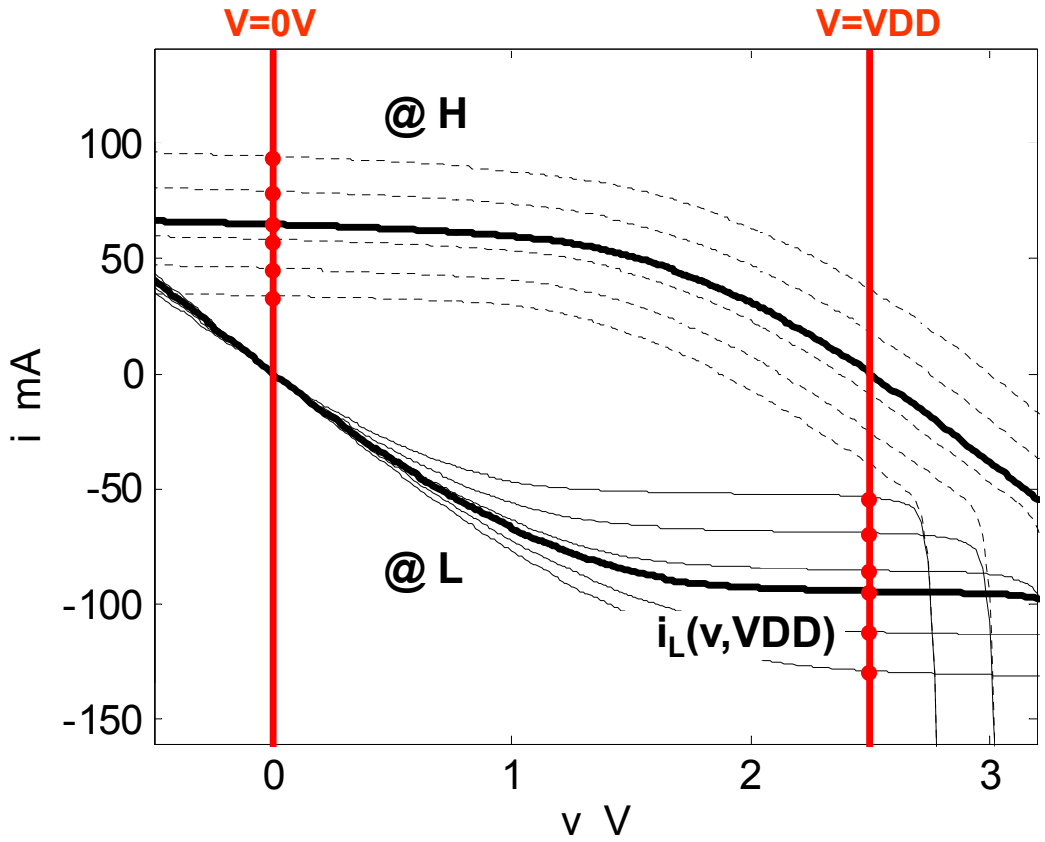




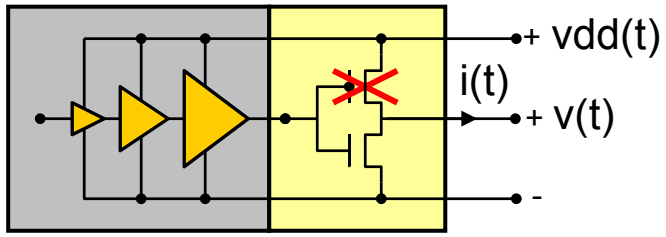
- Static error
- Timing error (delay)

A – static compensation

❑ **Static surface for vdd ∈ [70,130]%VDD**



e.g., Device @ L state

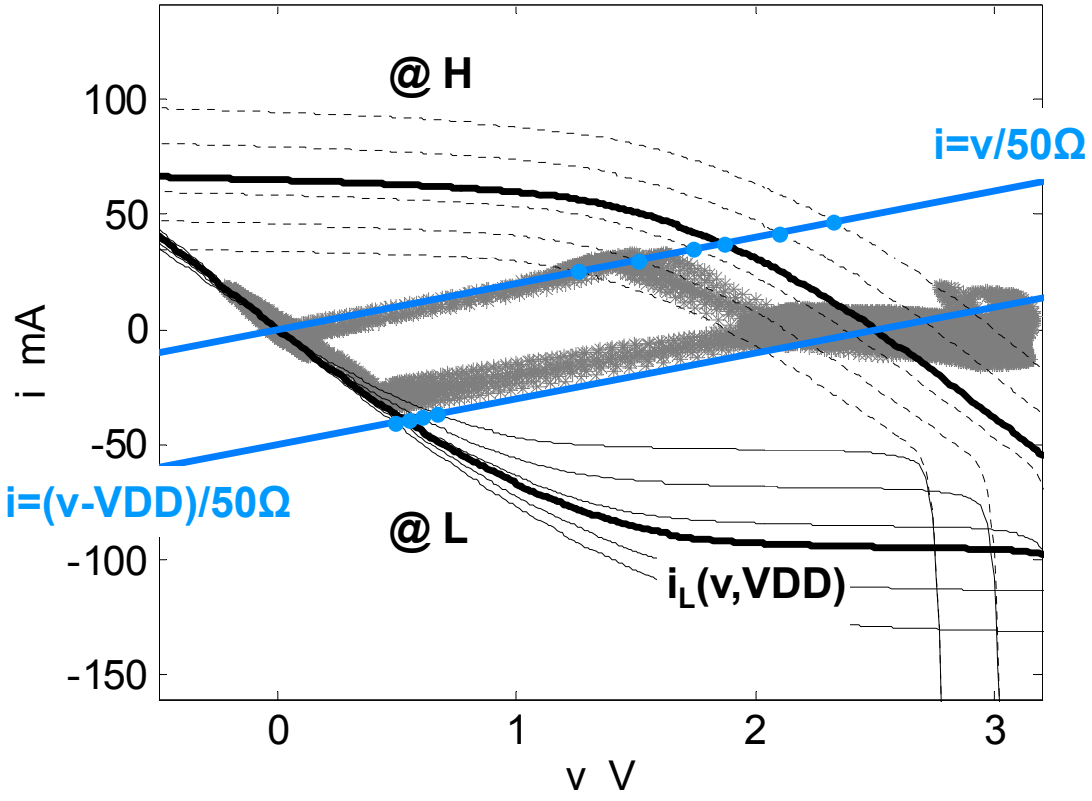


- State-of-the-art: i_L(v,VDD) (—)
- Complete 2D surface **(model complexity increases)**
- i_L(v,vdd) = k_L(vdd)* i_L(v,VDD) [2]

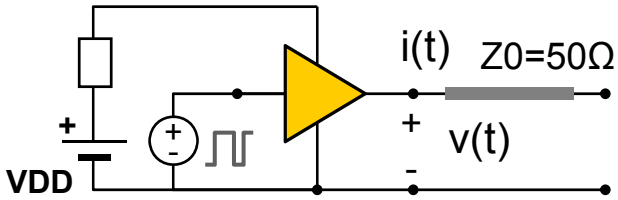
[2] Arpad Muranyi et. Al., "Gate Modulation Effect (table format)," IBIS BIRD #98.1, May 20, 2005.

A – static compensation, cont'd

- **Static surface for vdd ∈ [70,130]%VDD**



- **Actual i-v operating region**



- **Proposed model**

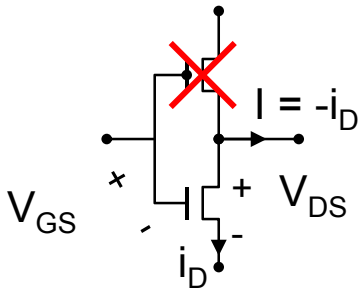
$$i_L(v,vdd) = k_L(vdd)^* i_L(v,VDD)$$

computed along the TL load lines

A – static compensation, cont'd

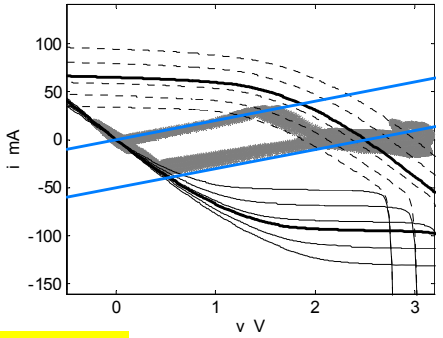
$$i_L(v,vdd) = k_L(vdd)^* i_L(v,VDD)$$

- include the information of the analytical MOS equations
- triode region [3]



$$i_D \cong A_n (V_{GS}V_{DS} - V_{DS}^2/2)$$

- A_n fitted with $i_L(v,VDD)$ (—)
- k_L **(vdd)** by matching analytical NMOS equation with model equation along the **load lines**

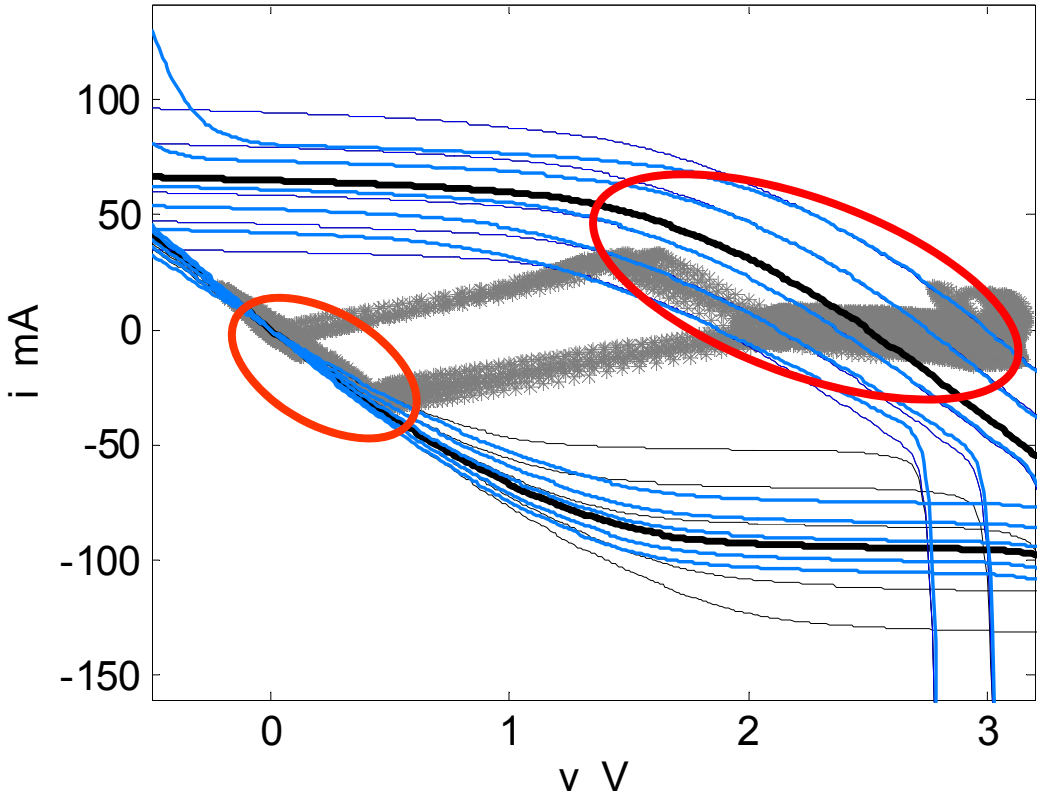


- **Need of static characteristics @ VDD only (—)**

[3] Jan M. Rabaey, "Digital Integrated Circuits - 2nd ed.", Prentice Hall electronics and VLSI series, 2003

A – static compensation, cont'd

- **DC model response**



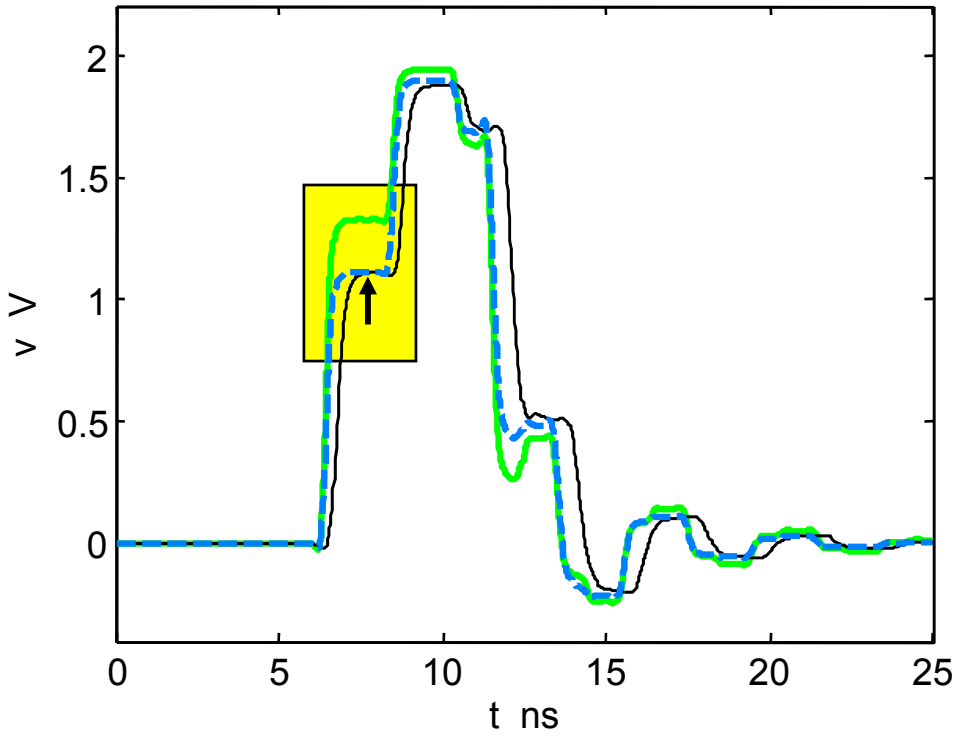
Relative errors less than 2%

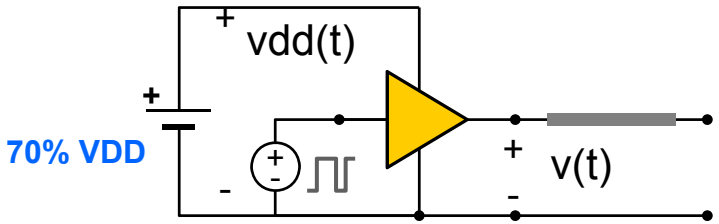
Possible discrepancies outside the operating region do not affect model accuracy

reference — **enhanced model (static comp.)**

A – static compensation, cont'd

- **Ideal power supply @ 70% VDD**



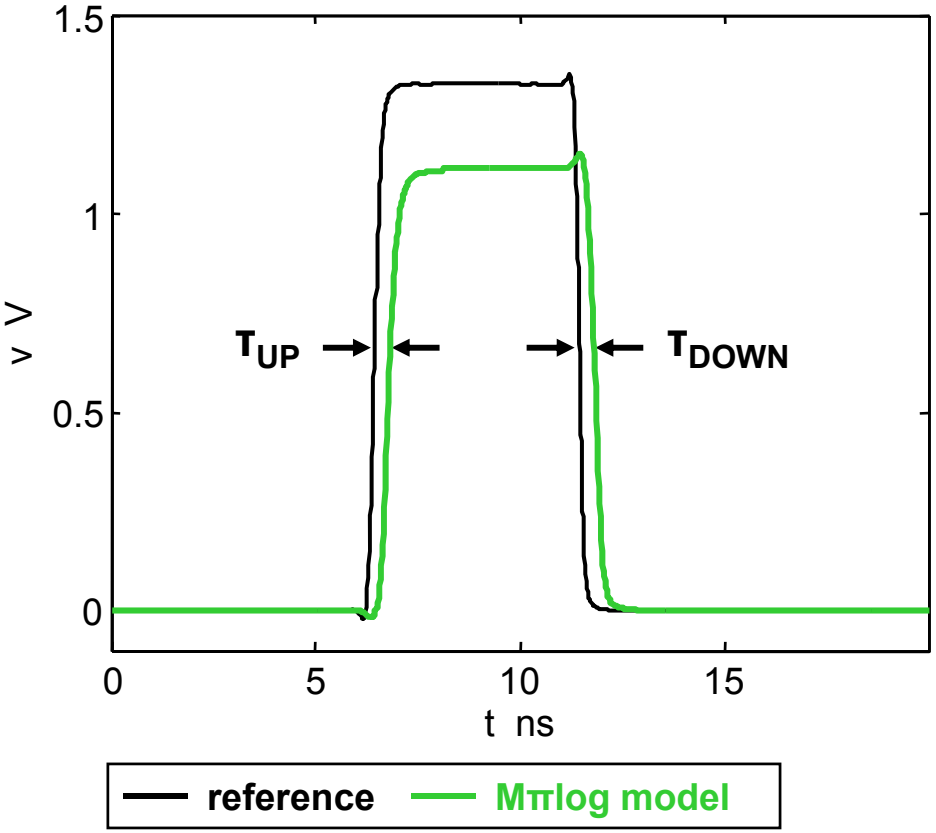


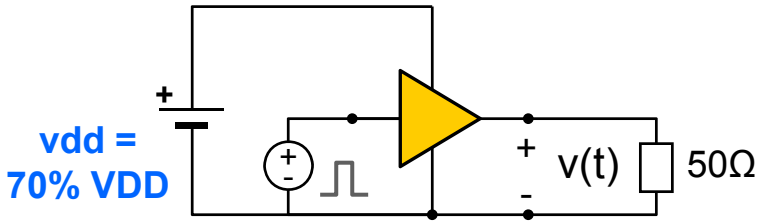
reference — MπIog model

enhanced model (static comp.)

Accurate prediction even with a very simple approximation of the 2D static surface

B – delay compensation



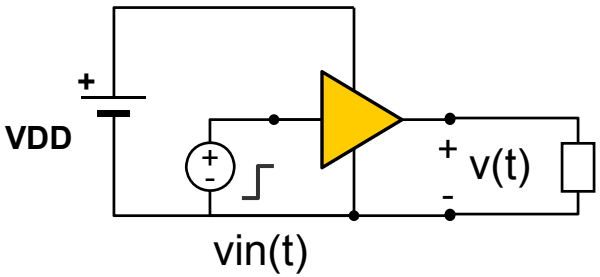


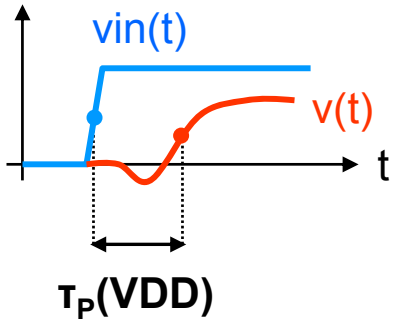
- **Embed** the τ (UP,DOWN) information in the model

$$w_{H,L}(t) \rightarrow w_{H,L}(t - \tau(vdd))$$

B – delay compensation, cont'd

- **Delay propagation [3]**





$\tau_P(vdd) \cong \tau_P(VDD) * (VDD/vdd)$ (accuracy: ~ 5%)

$$w_{H,L}(t) = w_{H,L}(t - \tau(vdd))$$

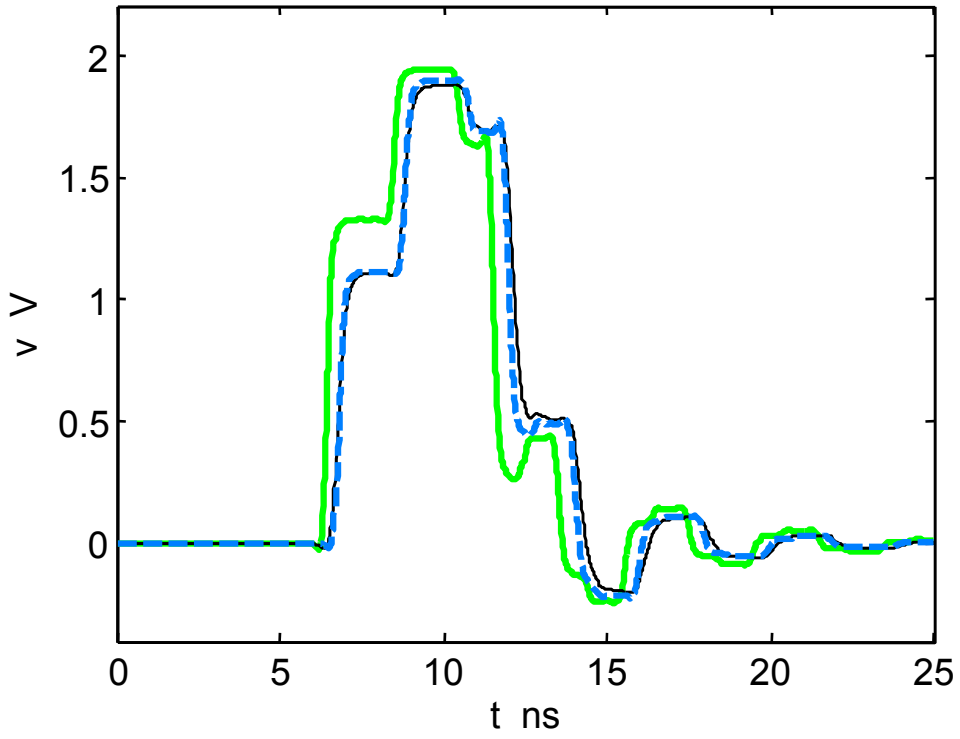
$$\tau(vdd) = \tau_P(VDD) - \tau_P(vdd) = \tau_P*(1-VDD/vdd)$$

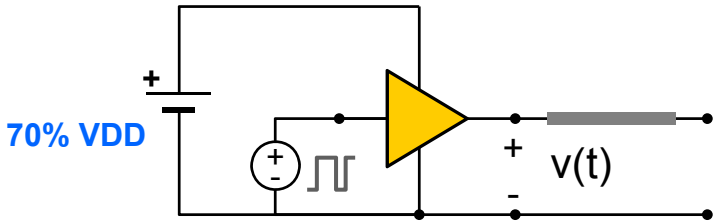
No additional information is required

[3] Jan M. Rabaey, "Digital Integrated Circuits - 2nd ed.", Prentice Hall electronics and VLSI series, 2003

Enhanced model performance

- Ideal power supply @ 70% VDD





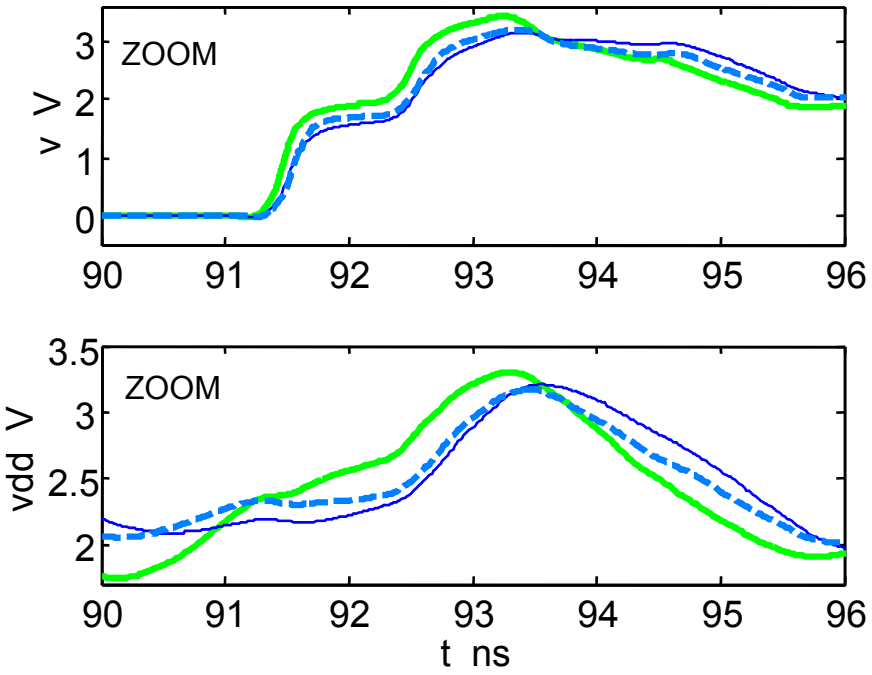
reference — MπIog model

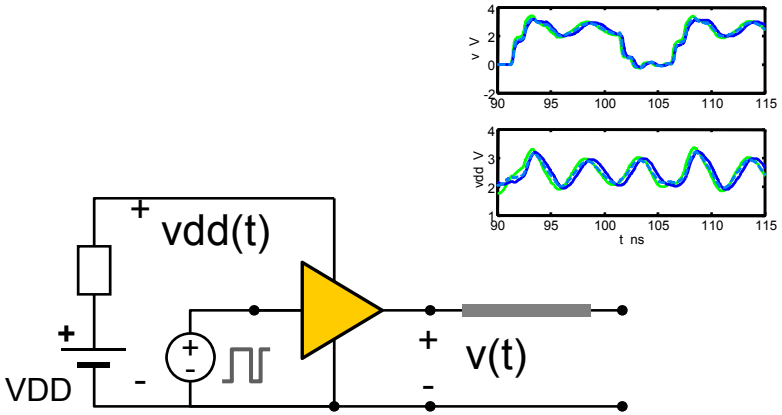
enhanced model (static & delay comp.)

Good accuracy
Same results for 130% VDD

Enhanced model performance, cont'd

- **Realistic test**





reference — MπIog model

enhanced model (static & delay comp.)

Accuracy confirmed for vdd(t) > 40% VDD

Current vs. enhanced models

$$i(t) = w_H(v,vdd,t)\, i_H(v,vdd,d/dt) + w_L(v,vdd,t)\, i_L(v,vdd,d/t)$$

Model	Submodels $i_{H,L}$	Weighting signals $w_{H,L}$
Mπlog	$i_{H,L}(v,VDD,d/dt)$	$w_{H,L}(t)$
Enhanced Mπlog	$i_{H,L}(v,vdd,d/dt)$	$w_{H,L}(t-\tau(vdd))$

- no additional characterization required
- same complexity → same speed-up (10 ÷ 100x)

Conclusions

- Generation of enhanced device models for large VDD variations (>30%)
- Simplified analytical equations for static & delay compensation
- High accuracy verified on realistic tests
- Apply to different device types (e.g., precomp)

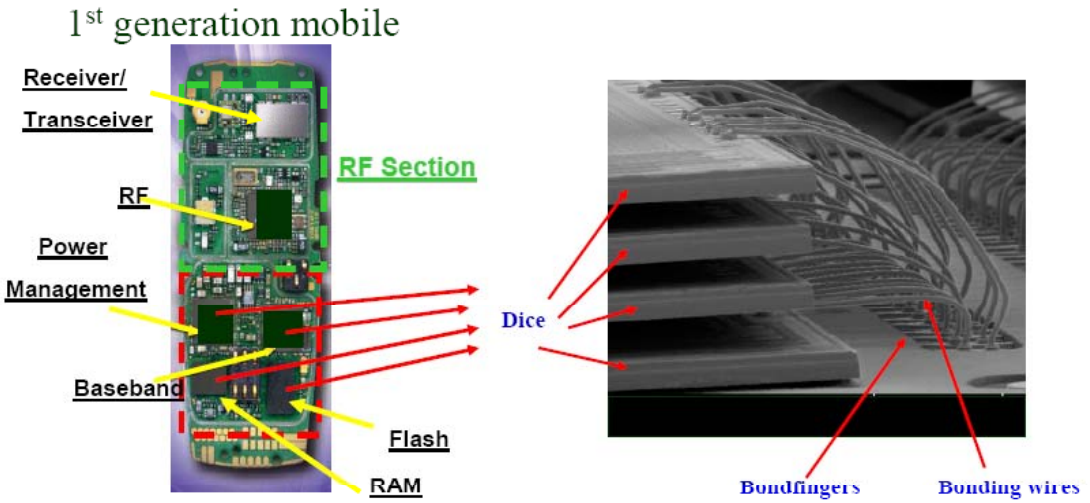
MOCHA, MOdelling and CHAracterization for SiP - Signal and Power Integrity Analysis

❑ European Project FP7-ICT-2007-1 (Jan 2008 – Dec 2009)

"Develop reliable modelling and simulation solutions for SiP design verification"

❑ Partecipants:

- **STMicroelectronics M6 SRL (Italy)**
- Politecnico di Torino (Italy)
- Cadence Design Systems Gmbh (Germany)
- Agilent Technologies (Belgium)
- Universidade de Aveiro (Portugal),
- Microwave Characterization Center (France)



❑ Work Packages

- IC power integrity model
- **IC buffers' innovative modelling approach**
- SiP design and verification EDA platform
- SiP signal integrity measurement platform

Q&A