# **EIA IBIS Open Forum Summit Minutes**

Meeting Date: March 14, 2008

### GEIA STANDARDS BALLOT VOTING STATUS

See last page of the minutes for the voting status of all member companies.

#### **VOTING MEMBERS AND 2008 PARTICIPANTS**

Agilent	Sanjeev Gupta, Radek Biernacki, Amolak Badesha			
	Fangyi Rao, Ian Dodd, Yutao Hu, Vuk Borich			
	Nobutaka Arai, Ludwig Eichingner*			
AMD	Nam Nguyen			
Ansoft Corporation	Steve Pytel			
Apple Computer	(Bill Cornelius)			
Applied Simulation Technology	(Fred Balistreri)			
ARM	(Nirav Patel)			
Cadence Design Systems	Terry Jernberg, Hemant Shah, Ambrish Varma			
Ois an Oriente ma	C. Kumar, Brad Grimin			
Cisco Systems	Syed Hud, Mike LaBonte, AbdulRanman (Abbey) Ratiq			
	Huyen Pham, Emily Yao, Susmita Mutsuddy			
	John Fisher, Paul Ruddy, Jun Li, Jianmin Zhang			
	Luis Boluna, Kelvin Qiu, Jane Lim, Ilyoung Park			
	Rick Brooks, Chris Padilla, Ehsan Kabir			
Ericsson	Anders Ekholm			
Freescale	Jon Burnett			
Green Streak Programs	Lynne Green			
Hitachi ULSI Systems	Kazuyoshi Shoji*			
Huawei Technologies	Tao Guan, Xiaoqing Dong			
IBM	Adge Hawes			
Infineon Technologies AG	Christian Sporrer*			
Intel Corporation	Michael Mirmak, Rich Mellitz			
IO Methodology	Lance Wang, Zhi (Benny) Yan, Li (Kathy) Chen			
LSI	[Frank Gasparik], Brian Burdick, Kim Helliwell			
Marvell Semiconductor	(Itzik Peleg)			
Mentor Graphics	Arpad Muranyi, John Angulo			
Micron Technology	Randy Wolff			
Nokia Siemens Networks GmbH	Eckhard Lenski*, Klaus Huebner*, Katja Koller*			
Panasonic	(Atsuji Ito)			
Samtec	Jim Nadolny, Justin McCalister			
Signal Integrity Software	Mike Steinberger, Walter Katz, Todd Westerhoff			
Ciarity	Doug Durris, Mike Mayer, Barry Katz			
Signity	Sam Gintwood, Brad Brinn, Ben Franklinn,			
CTMiereeleetreniee				
SINICroelectronics	(Anii Kala)			

Synopsys	Ted Mido			
Teraspeed Consulting Group	Bob Ross, Tom Dagostino, Al Neves			
Texas Instruments	Richard Ward			
Toshiba	(Yasumasa Kondo)			
Xilinx	David Banas, Ajay Shah, Suzanne Yiu			
	Mustansir Fanaswalla			
ZTE	(Ying Xiong)			
Zuken	Michael Schaeder*, Ralf Bruening*			

#### **OTHER PARTICIPANTS IN 2008**

Aeroflex Metelics David Nguyen Aica Kogyo Akihiro Tanaka Altera Ravindra Gali, Jing Wu, John Oh, Hui Fu Minh Quach, Sari Tocco Avago Technologies Bayside Design Elliot Nahas, Kevin Roselle Celestica Ihsan Erdin ECL Advantage Thomas Iddings **Ekkehard Miersch\*** EFM Elma Bustronic Michael Munroe Exar Helen Nguyen Flextronics Hasnain Syed GEIA (Chris Denham) Golden Bridge Networks Saman Sadigh **ICT Solutions** Steven Wong NetLogic Microsystems Eric Hsu Nokia Ali Arsian\* Nuova Systems Zhiping Yang Politecnio di Torino Igor Stievano\* Physware Marc Kowalski Qimonda AG Md Morshed Alam Heial\*, Suhas Jawale\* Siemens AG Manfred Maurer\*, Annika Woehner\* Simberian Yuriy Shlepnev SimLab Software GmbH Heiko Grubrich\* Tektronix Steve Corey TietoEnator GmbH Heinz-Hartmut Ibowski\* Tyco Electronics Chad Morgan Vertical Circuits Mark Egbers Robert Bada Xsigo Systems Independent Guy de Burgh, Ardy Forouhar, Dave Galloi Kazuhiko Kusunoki

In the list above, attendees at the meeting are indicated by \*. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

#### **UPCOMING MEETINGS**

The bridge numbers for future IBIS teleconferences are as follows:

Date	Telephone Number	Meeting ID
March 14, 2008	1-866-432-9903	1-2135-7831

All meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, press 1 to attend the meeting, then follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing\_business/conferencing/index.html

NOTE: "AR" = Action Required.

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#### INTRODUCTIONS AND MEETING QUORUM

No new participants.

#### INTRODUCTIONS AND MEETING QUORUM

The IBIS Open Forum Summit was held in Munich, Germany at the ICM Convention Center during the 2008 Design Automation and Testing in Europe (DATe) Conference. About 20 people representing 13 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda-stds.org/ibis/summits/mar08/

Ralf Bruening welcomed everybody to the 11<sup>th</sup> European IBIS Summit meeting in Munich. He said he is looking for news with respect to new IBIS modeling features, as the summit is the place where the exchange of experiences takes place and where new problems can be discussed.

He thanked the sponsors including Sigrity, Agilent Technologies, Mentor Graphics, Infineon, Zuken, and Nokia Siemens Networks.

Ralf reported on an agenda change. Unfortunately, Saliou Dieye of Agilent Technologies encountered flight delays and could not attend. So the last scheduled presentation titled "New Interconnect Models Remove Simulation Uncertainty" had to be cancelled.

Ralf then asked everyone to introduce themselves. (Thanks to Eckhard Lenski for taking minutes.)

#### DRIVER SCHEDULE: PRE-/DE-EMPHASIS AND FREQUENCY/DATA RATE ISSUES

Eckhard Lenski, Nokia Siemens Networks, Germany

Eckhard started with a short review about pre-/de-emphasis. He explained that despite the two logic states for high and low, there might be four states. These can be defined from pre-/de-emphasis settings as "low", "low-pre", "high" and "high-pre". He showed that four different switching modes can be defined that correspond to the last logic state prior to the switching.

He continued with some remarks about the availability of information on [Driver Schedule] modeling, which can be found either in a lot of IBIS summit presentations, in the IBIS Cookbook 4.0 and IBIS Version 4.2. He showed that is very important to know which static curves of which model are used in the [Driver Schedule]. These are the [POWER Clamp] and [GND clamp] curves from the top level model and the [Pullup] and [Pulldown] curves from the scheduled models. He than compared a data signal with a clock signal, with the important parameter of UI (Unit Interval) for a data signal and the clock period for a clock signal. He said that from the UI, it is very simple to calculate the data rate, by calculating the reciprocal. He pointed out that for a data pattern that is composed of alternating 1s and 0s, a maximum corresponding frequency of the data rate can be calculated as F = (Data rate / 2).

He then explained that, for a classical IBIS model, a max frequency where the model can be used at is calculated out of the rising and falling times of the waveforms by: Fmax = 1 / ( trise + tfall ). By using a [Driver Schedule] for SerDes multi-gigabit applications, this is no longer true, as now it has to be taken into account that a signal has to be long enough above the high-threshold or below the low-threshold, which results in an eye diagram.

He then showed the influences of using a normal push-pull CMOS model at increasing frequencies, which end up that the model looks suspicious when the frequency is greater than Fmax = 1 /( trise + tfall ). From the signal characteristics of a model with pre-emphasis, it can be seen that both the rising and the falling edges contain information for two bits or two UI. The first bit shows the emphasized behavior of the output, while the second bit shows the behavior without pre-emphasis.

Five examples were shown of using a [Driver Schedule] model at different clock frequencies. For 250MHZ and 500MHz both the logic state with and without emphasis can be seen. At a frequency of 1000MHz, the signal just shows a switching from high-pre to low-pre. All five examples showed that the use of a [Driver Schedule] model in n 'clocking or frequency' application is not valid. So therefore the use a PRBS (pseudo random bit sequence) is necessary, to really show all possible switching modes of the model containing pre-emphasis. Eckhard continued with 4 examples that used different UI to show a realistic behavior. He said that only by using the correct UI in the simulation, which is the same UI that is encoded in the model, a correct switching and/or eye diagram could be measured.

In his summary he pointed out that normal push-pull CMOS models can be used up to a specific frequency Fmax, but a [Driver Schedule] modeling pre-emphasis can only be used for one data rate. The reason for this is that in this [Driver Schedule] model a data pattern of 1100 is encoded in the model behavior which will only be valid for the corresponding UI or data rate (in comparison to the push-pull CMOS model, which only has the classical 10 pattern encoded). He closed with the remarks that the user himself has to take care of using the correct data rate, as the tool doesn't care about the UI or encoded pattern of the model.

The first question was if there is really a need for a new model for each data rate. Eckhard answered that as the results he made have shown, this is really the case. The second question was, whether Eckhard had already compared the behavior of a real device showing preemphasis in comparison to the model. Eckhard had not, and he figured out that the problem of [Driver Schedule] is the modeling of normally two different models, one for the main buffer and one for the boost buffer, and both buffers switching to their specific load. Later on in the simulation, the tool will have to put these two buffer behaviors together to get a switching behavior. For the static curves the voltage levels can be calculated manually, but the transient behavior is up to the tool. Dr. Miersch stated that the pre-emphasis in accordance to the application would change, so that not only the data rate, but also e.g. the line length will afford a new model.

#### **IQC - IBIS QUALITY CHECKER**

Manfred Maurer\* and Christian Sporrer\*\*, \*Siemens AG, and \*\*Infineon Technologies AG, Germany

Manfred noted that the idea for this IBIS checker came up about two years ago in the Siemens IBIS Group (SIG). The intention was to improve IBIS model quality. On the SIG web page there are explanations of IBIS, details of what is expected from IC vendors concerning model quality and also the reasons why. Furthermore, on this web page hints and examples about good IBIS modeling can be found. He pointed out that regardless of the simulation tool used, the quality of the models are the main factor for good simulation results.

He continued by mentioning that the first attempt in this direction was the Excel sheet from the IBIS Quality task group. This Excel sheet contains about 80 lines of quality issues (for each model), so for manual checking this will be time consuming. This might be also the reason for the low acceptance until today.

Manfred has the impression (which he got from talks with many vendors and users) that an automation of these checks is necessary. The advantages of the checklist are an increased confidence in the models and better comparability between models. At the moment there are disadvantages for the vendor because it is very time consuming, and for the user there are only restricted consistency checks possible with no possibility of proving the quality info.

He mentioned that almost every company has its own scripts for testing the models, and that it might be better if the same quality checks would be available for all. Furthermore, the quality would have to be improved only once (by the vendor). He proposed one possible proceeding, which is based on the Excel sheet summary of the IBIS Quality task group and on the needs and requests from the SIG.

The concept should set priorities according to the Pareto principle (80/20). The structure should be a modular one, and later on this program could be transferred to the Quality group. He then showed an overview of the structure of the IQC. There will be a configuration file as well as a parameter file. The configuration file will contain less restrictive values for checking parameters, while the parameter file might contain more specific/restrictive values. The output will contain a message file in both ASCII format and graphic format and also a result file with all the accomplished checks. There will be consistency checks as well as curve evaluations and curve checks, but also information about the number of present models and pins will be there.

Eckhard then turned the presentation over to Dr. Christian Sporrer, who has implemented the first steps of the IQC.

Christian continued with an overview of the implementation. There is an IQC library, which contains functionality form computational tasks as well as executables with IBIS checks and datasheet checks. The checker will make usage of plug-in modules by using encapsulation. This means that the check does not work directly, but will use methods. He then explained the structure of both the parameter file and the configuration file. They are grouped into 5 sections: package, pin, model general, model specific and data sheet.

The configuration file will contain more general parameters for a first basic model check, while the parameter file will contain more specific or more restrictive values/checks. He explained these files with two examples. He then showed an overview of the File I/O methods in the IQC library. There are different files with different methods for checking the models, but the names of these methods should be self explanatory. Examples are getconfigurationvoltage, gettolerance (which will check for the tolerance of the power supply) and getibispinlist.

The computing methods are the computational part of the check with names like compareValues(), checkRampOrder() and countModels(). On the next slide he showed the checks that are already implemented in the IQC demonstrator. They contain section A (package), section B (pins), section D (models) and section E (datasheet). Afterwards, he explained how a new check could be added to the IQC. Everything should be implemented as methods for a high level of reuse as well as a high level of modularity. At the end he showed an excerpt of the Perl program with the voltage check plug-in.

In the summary he pointed out that the IBIS Quality checklist would only have a chance if most of it can be automated; the benefits are clear, but no one has started using it yet. There will be a lot of work to do to implement the tool if all checks are to be included at once. He suggested that this should be done step by step and invited everybody to help out.

The first question was whether a vendor will support the configuration and parameter files. It was answered that there won't be any problems concerning the confidential aspects, but the use of these files is user dependent, so usually the files will have to be application specific.

Another observation was that the user normally doesn't want to do these checks, and that everything should be shifted to the vendor. Will this be possible? Christian answered that the advantage of the IQC would be that, not only the will the parser checks be fulfilled (with the IBIS parser), but also, additional quality checks will be accomplished. But, of course, a reference platform for model checks would be fine. By giving the vendor a reference platform they will get good information on how to check the models beyond the IBIS parser and checklist, because the model in-sourcing can only be done when the supplier delivers a good model. Christian pointed out that it might be possible to deliver to the customer an application specific model, which then will work explicitly for this costumer, but that this also might lead to additional costs.

The last observation was that a check of the curves is also very important, and that this might be the trickiest part to do.

# PROPER IBIS PACKAGE MODELING TECHNIQUES AND USAGE IN IDEAL PDS AND SSO SIMULATIONS

Sam Chitwood, Sigrity, USA (Presented by Brad Brim, Sigrity, USA)

Brad pointed out that IBIS is a well-established standard, and therefore it helps a lot to define how an IBIS model should look and which information it should contain. But he also pointed out that as with many things, there are some limitations which should be overcome. This is especially true for power integrity analysis, where a lot of improvements are needed.

He explained that in IBIS there is an assumption of a 1:1 relationship between the die pads and the board pins. He figured out that this is true for lead frame packages, but for modern BGA packages, there are power planes inside the package and not only pads. [Pin Mapping] is a first step in the right direction, but he remarked that these connections with the current IBIS standard are ideal and no die parasitics are taken into account.

He continued with the [Pin] list keyword. In this list all pins should be included, but very often the power and ground pins are omitted. What is missing here is that there is no coupling modeled between the pins. There are some limitations for the [Pin] parameters for PDS simulations, e.g. there are no mutual values, and therefore no current loops can be defined. Furthermore, for high frequency, both power and ground pins have to be assumed as RF ground. For using the [Pin] list in signal modeling, there are three problems: C\_pin should be divided in C\_pin-PWR and C\_pin-GND like it is done with C\_comp; for inductance there is no mutual inductance, so it is difficult to define a current return path; the parameter R-pin has no frequency dependency, so one does not know if the skin effect is included or not.

Brad continued with hints for proper extraction of [Pin] inductance, resistance and capacitance, but noted that you still have to keep in mind that these values should only be used for an ideal PDS simulation. So, for all measurements, the power and ground pins should be AC-shorted, by doing so, the inductance will become L\_loop, including mutual inductance, and capacitance will become C\_total, including C\_pwr-signal, C\_gnd-signal and C\_sig-signal.

For the values in the [Package] section he explained, that very often in the min and max columns, there is a mixture of signal pin values and power pin values. This results in values of L\_pkg which are too small and C\_pkg which are too big (summation of parallel C's and parallel L's in power pins).

Advanced packaging features may be used through the [Define Package Model], which itself can be separated in two types. One is the [Number of Sections], which has the same drawbacks as the [Pin] parameters. The second is [Model Data], which is a real improvement, because you can model coupling between pins. He continued with a suggestion for the extraction of the parameters, where for better results all corresponding power pins and ground pins should be lumped together as positive or negative references respectively. It is important that now there would be just one pin listed for the power pins, and the ground pin would not even be listed. He showed a picture which showed that the performance of an IBIS RLC model could be improved by using a broadband approach of using frequency dependant matrices. He ended his presentation with remarks of not using on-die de-caps in the package models, as this will cause resonance-problems, and that only the pins which do have de-caps should be mentioned.

# MACROMODELS OF IC BUFFERS ALLOWING FOR LARGE POWER SUPPLY FLUCTUATIONS

Flavio Canavero, Ivan Maio, and Igor Stievano, Politecnio di Torino, Italy Igor started his presentation with the information that there are real parts like stacked SiP devices that show a power variation in VCC of about 30-40% from the nominal value. This is far beyond the approach of BIRD 98.1, which will cover variation of approximately 10-15%.

He continued by showing that this problem is common to all kinds of behavioral models like IBIS,  $M\pi$ log, etc. He gave an overview of the structure of the  $M\pi$ log model and explained that all the necessary parameters have been computed for the nominal power supply. Two errors for the model behavior were shown when using large power supply variations. The first is a static error, which showed up in different voltage values for the output behavior. The second error could be identified as a timing error, because the overall behavior showed a delay compared to the reference.

One choice to improve the model would be to extract all the different static curves for each corresponding VCC value, but this might be too time consuming. So he thought about reducing this by looking at the actual operating range of the device. He found that around the load-curves with 50 ohms to VCC and 50 ohms to ground a region could be found where a device is normally operated. By including this information (operation around the load lines) in the M $\pi$ log model, the static errors disappeared.

This was done by matching the correcting factor  $k_L(vdd)$  to analytical NMOS equations. Igor pointed out that this region is also valid for using the model under pure capacitive load conditions. His next slide showed that the dc-errors had disappeared, but the dynamic errors still were there. So now this delay had to be modeled. He showed that in standard books there exist equations which describe the delay propagation in accordance to VCC fluctuations with an accuracy of approximately 5%. After adding this corrective factor to the new M $\pi$ log model, the dynamic error disappeared.

A comparison between the old and the enhanced  $M\pi \log$  model was shown. He pointed out that the main advantage of this method is that no additional characterization is required. So just by enhancing the nominal  $M\pi \log$  model with the two correction factors for VDD variation, one can deliver models which include the behavior for large VDD variations. These enhanced models are still very accurate.

A question was asked for which classes of circuits this approach is valid. Igor answered that it is valid for classical devices which have a digital output, but also for differential outputs and even for precomps. For precomps one has to take into account that the modeling must be done in a different way, because the rule/equation for the deviation of VDD is greater than 5%, so the delay error has to be modeled differently. Igor pointed out that even the mentioned stacked SiP could be modeled correctly.

Someone asked if this approach would work for non-linear parts. Igor pointed out that the part had to be separated into a kind of sub system level with core, IO and supply considerations. The nonlinear part will be either extracted from simulation or has to be measured, but the package has not been under investigation.

The last question was about the validity of this load lines approach. Igor explained that in a

realistic operation the part would always be inside the gray area. But if the device will be loaded with a drastically different load, e.g. a 10 ohm load, than a new model for this load condition has to be created.

#### **BIRD 104.1 - AMI MODEL - NEW IBIS SUPPORT**

Manfred Maurer, Siemens AG, Germany

Manfred began the presentation by saying that many customers and IBIS users had asked him about AMI, and he pointed out that there had also been a lot of presentations at different IBIS summits during the last two years. There was the impression that it might not be possible to create an AMI model without knowledge of MATLAB or C++. He showed the advantages of a classical IBIS model in ASCII format. The easy readability of that standalone IBIS model meant that the engineer could look at the model directly. Then he pointed out that there had been a lot of improvements for IBIS models like [Driver Schedule], [Add Submodel] and even [External Model].

With the appearance of the AMI model a new level of model has come into being. It looks as if there is a growth of applications for this kind of model. The reason for this AMI model came from SerDes devices operating at frequencies above 5 GHz and their need to model equalization, feedback, clock recovery etc., and the need for simulation of extremely long (> 10 Million UI) bit streams. A large list of parameters is needed and is defined inside the model. These parameters might be platform, or even compiler, dependant. Furthermore, there are user defined parameters that are not easy to define (e.g. jitter, Rx-clock-PDF).

His next slide showed that there are three function signatures, AMI\_INIT, AMI\_GetWave and AMI\_Close, and writing these functions requires the knowledge of a lot of disciplines (software engineer, electrical engineer and mathematician). He explained that an AMI model contains many parts including the I/O-model, channel information, complicated source and sink circuits and control parameters. All this information will be packed in a DLL (dynamic linked library), so the user does not know explicitly if the model will run on his/her system with their specific version of operating system.

The AMI model consists of an electrical part and an algorithmic part. The electrical part contains the transmitter, receiver, and the channel that is characterized by means of an impulse response. The algorithmic part includes the equalization and the clock and data recovery and is connected by high impedance to the analog part. The modeling description is done by an executable code (MATLAB/C++). He ended with a summary of the advantages and disadvantages of the AMI model. Advantages include that the model shows maximal flexibility, protects proprietary information and shows a short simulation time for millions of UI (in comparison to any other traditional tools). The main disadvantage is that the model is no longer in ASCII-format, but is hidden in a DLL.

Manfred was asked if he had used the tool kit. He had used it and it was complicated, but in the end, he was successful. Multidiscipline knowledge was necessary. The next question asked about the time it took to get first results, and he said it was easy after he had talked to the toolkit suppliers. He was asked about the future of IBIS, and he said that during his attendance at the IBIS summit at DesignCon 2008, he got the answer from the experts. At the moment only SerDes will be modeled with AMI, but the rest of IBIS will stay.

He was asked further about the readability of the parameter file, and he pointed out that it is readable in the toolkit, but it has the complexity of a book. Another question referred to comparison of simulation and measurement, and Manfred said that from his knowledge, he doesn't know of any comparison between the AMI model and practical measurements.

There was a remark that the normal IBIS user needs simple things, but that the future might go in this direction. The next question asked whether the models for RX and TX are linear or not. Manfred explained that the models used are linear, but that also non-linear models might be possible. The last question referred to the power noise influence on the AMI model, how this might be included or if it is included in the jitter. Manfred assumed that as jitter and noise come through parameters, the channel becomes everything.

#### **CONCLUDING ITEMS**

Ralf Bruening closed the meeting by thanking the sponsors and attendees. The meeting was adjourned at about 14:15.

#### **NEXT MEETING**

The next IBIS Open Forum teleconference will be held March 14, 2008 from 8:00 AM to 10:00 AM US Pacific Time. A vote is scheduled for Touchstone 2.0.

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#### NOTES

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This meeting was conducted in accordance with the GEIA Legal Guides and GEIA Manual of Organization and Procedure.

The following e-mail addresses are used:

#### majordomo@eda-stds.org

In the body, for the IBIS Open Forum Reflector: subscribe ibis <your e-mail address>

In the body, for the IBIS Users' Group Reflector: subscribe ibis-users <your e-mail address>

Help and other commands: help

#### ibis-request@eda-stds.org

To join, change, or drop from either or both: IBIS Open Forum Reflector (<u>ibis@eda-stds.org</u>) IBIS Users' Group Reflector (<u>ibis-users@eda-stds.org</u>) State your request.

#### ibis-info@eda-stds.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the EIA-IBIS Open Forum as a full Member.

#### ibis@eda-stds.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting

information is not permitted.

#### ibis-users@eda-stds.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

#### ibis-bug@eda-stds.org

To report ibischk parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda-stds.org/ibis/bugs/ibischk/ http://www.eda-stds.org/ibis/bugs/ibischk/bugform.txt

#### icm-bug@eda-stds.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda-stds.org/ibis/icm\_bugs/ http://www.eda-stds.org/ibis/icm\_bugs/icm\_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda-stds.org/ibis/bugs/s2ibis/bugs2i.txt http://www.eda-stds.org/ibis/bugs/s2ibis2/bugs2i2.txt http://www.eda-stds.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eigroup.org/ibis/ibis.htm

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda-stds.org/ibis/directory.html

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### **GEIA STANDARDS BALLOT VOTING STATUS**

Organization	Interest Category	Standards Ballot Voting Status	February 1, 2008	February 7, 2008	February 22, 2008	March 14, 2008 Summit
Advanced Micro Devices	Producer	Inactive	1		1	
Agilent Technologies	User	Inactive		$\checkmark$		$\checkmark$
Ansoft	User	Inactive		$\checkmark$		
Apple Computer	User	Inactive				
Applied Simulation Technology	User	Inactive				
ARM	Producer	Inactive				
Cadence Design Systems	User	Active	$\checkmark$	$\checkmark$	$\checkmark$	
Cisco Systems	User	Active	$\checkmark$	$\checkmark$	$\checkmark$	
Ericsson	Producer	Active	$\checkmark$	$\checkmark$	$\checkmark$	
Freescale	Producer	Inactive		$\checkmark$		
Green Streak Programs	General Interest	Inactive			$\checkmark$	
Hitachi ULSI Systems	Producer	Inactive		$\checkmark$		$\checkmark$
Huawei	User	Active	$\checkmark$	$\checkmark$	$\checkmark$	
IBM	Producer	Active	$\checkmark$	$\checkmark$		
Infineon Technologies AG	Producer	Inactive				$\checkmark$
Intel Corp.	Producer	Active	$\checkmark$	$\checkmark$	$\checkmark$	
IO Methodology	User	Active	$\checkmark$	$\checkmark$	$\checkmark$	
LSI	Producer	Active	$\checkmark$	$\checkmark$	$\checkmark$	
Marvell Semiconductor	Producer	Inactive				
Mentor Graphics	User	Active	$\checkmark$	$\checkmark$	$\checkmark$	
Micron Technology	Producer	Active		$\checkmark$	$\checkmark$	
Nokia Siemens Networks	Producer	Active			$\checkmark$	$\checkmark$
Panasonic	Producer	Inactive				
Samtec	Producer	Inactive		$\checkmark$		
Signal Integrity Software	User	Inactive	$\checkmark$	$\checkmark$		
Sigrity	User	Inactive		$\checkmark$		$\checkmark$
STMicroelectronics	Producer	Inactive				
Synopsys	User	Inactive		$\checkmark$		
Teraspeed Consulting	General Interest	Active	$\checkmark$	$\checkmark$	$\checkmark$	
Texas Instruments	Producer	Inactive		$\checkmark$		
Toshiba	Producer	Inactive				
Xilinx	Producer	Inactive	$\checkmark$	$\checkmark$		
ZTE	User	Inactive				
Zuken GmbH	User	Inactive				$\checkmark$

#### I/O Buffer Information Specification Committee (IBIS)

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH GEIA BALLOT VOTING ARE:

- USERS MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
- PRODUCERS MEMBERS THAT SUPPLY ELECTRONIC EQUIPMENT.
- GENERAL INTEREST MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.