

JEITA EDA -WG Activity and Study of Interconnect Model Part-2

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European IBIS SUMMIT in Munich**

**JEITA EDA-WG
Takeshi Watanabe (NEC Electronics)
Atsuji Ito (Panasonic)
Kazuhiko Kusunoki (KAW/Keihin Artwork)**

JEITA ; Japan Electronics and Information Technology Industries Association

Outlines

- 1. JEITA EDA-WG Activities**
- 2. Short Term Direction of JEITA EDA WG**
- 3. Study of Interconnect Model**
- 4. JEITA IBIS Model Portal site**
- 5. Progress Report**

1. JEITA EDA-WG Activities

Objectives of JEITA EDA

EDA Model for

Digital Consumer Electronics

Cellular Phone, LCD /PDP TV,
Digital Camera/Video, DVD Recorder

(Digital , RF, and Analog circuits)

Auto Mobile Electronics ?

(Motor Drive, EMC)

< Applicability of IBIS V4.1 >

EMI, SI and PI for Digital Consumer Electronics

<Background>

EMI High-speed Clock Frequency

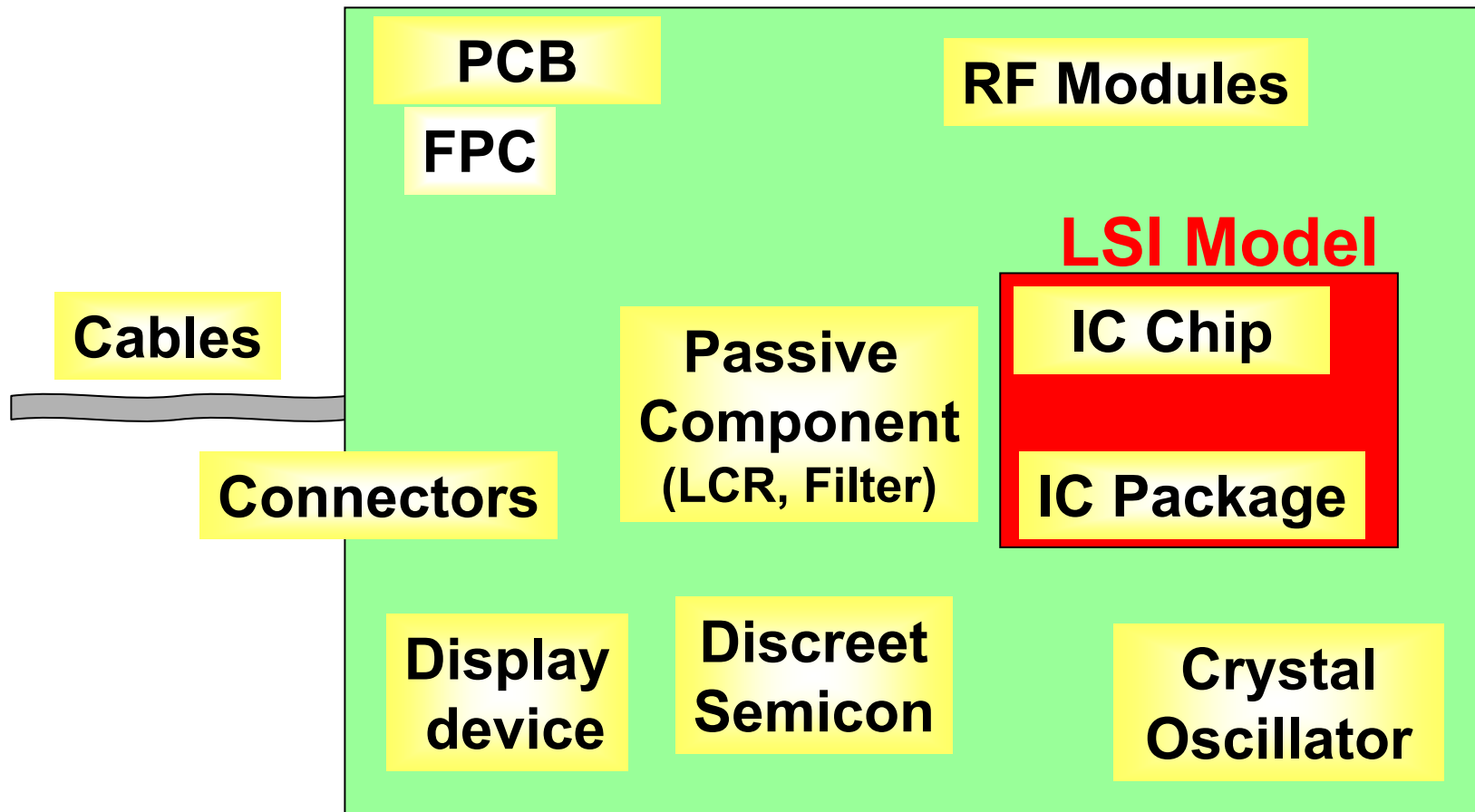
SI DDR, PCI, PCI-Express

PI High density and Large scale IC

SiP and Module, PCB level

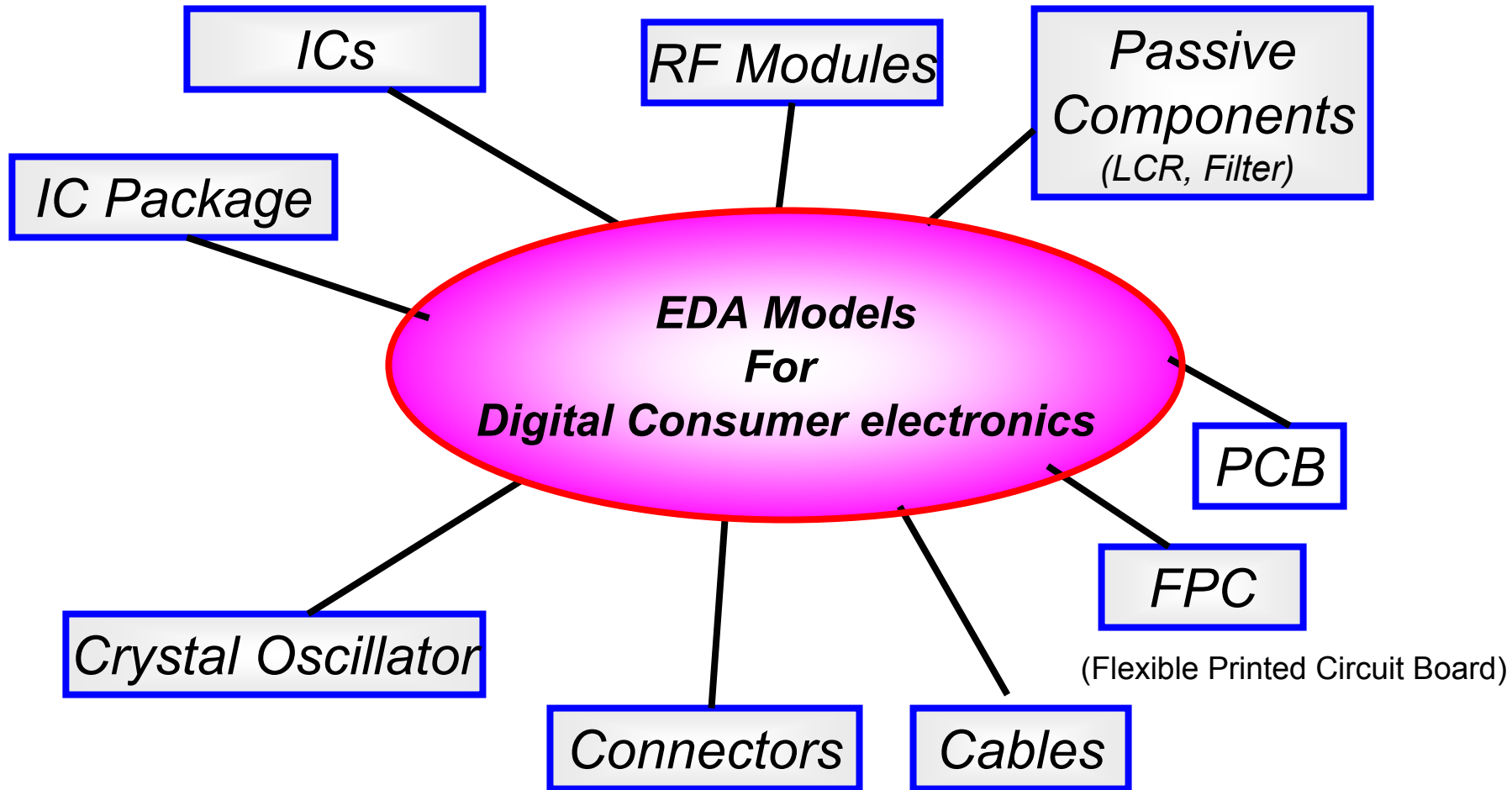
EMI, SI and PI Simulation Technology

EDA Model for EMI, SI and PI Simulation



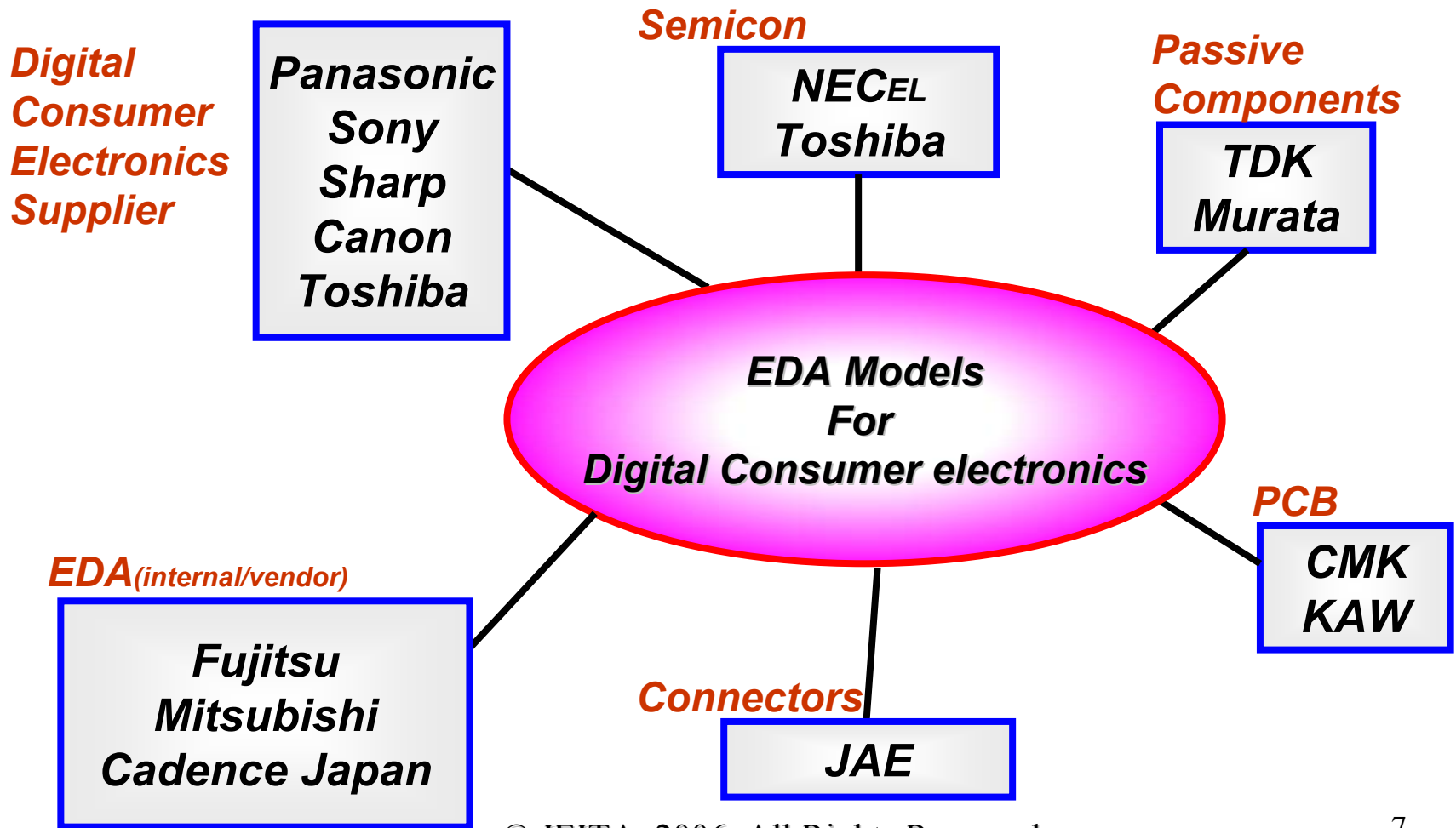
Focus of EDA Model for Simulation

9 components



JEITA EDA-WG Member

15 Major Companies

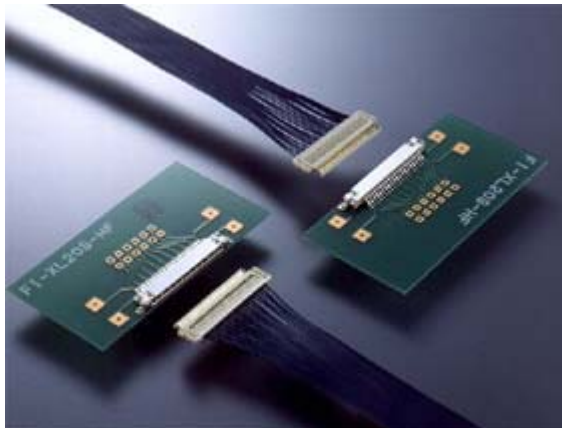
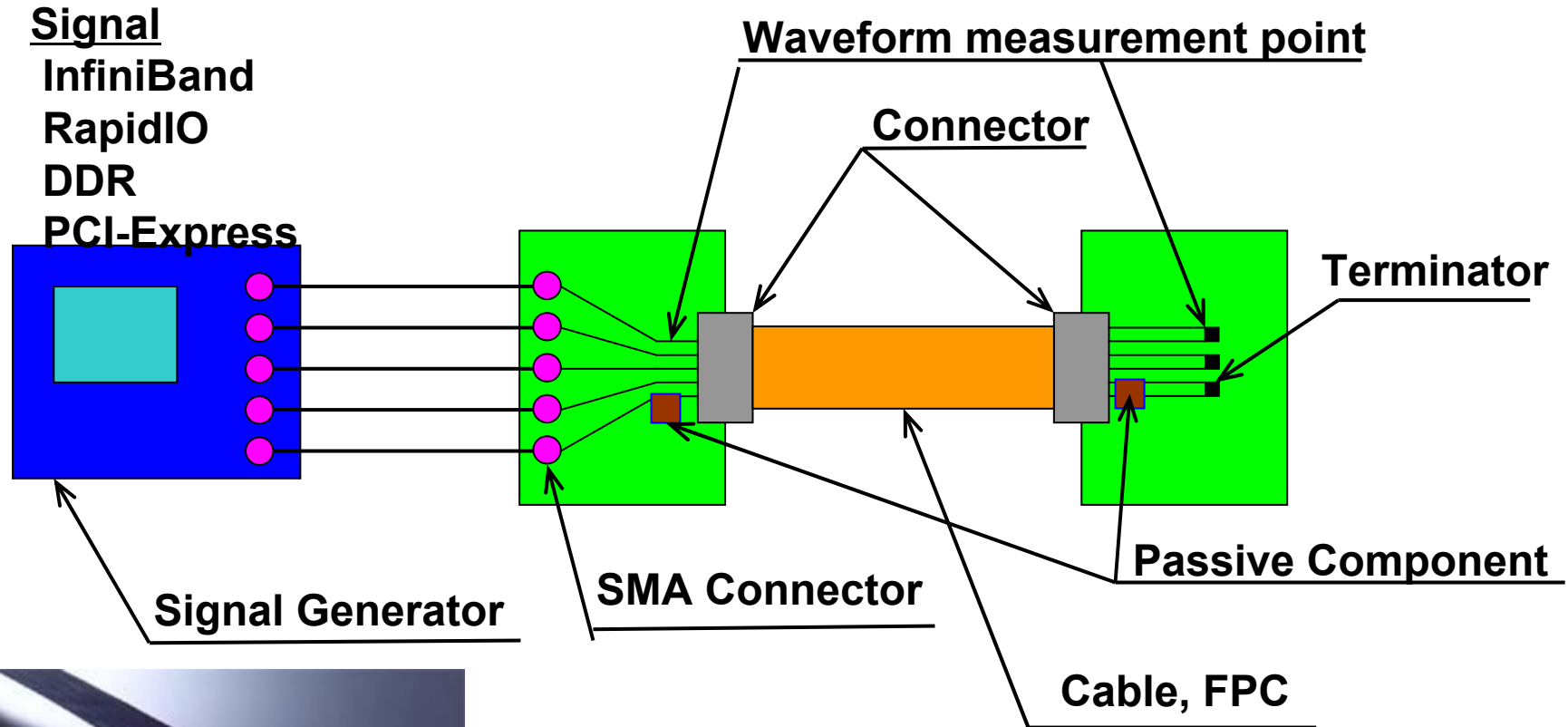


2. Short Term Direction of JEITA EDA WG

- Study of Interconnect Model
- IBIS Models of **Passive Components and Connector and other Components**
- JEITA IBIS Model HP
- Discussion about Case study of Simulation for Digital Consumer Electronics and **JEITA-IBIS Joint meeting include European IBIS member periodically**

3. Study of Interconnect Model

SI Model (Connector, PCB, Cable)



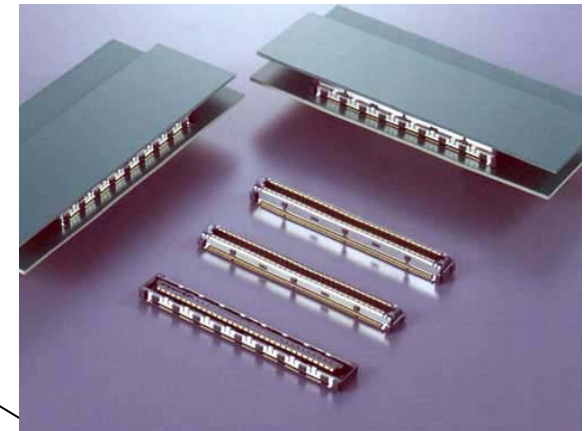
JAE (Japan Aviation
Electronics Industry)
FI-X Series

Study of Interconnect Model for Signal Integrity

- ◆ **Target Application; DDR, PCI-Express etc.**
- ◆ **EDA Model; Connectors,
Passive Components,
PCB (Via, Pattern),
(LSI)**
- ◆ **Simulation Tool; Cadence etc.**

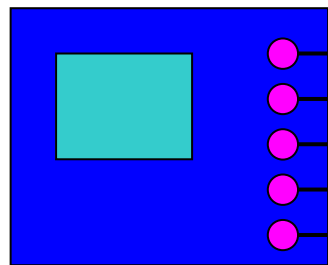
SI Model (Connector- Type B; stacked module, PCB, Cable)

Signal
PCI-Express
HyperTransport

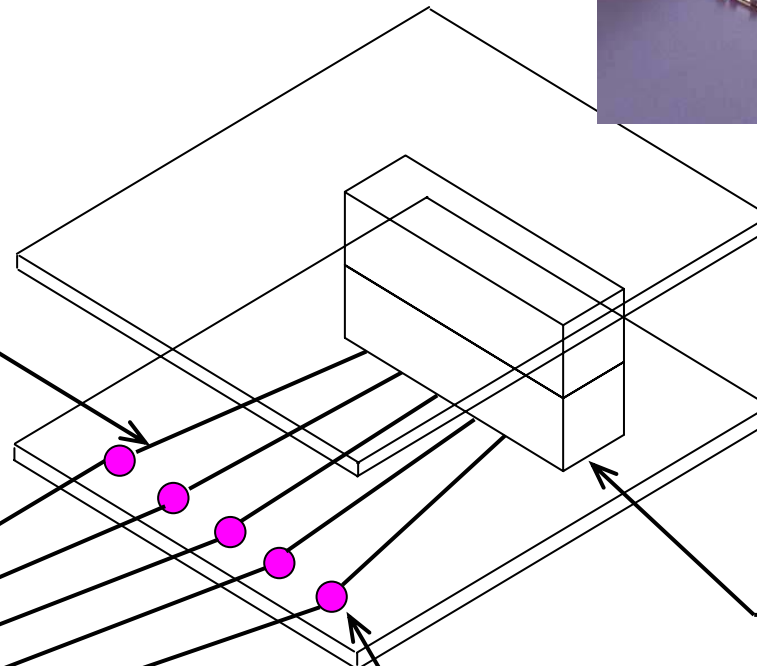


WB3 Series

Waveform measurement point



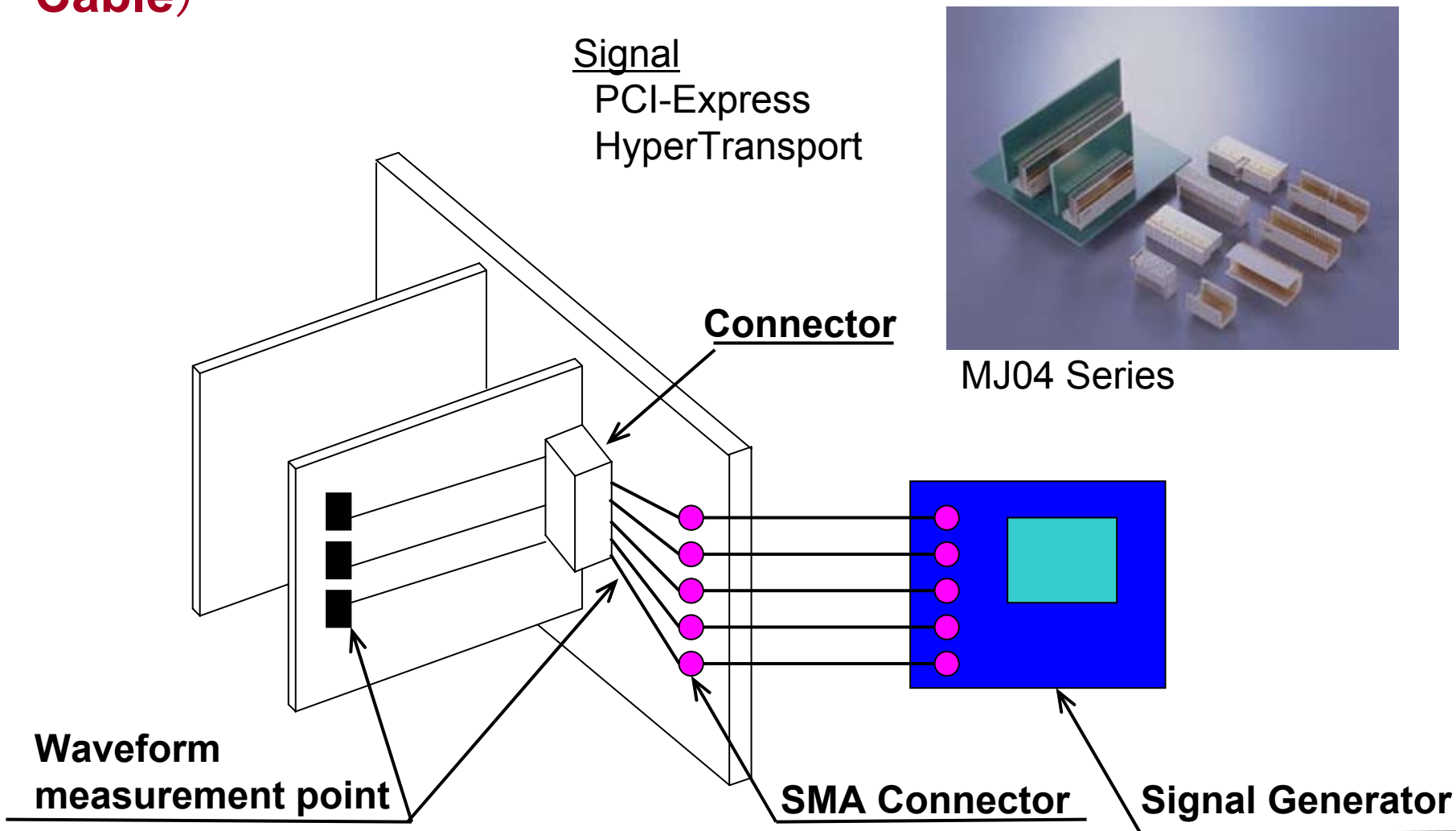
Signal Generator



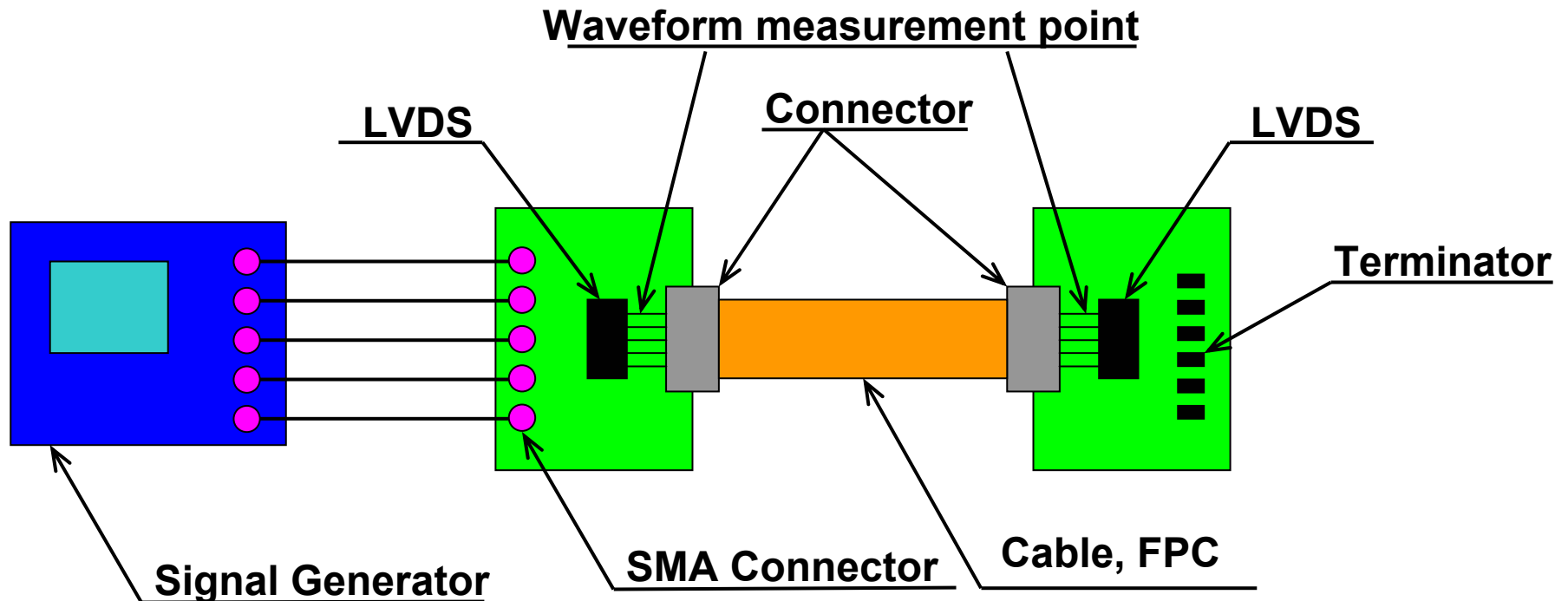
Connector

SMA Connector

SI Model (Connector- Type C, PCB, Cable)

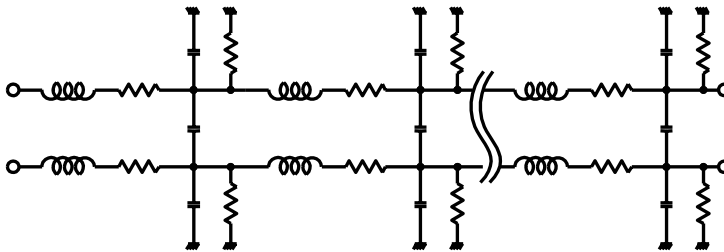


SI Model (Connector, PCB, Cable, LVDS)

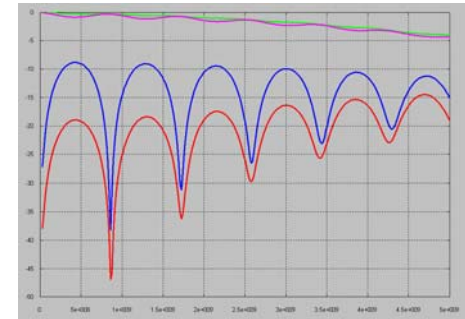


Simulation Model

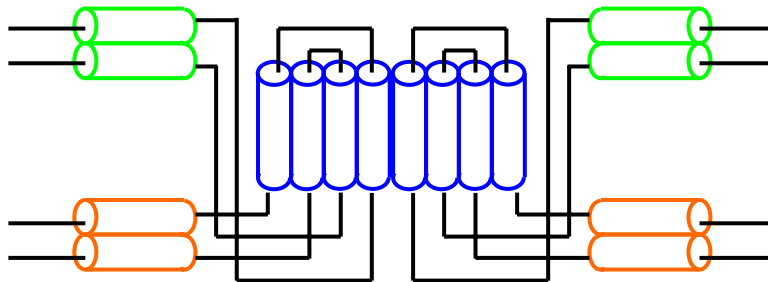
Equivalent circuit



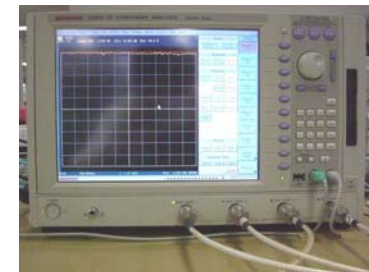
Simulation



TML

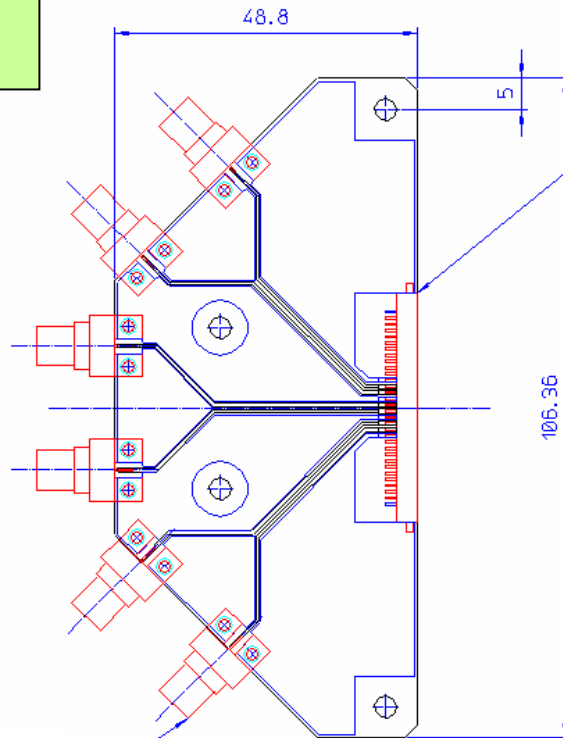


Measurement



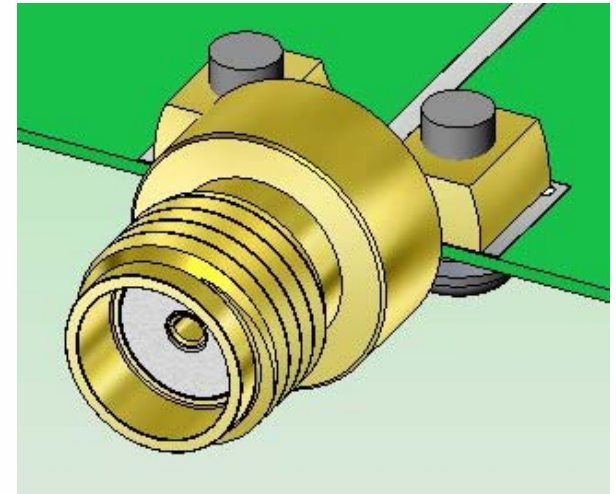
Evaluation Board

Connector

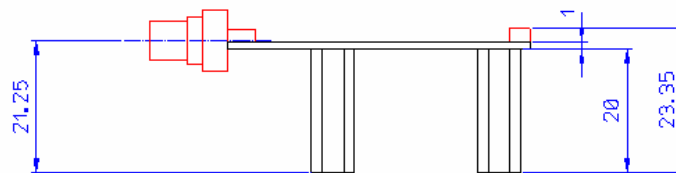


Fi-X Connector

SMA Connector
SMAR006D00

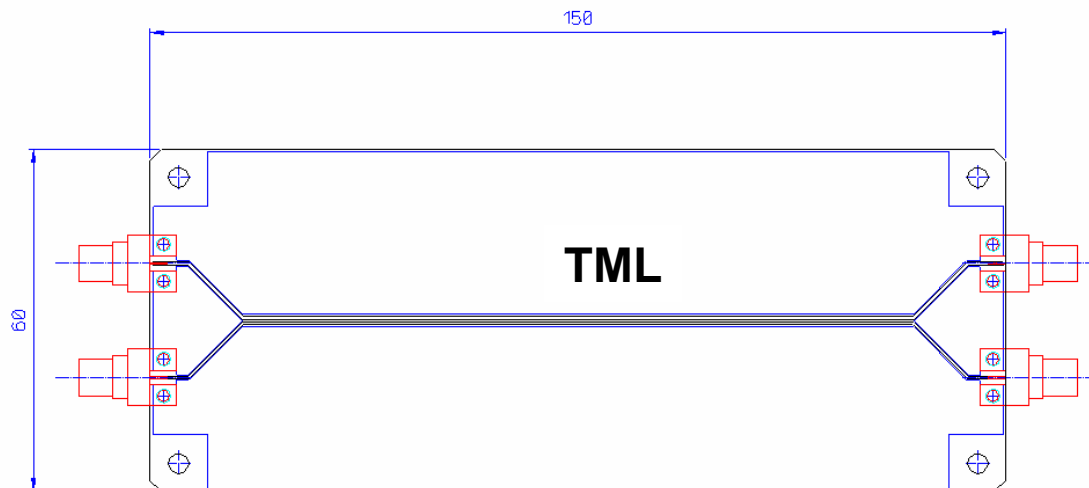


SMA Connector

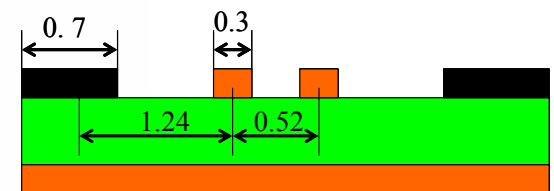
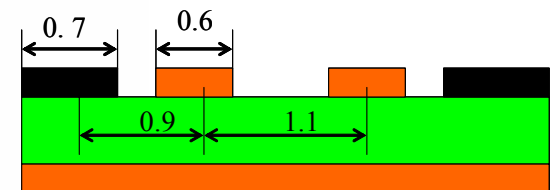
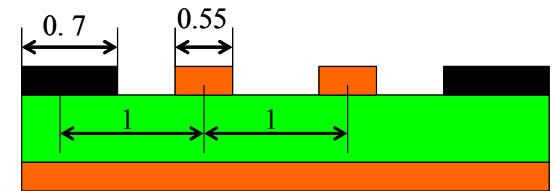


spacer

TML



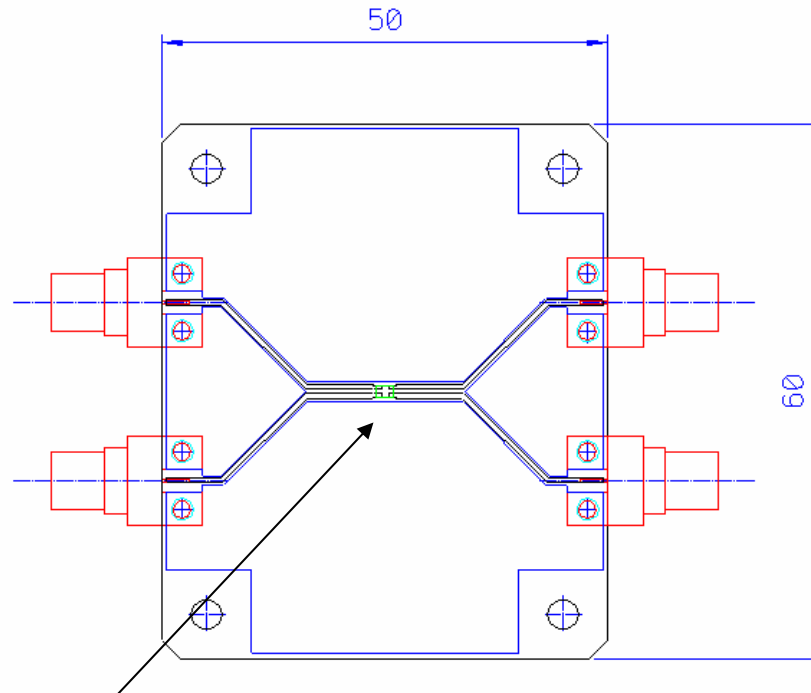
layer structure



SMA Connector



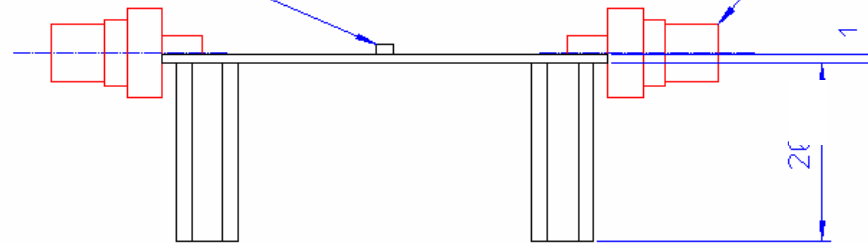
Passive Components



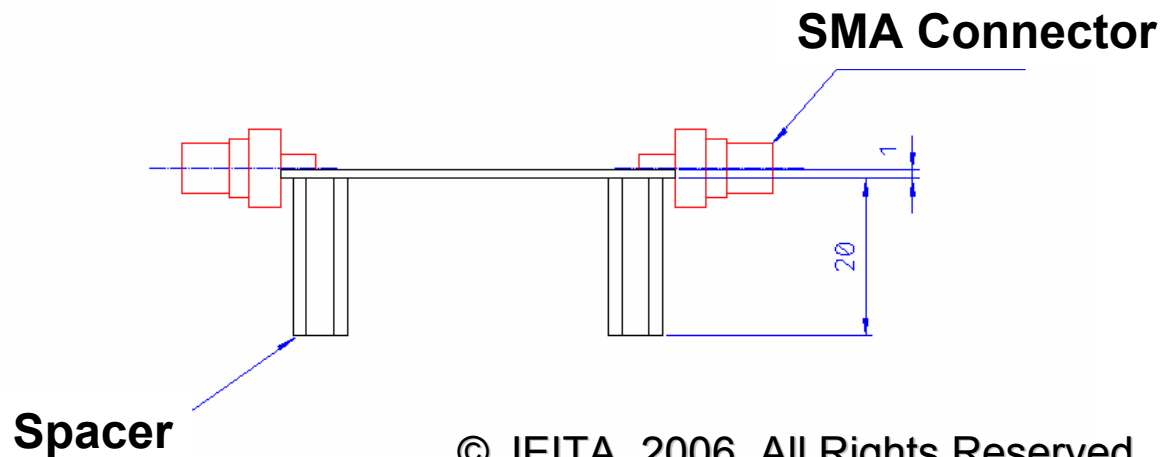
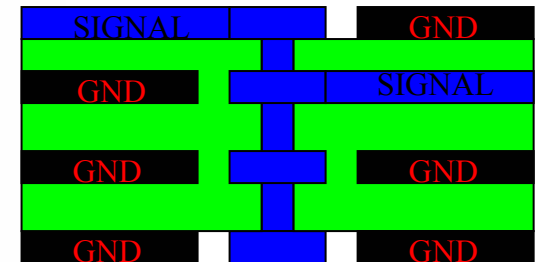
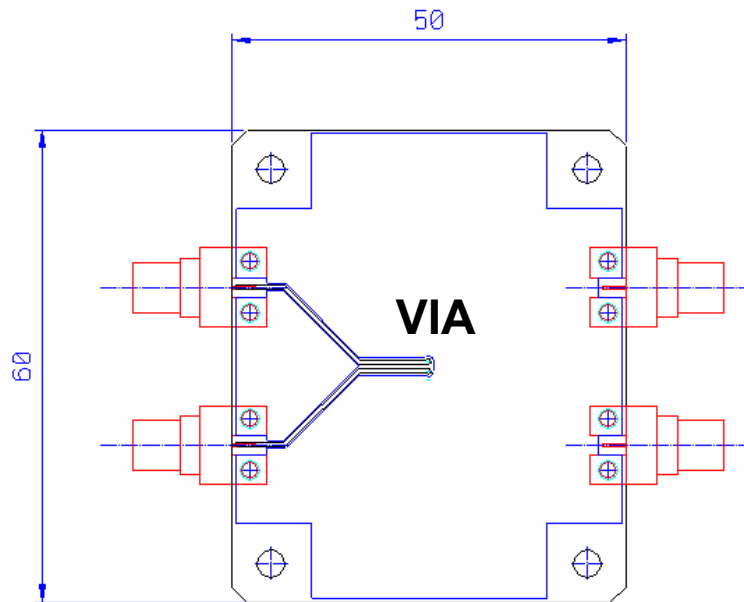
Passive Components

SMA Connector

Spacer

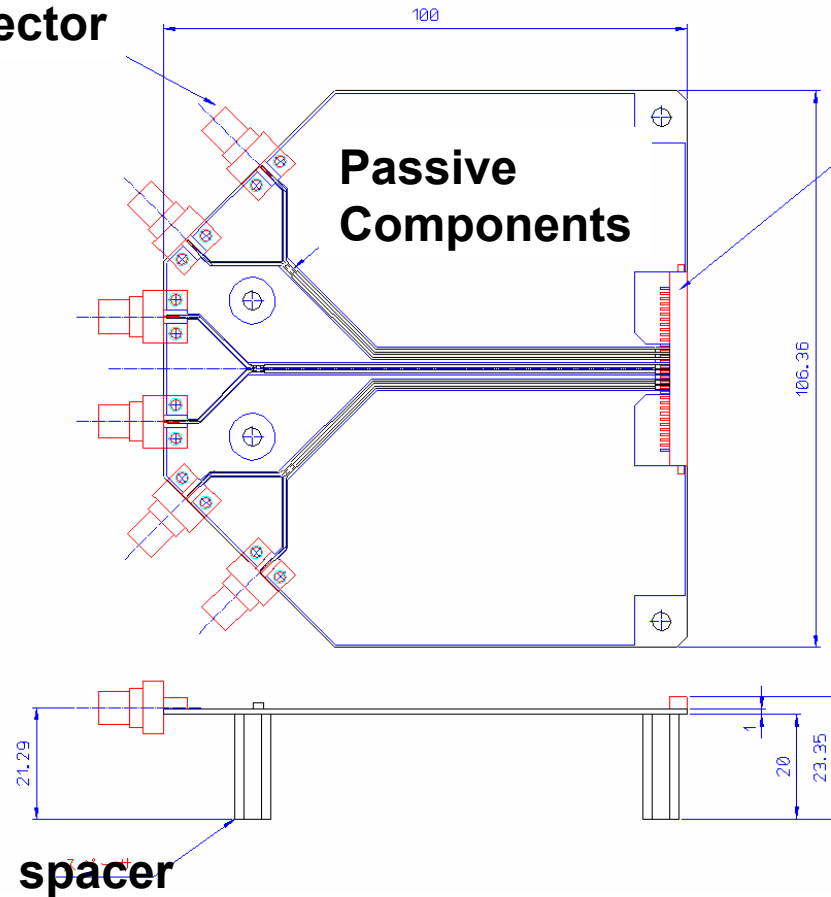


VIA



All Component (TML, Passive Components, VIA, Connector)

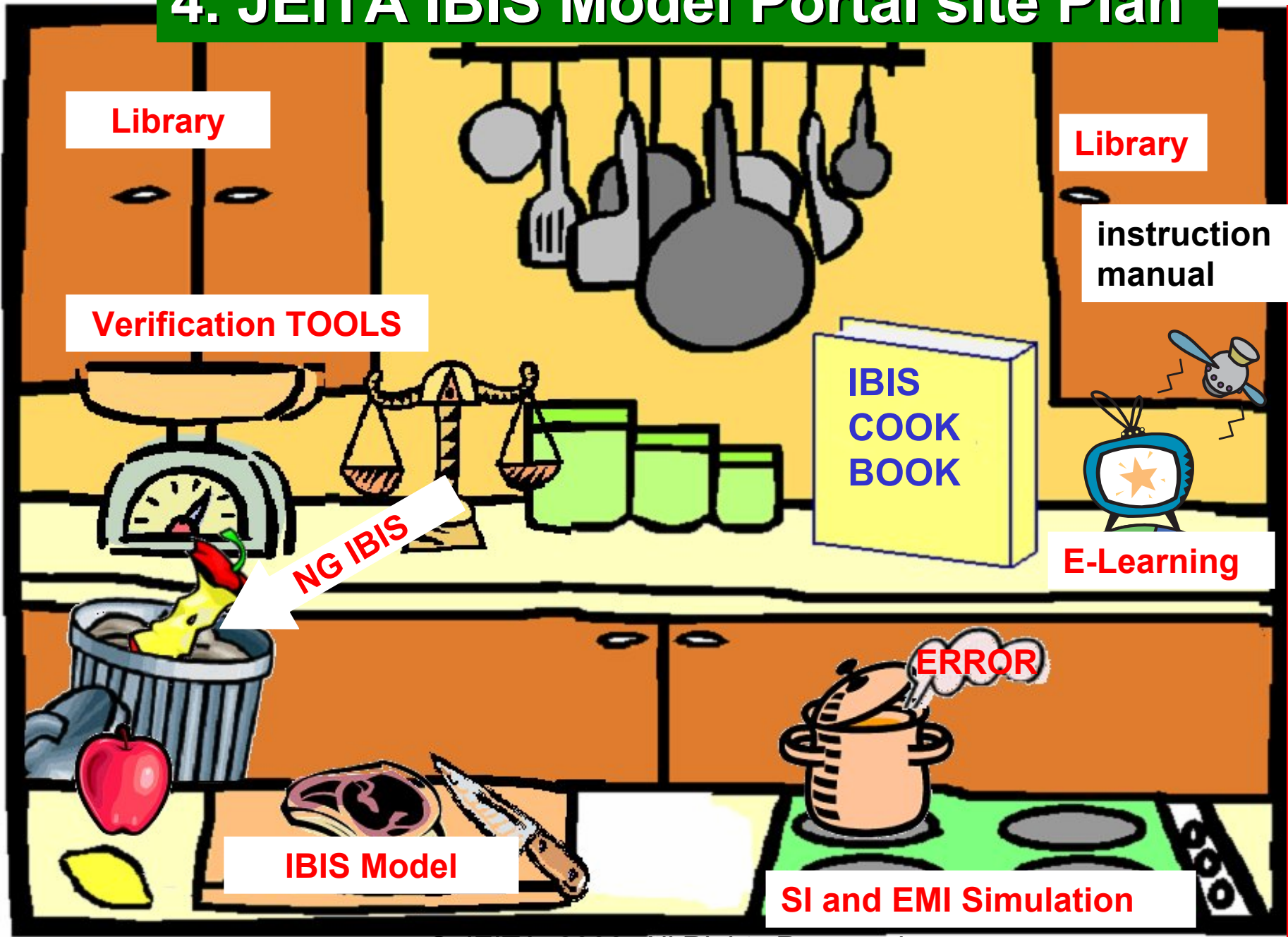
SMA Connector



Fi-X Connector

spacer

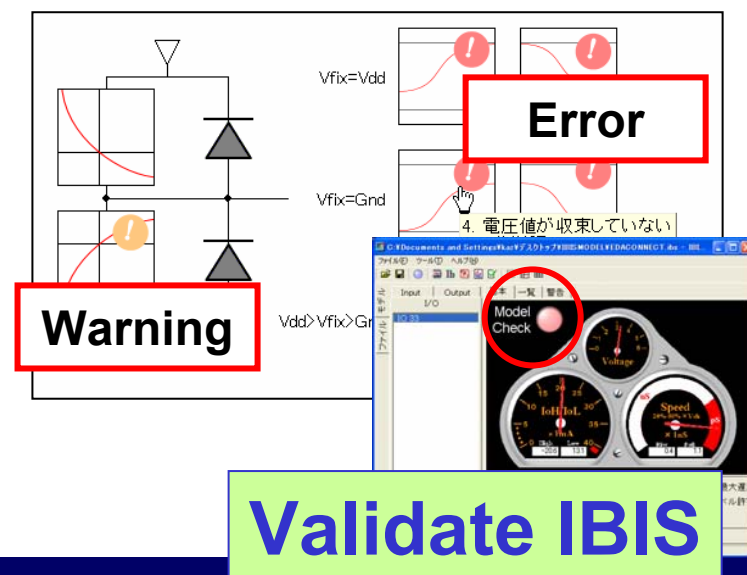
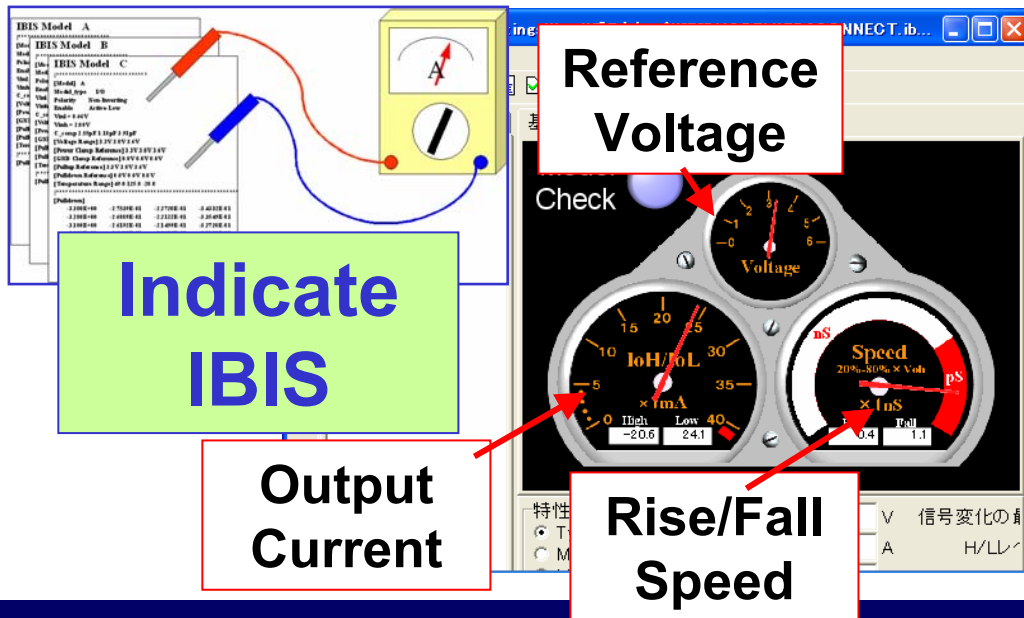
4. JEITA IBIS Model Portal site Plan



JEITA IBIS Model Portal Site Contents

- **IBIS Documentations**
COOK BOOK
- **IBIS Library**
Instruction manual
IBIS Model Storage rack
- **IBIS Training / IBIS E-Learning**
- **IBIS Free Tool**

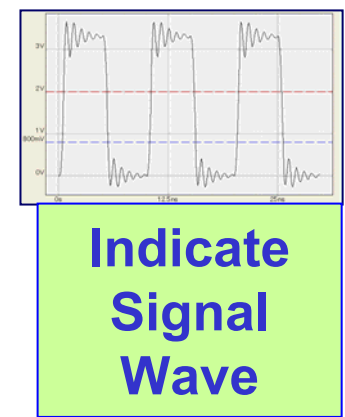
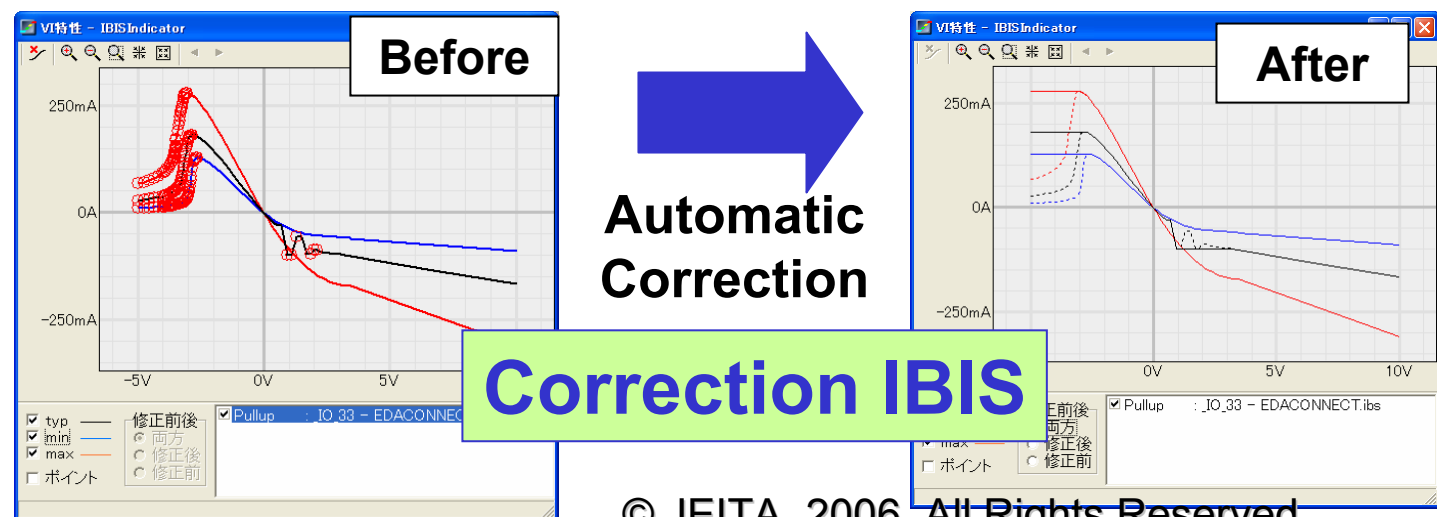
Support for IBIS Users



IBISIndicator™

The IBIS Model Engineering Stationery

By KAW/JAPAN www.kaw.co.jp



5. JEITA EDA-WG Progress Report

- **Study of Interconnect Model**
- **IBIS Documentations**
- **IBIS Free Tool**

~March of 2006

2006

Studying in progress

Study of Interconnect Model
for Signal Integrity

Evaluation for using different kind of model.

Which model might be better to practical use
for every simulation engineer.



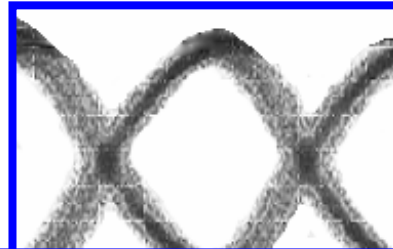
S-parameter?

Spice?

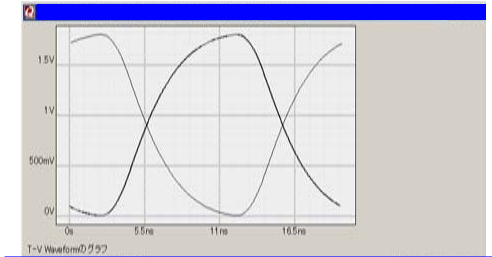
RLGC?

?

Compare Measurement with Simulation

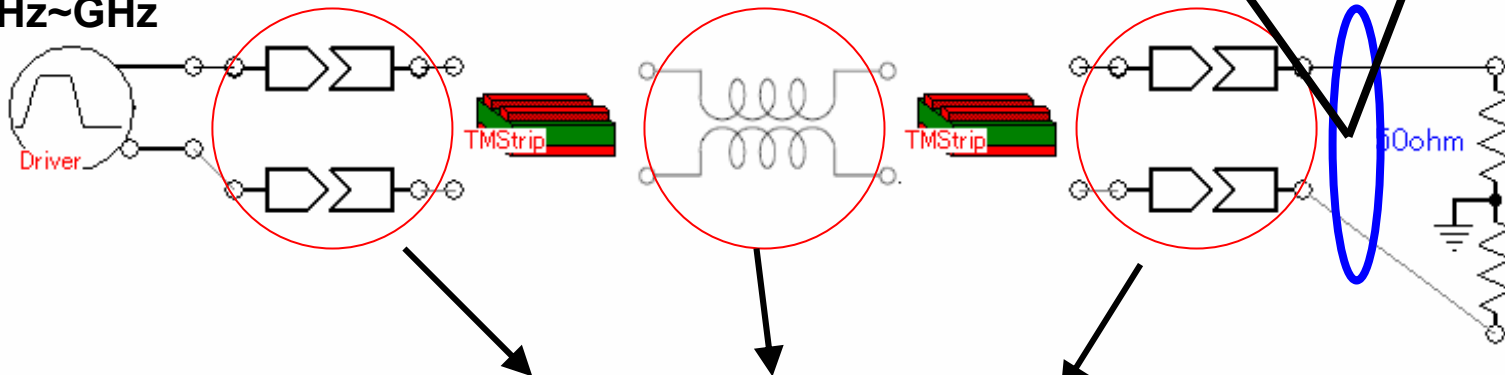


Measurement



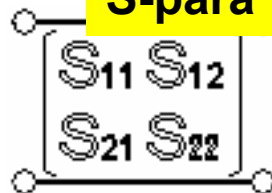
Simulation

MHz~GHz



Model

S-para



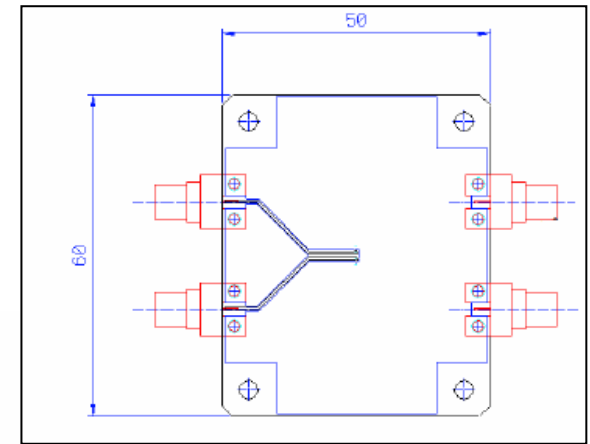
Spice



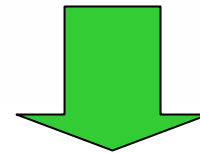
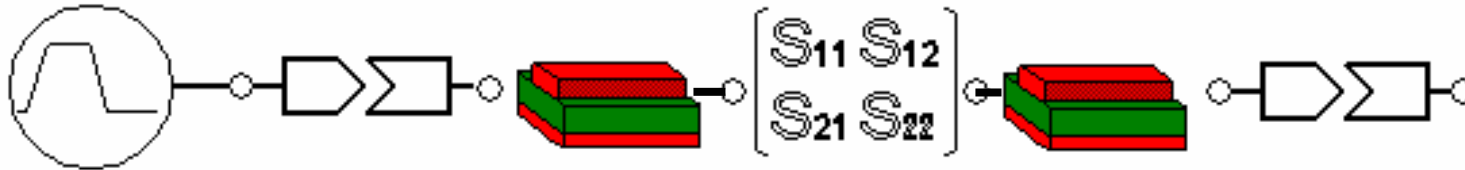
RLGC

$\Omega/H/S/F$

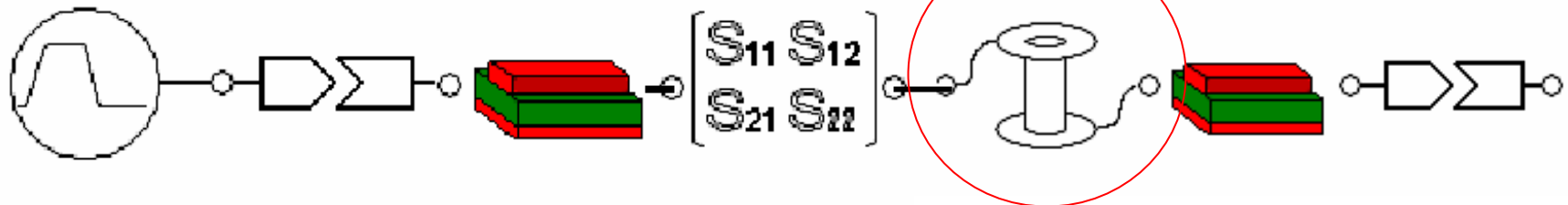
Testing the VIA effect



MHz~GHz



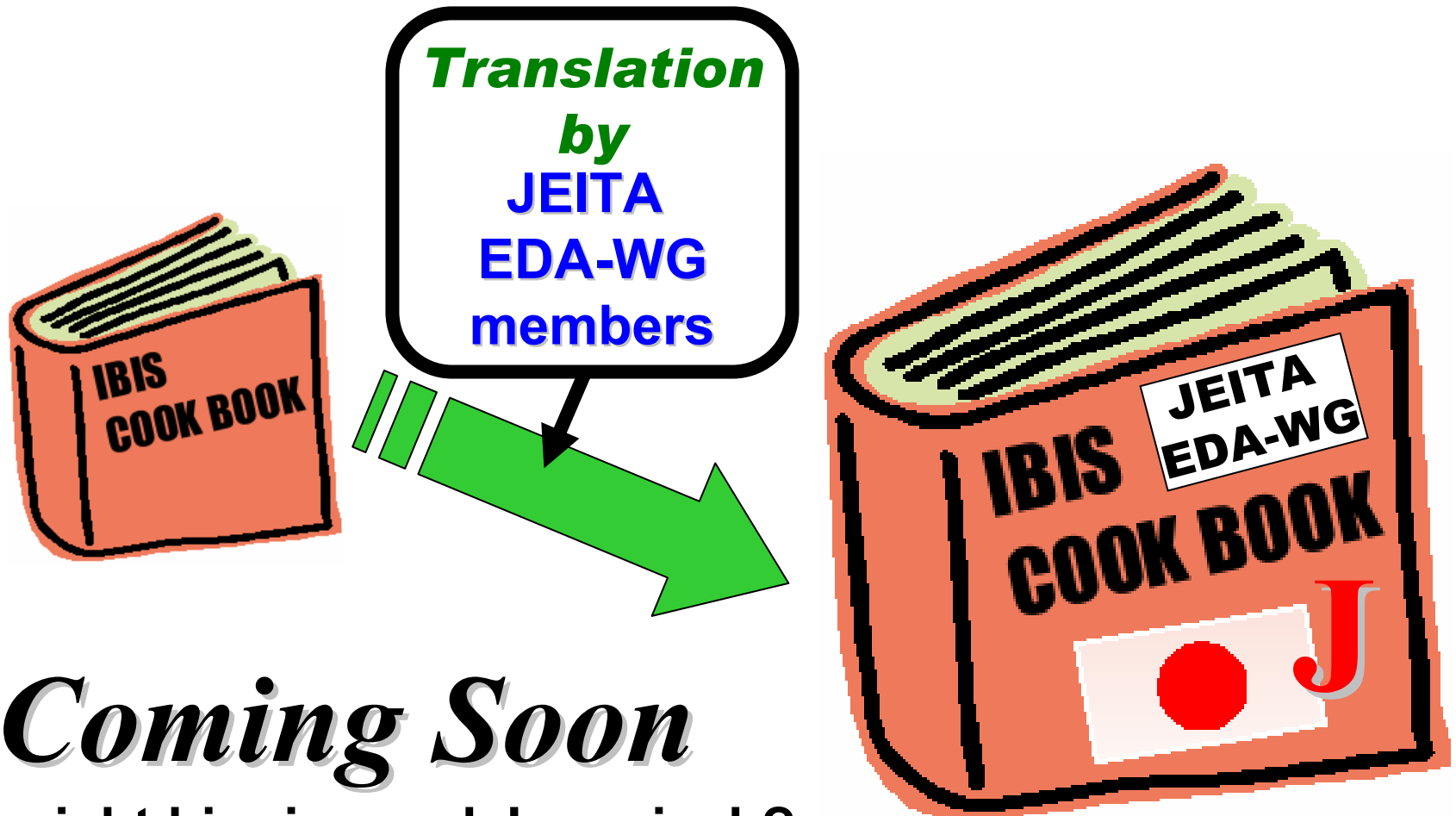
MHz~GHz



And more

IBIS Documentations

IBIS Cook Book in Japanese



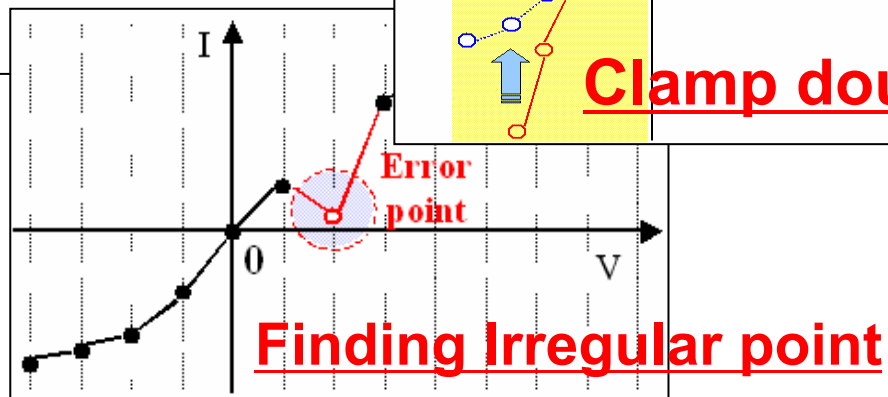
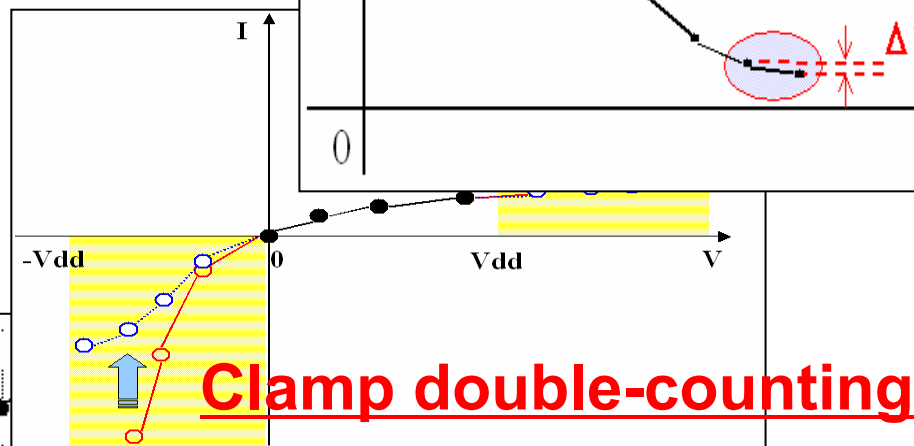
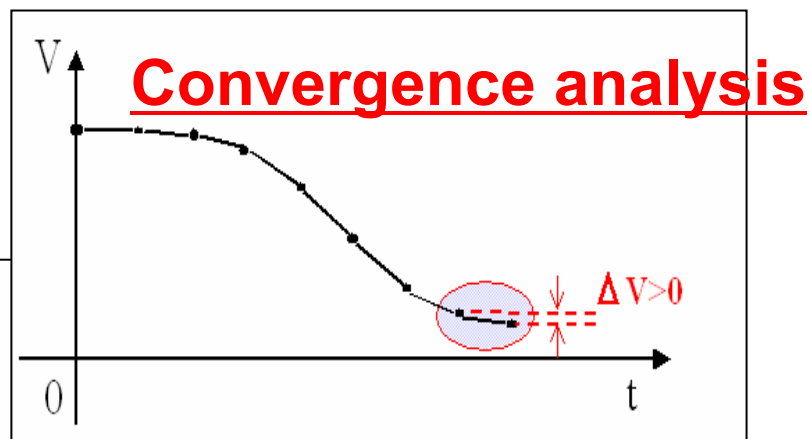
Coming Soon

Spricht hier jemand Japanisch?

IBIS Free Tool

Based on
IBISIndicator™

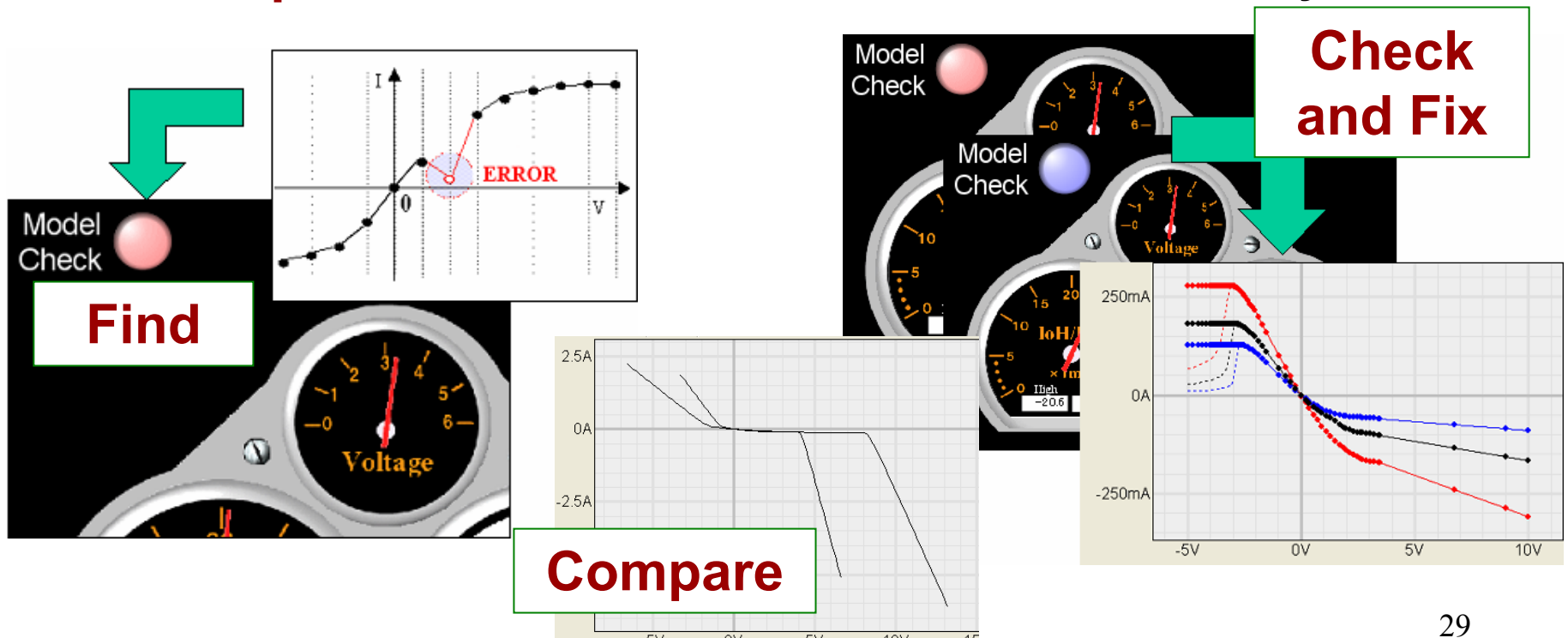
The Tool for
Supporting IBIS Users



20 Check Items

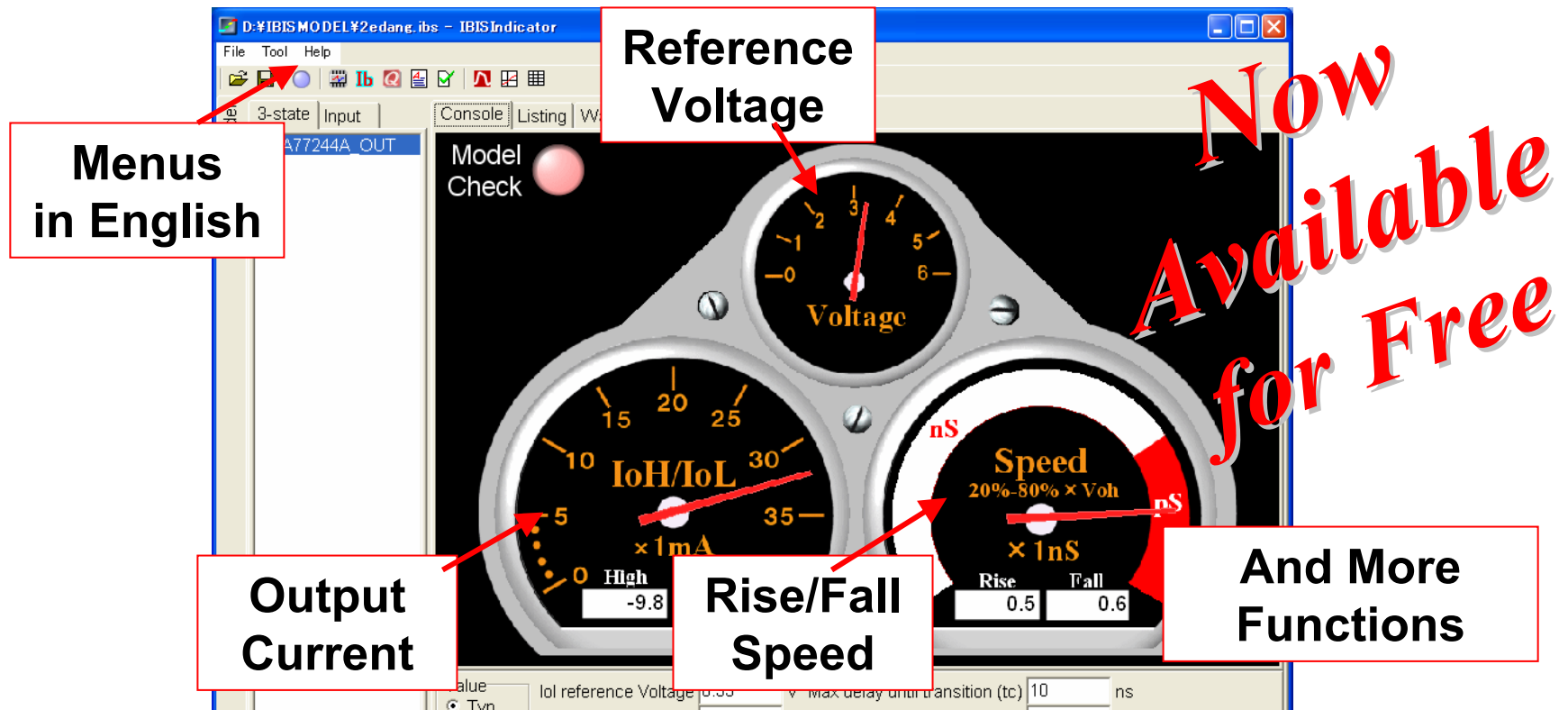
With the exception of Syntax

- Compare Check IBIS which are same Output current in the data sheets.
- Check and Auto-fix for IBIS Non-monotonic error.
- Find the problems of IBIS which has no-error in IBIS Syntax check.



IBIS Free Tool

IBISIndicatorTM The IBIS Model Limited Edition Engineering Stationery



Down Load: www.edaconnect.co.jp

JEITA IBIS Model Portal site in Progress

Library

Library

instruction
manual

Verification TOOLS



NG IBIS



E-Learning

ERROR

IBIS Model

SI and EMI Simulation

**We hope to discuss case
study of IBIS with European
IBIS members periodically**

**Thank you for all the help
EIA/IBIS Committee!**

Auf Wiedersehen!