HDL and IBIS 4.1 Models in a Functional DDR Memory Interface Analysis

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Simon Vines
simon_vines@mentor.com

UK Applications Group
Newbury

Mentor Graphics®

Project Definition

- ***Analyze a complete DDR memory interface in one simulation***
- ***Simulation should consider:***
  - ***Overshoot/Undershoot violations***
  - ***Setup and hold timing violations***
  - ***Include pattern dependant crosstalk between address, command, control, and data signals***
  - ***Slew dependant timing calculations***

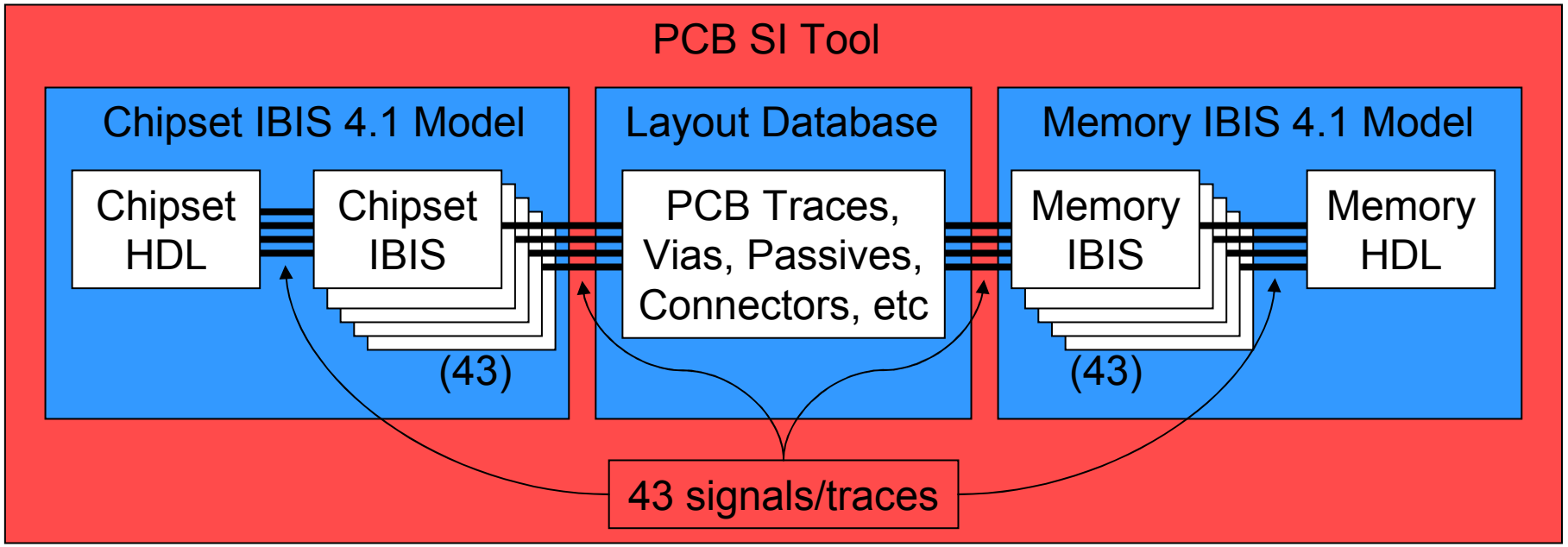
Project Approach

- *Combine HDL functional models and IBIS I/O models*
- *HDL code takes care of timing checks*
- *IBIS model contains basic electrical checks*
- *How does it all work?*

IBIS 4.1!

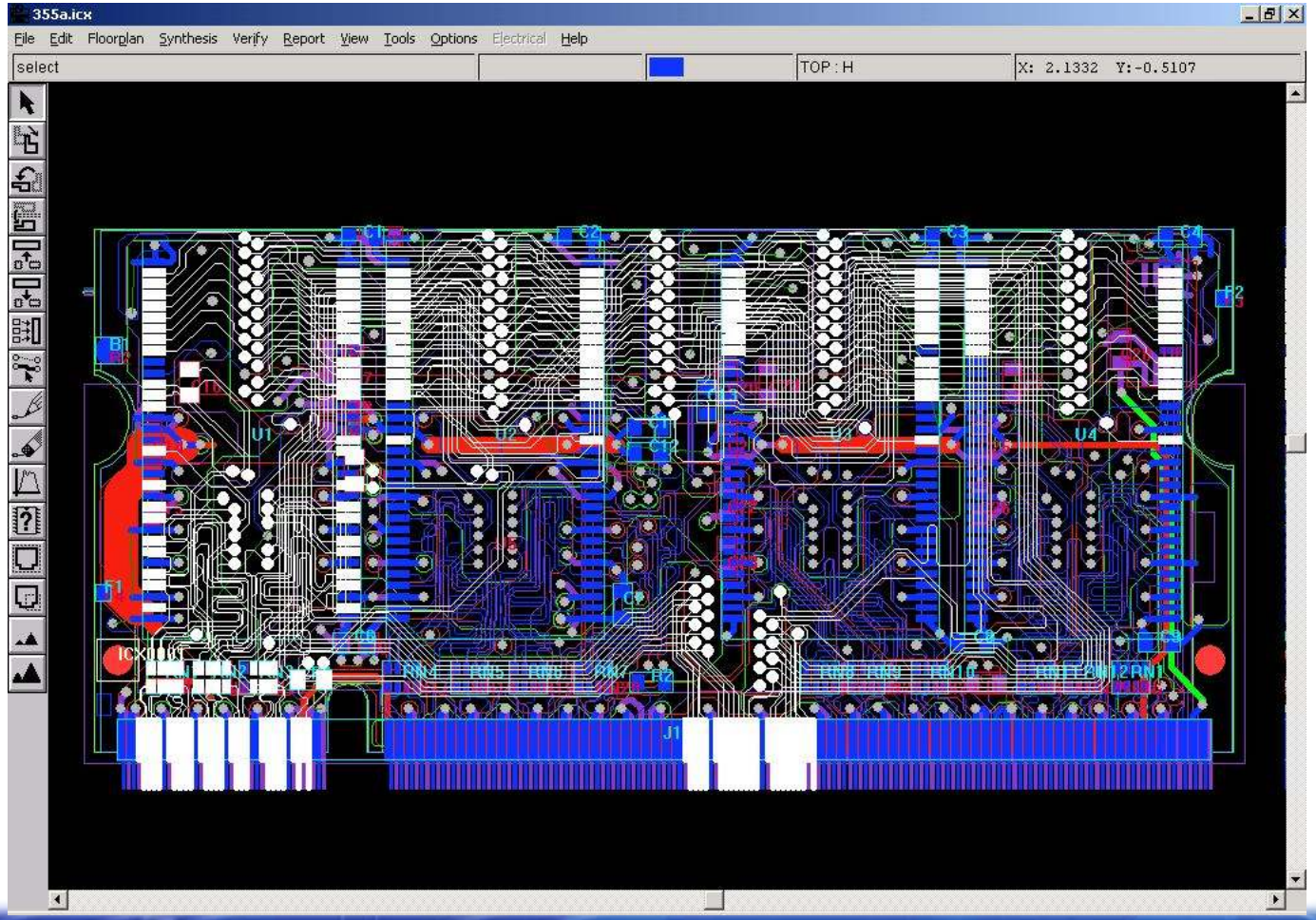
Simulation Diagram

- ***Connection of HDL functional models and IBIS I/O models to the physical board layout***



Analysis Details

- ***Memory module (simulated traces highlighted in white)***

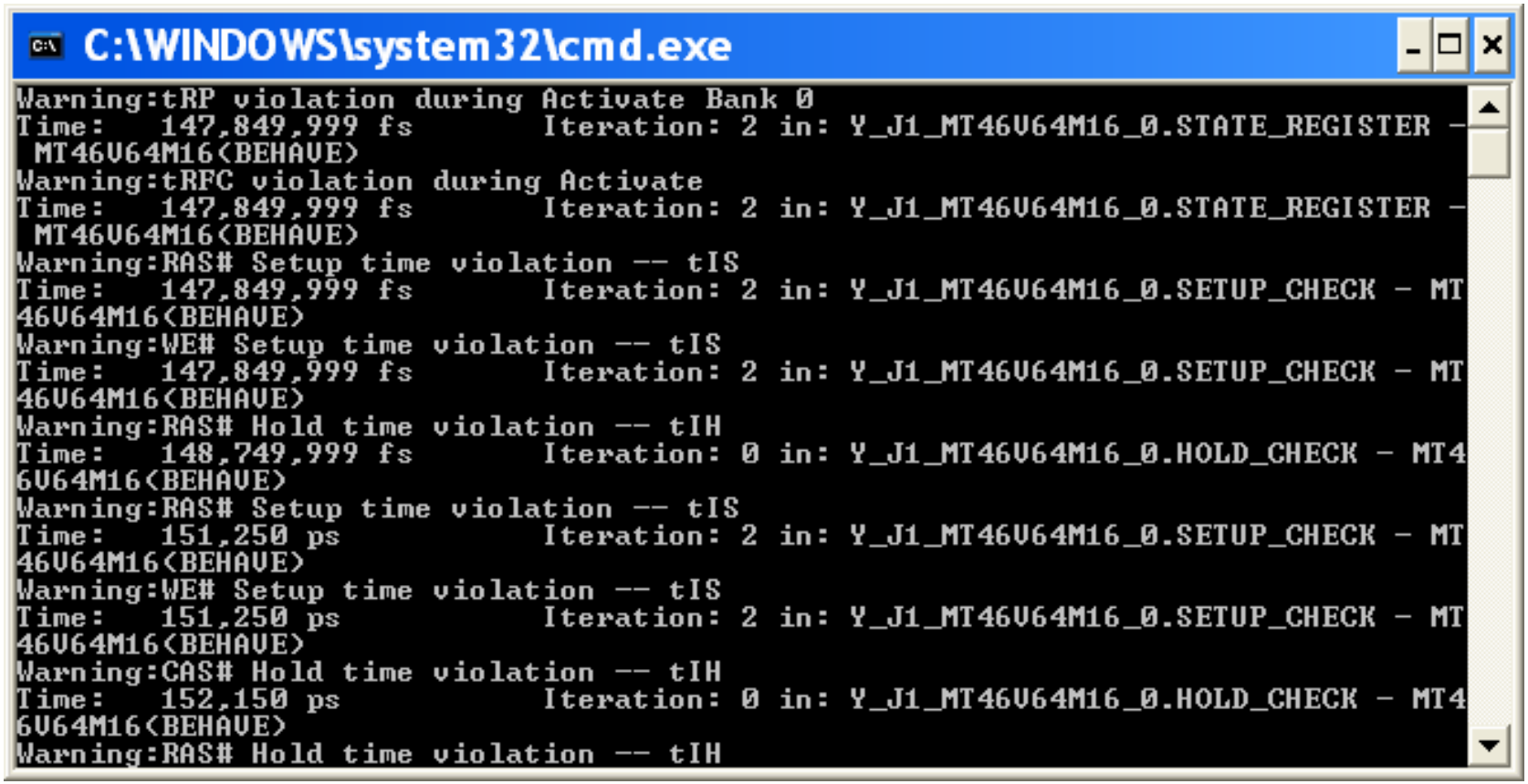


Analysis Details

- ***Digital code from the chipset testbench generates the system stimulus***
- ***Random address and data pattern generators ensure realistic stimulus patterns for the Write cycle***
- ***Memory responds to chipset commands, thus automating Read cycle data patterns***
- ***Single simulation completes a Read and Write Cycle – multiple cycles can be run to simulate realistic bus utilization***

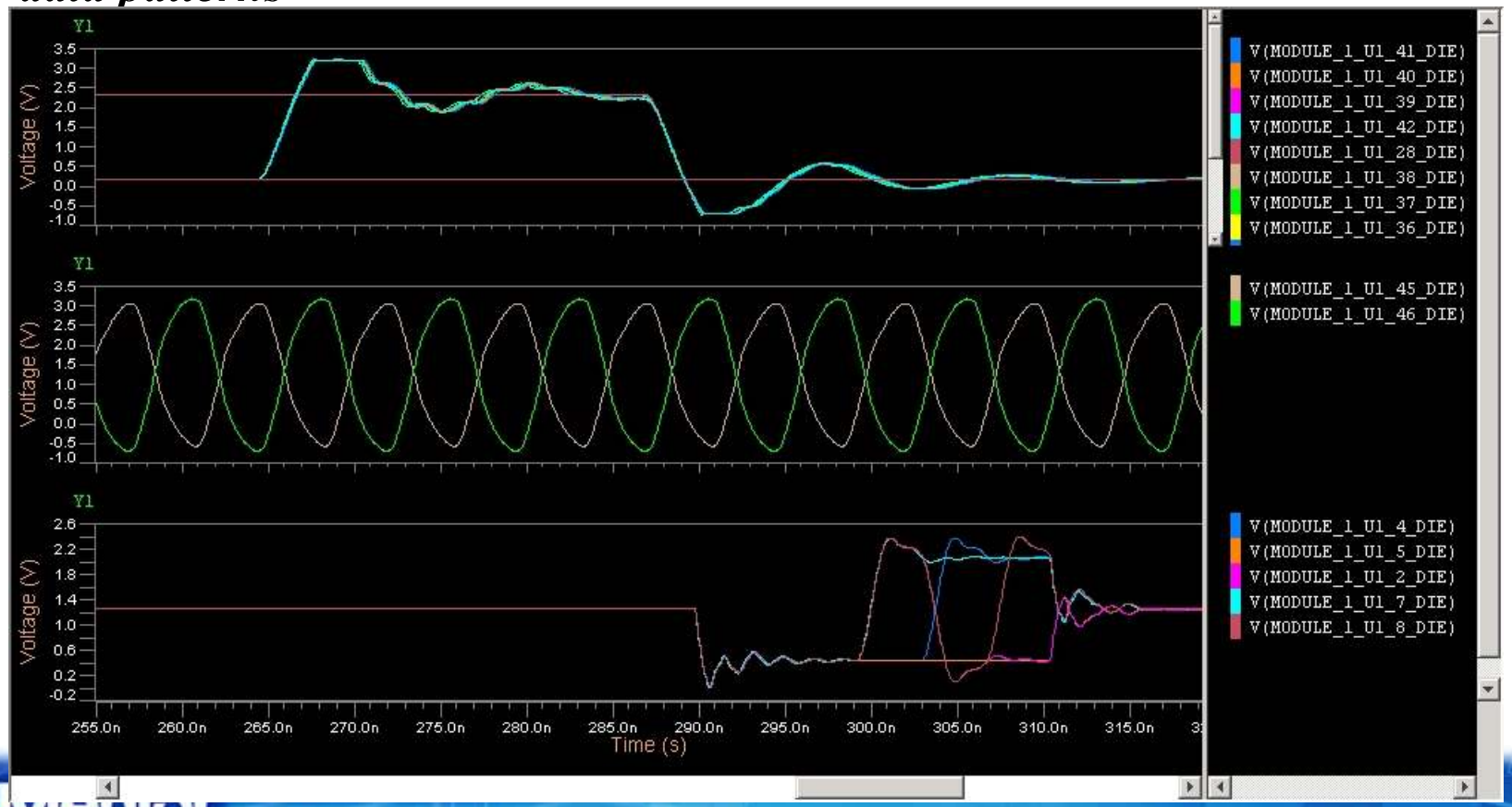
Functional SI Verification Results

- *HDL models contain timing checks*
- *Timing violations caused by PCB effects are flagged*



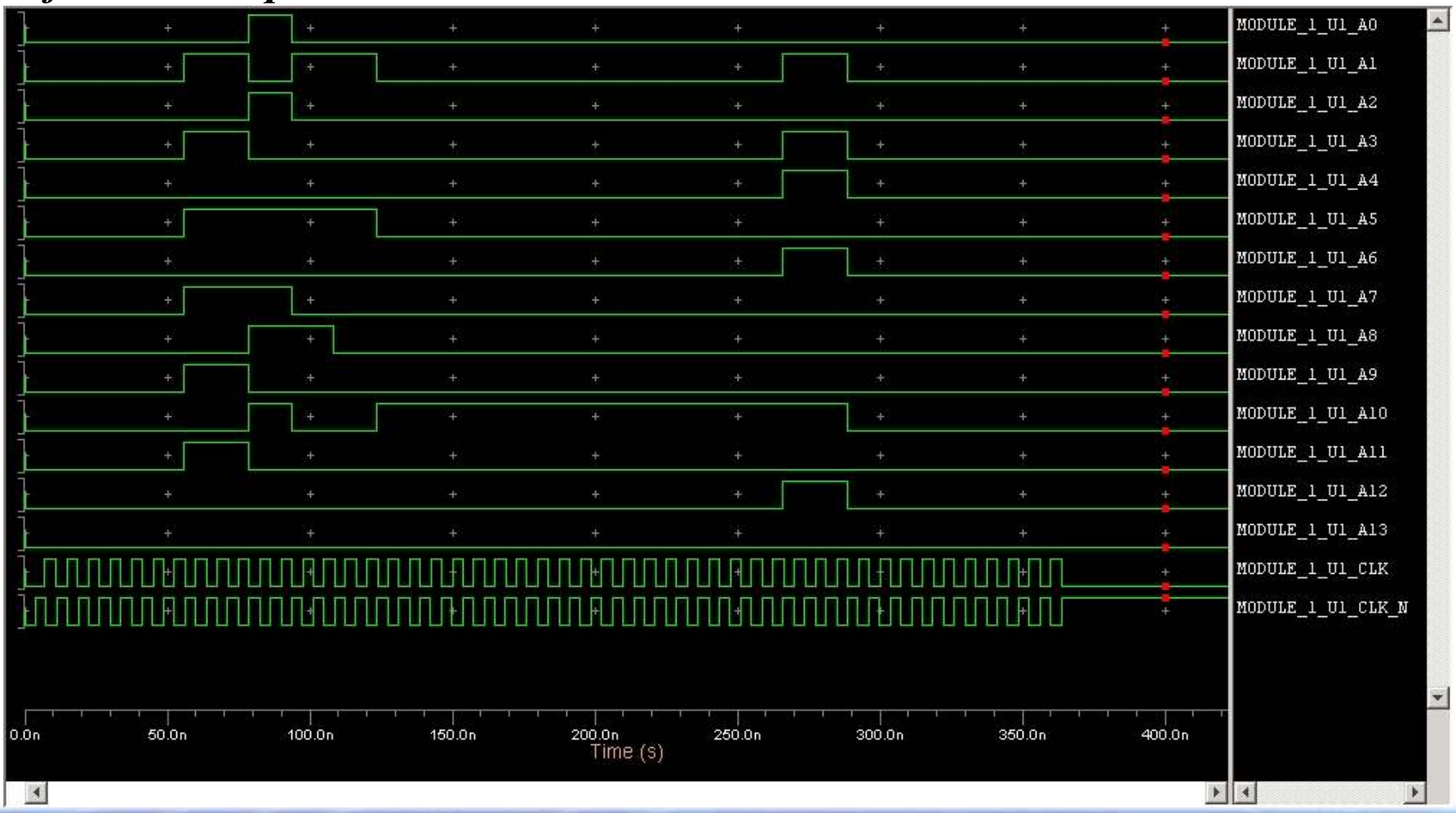
Functional SI Verification Results

- *Analog Address, Clock, and Data signals at memory during a burst write from the chipset*
- *Simulation easily changed to generate pseudo-random or fixed address and data patterns*



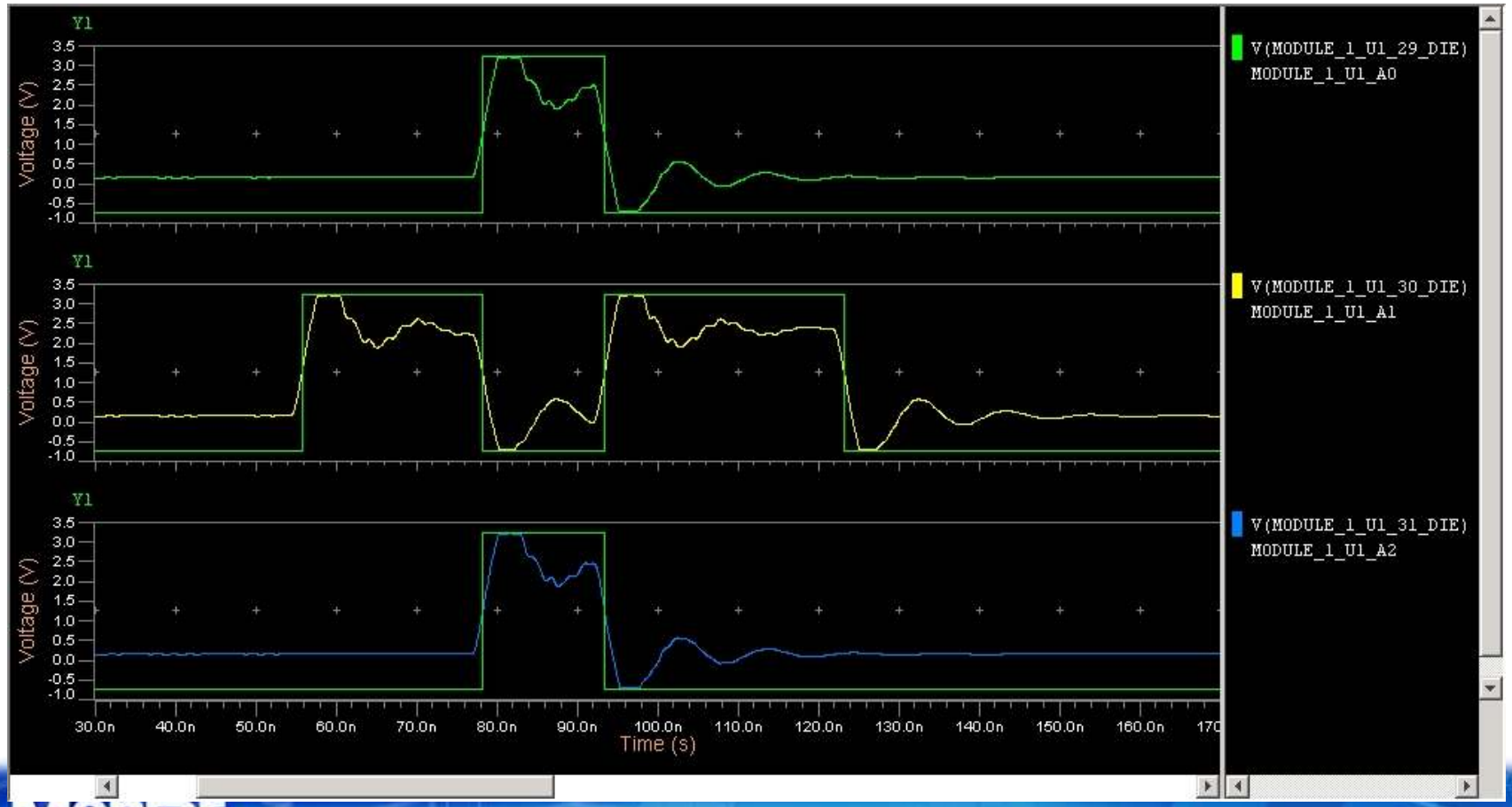
Functional SI Verification Results

- ***Digital Address and Clock signals at the memory die during a burst write from the chipset***



Functional SI Verification Results

- ***Combined analog and digital Address signals at the memory die during a burst write from the chipset***
- ***Provides a useful visualization of the logical analog equivalent***



Future Enhancements

- ***Exercise all 64 DQ signals in the system (instead of 16)***
- ***Use AMS to analyze slew dependant timing – outputting results on separate signal***
- ***Model DDR2 system including ODT effects***
- ***Include S-parameter models to replace PCB physical information for enhanced crosstalk analysis***
- ***IBIS enhancements:***
  - ***Instantiating a [Model] in a [Circuit Call] statement***
  - ***Corner-specific Parameters passing***

Each instance of an [External Circuit] is referenced by one or more [Circuit Call] keywords discussed later. ~~(The [Circuit Call] keyword cannot be used to reference a [Model] keyword.)~~

Project Contributors

- *Gary Pratt, Mentor Graphics*
- *Mark Kniep, Micron Technology*
- *Pavani Jella, Micron Technology*
- *Randy Wolff, Micron Technology*

- *Paper Reference:*
  - *Functional SI simulation using IBIS 4.1 and HDL models*
    - *Pratt, Kniep, Jella, Wolff, 2006*

Summary

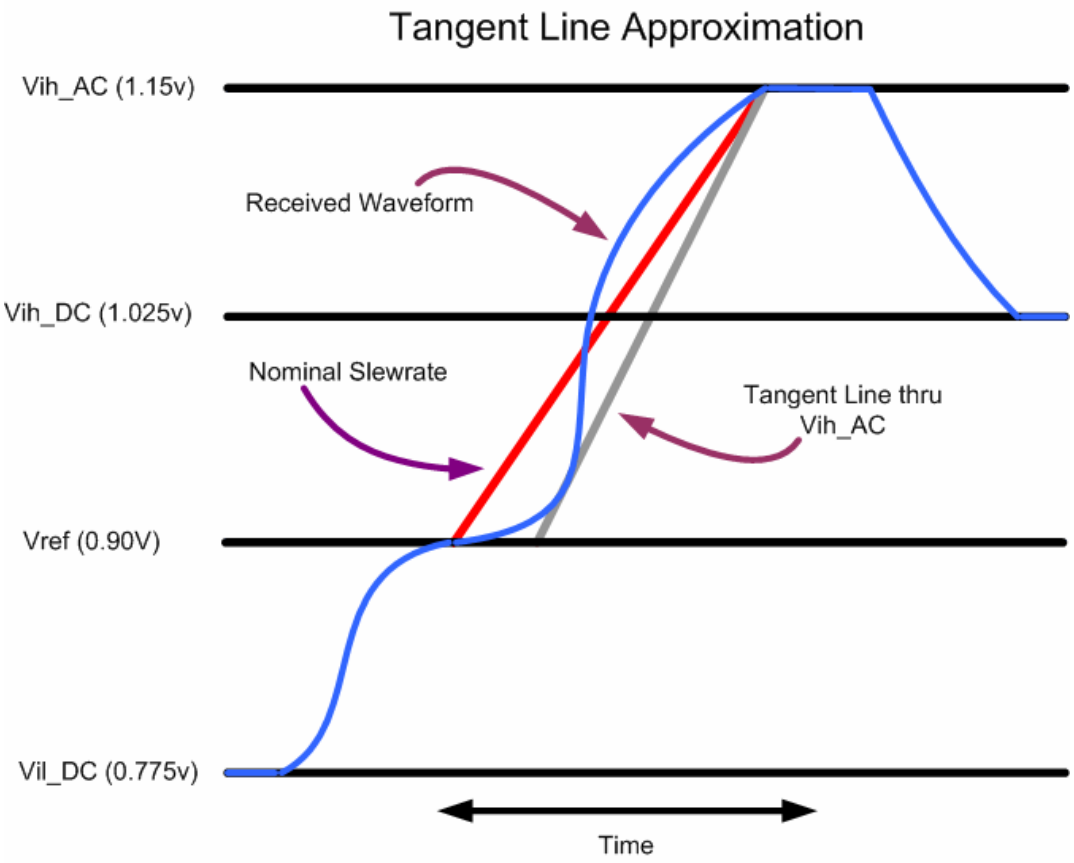
- *IBIS 4.1/AMS*
  - *Clear Choice for SERDES SI Analysis*
  - *Clear Choice for the Future of SI Analysis*
  - *Extremely User Friendly*
  - *Fast and Accurate*
  - *Uses Limited Only by the Imagination*

- *Next Step*
  - *Silicon Vendors*
    - *Contact Gary Pratt for help getting started with IBIS/AMS*
      - *Gary_Pratt@mentor.com*
  - *PCB Vendors*
    - *Contact Gary Pratt to work with your vendor*

Breaking News…

- ***DDR2 Measurements***
  - ***Automatic Derating measurements***
    - ***Calculates slope***
    - ***Uses Derating look-up table***

DDR2 Derating



VHDL-AMS Code

```
process
   type data_point_type is array (0 to max_points) of real;
   variable data_point_v : data_point_type;
   variable data_point_t : data_point_type;
   variable data_point_cntr: integer;
   variable slope, max_slope : real;

begin  -- measure the rising setup time slew rate
   max_slope := 0.0; data_point_cntr := 0;
   -- wait for positive crossing of vref
   wait until vref_cross;
   -- store all the data points until vih_ac crossing
   while not vih_ac_cross loop -- loop until vih_ac crossing
      data_point_v(data_point_cntr) := v_a_signal; --store voltagae
      data_point_t(data_point_cntr) := now;        --store time
      assert data_point_cntr < max_points-1 -- check for pointer overflow
         REPORT "transistion exceeded max_transistion_time" SEVERITY ERROR;
      data_point_cntr := data_point_cntr + 1;  -- increment pointer
      wait on analog_solution_point; -- wait for the next time step
   end loop;
   -- determine the maximum slope
   for i in 0 to data_point_cntr-1 loop  -- loop through points, find slope
      slope := (v_a_signal - data_point_v(i)) / (now - data_point_t(i));
      if slope > max_slope then max_slope := slope; end if;
   end loop;
   --Apply this slope to the LUT, to determine Setup time requirement
   rising_tds_slope_sig <= max_slope*1.0e-9;  -- for now, just display the slope

   -- measure the falling hold time slew rate
   ...
```

WARNING

The Slides you are about to see are intended for model developers only!

The purpose of this application is to provide a thorough, easy-to-use memory interface verification. Once developed, these models are as easy to use as any other IBIS models.

End Users: Close your eyes now …

IBIS File (screen 1)

Typical IBIS Header

```
|*****************************************************************************
| mt46v64m16.ibs * IBIS 4.1 Model
| 1Gb DDR SDRAM - Die Revision "A"
|
| Part Number       VDD/VDDQ          Architecture        Package
| MT46V64M16TG      2.5V/2.5V          64M x 16           66-pin TSOP
|*****************************************************************************
|
[IBIS Ver]     4.1
[File name]    mt46v64m16.ibs
[File Rev]     2.3
[Date]         09/22/2005
[Source]       From silicon level SPICE model at Micron Technology, Inc.
                   Micron Technology, Inc.
                   8000 S. Federal Way
                   P.O. Box 6, M/S: 01-711
                   Boise, ID 83707-0006
|
[Notes]        Rev 1.0: 10/11/2002
                   - Initial file creation
               Rev 1.1: 12/05/2002
                   - Updated clamp characteristics
                   - Fixed x4 package pinout
               Rev 2.0: 6/10/2003
                   - Matched the I-V curves of the dq_full and dq_half models
                     to silicon measurements
                   - Updated the input capacitance of all models
               Rev 2.1: 12/18/2003
                   - Matched the I-V curves of the dq_full and dq_half models
                     to the most recent silicon measurements
                   - Added Vinl and Vinh corners to all models
                   - Added Vmeas corners to the dqbuff models
               Rev 2.2: 09/22/2005
                   - Matched to latest silicon measurements
                   - Added [Receiver Thresholds]
                   - Added Vref and Overshoot specs to [Model Spec] section
                   - Changed IBIS version to 4.0
```

IBIS File (screen 2)

Typical IBIS Pin List

```
|*****************************************************************************
|
[Component]     MT46V64M16TG_AMS
[Manufacturer]  Micron Technology, Inc.
|
[Package]   | TSOP package
|               typ              min              max
R_pkg           0.036            0.025            0.046
L_pkg           4.35nH           2.73nH           5.97nH
C_pkg           1.00pF           0.72pF           1.29pF
|
[Pin]    signal_name    model_name    R_pin      L_pin          C_pin
|
1        VDD            POWER         0.034      5.02nH         4.29pF  |POWER
2        DQ0            NC            0.043      5.22nH         1.26pF  |dqbuff
3        VDDQ           POWER         0.044      5.02nH         1.22pF  |POWER
4        DQ1            NC            0.042      5.53nH         1.19pF  |dqbuff
5        DQ2            NC            0.041      5.32nH         1.16pF  |dqbuff
6        VSSQ           GND           0.041      4.48nH         1.13pF  |GND
7        DQ3            NC            0.039      4.34nH         1.11pF  |dqbuff
8        DQ4            NC            0.037      4.13nH         1.07pF  |dqbuff
9        VDDQ           POWER         0.036      3.78nH         1.02pF  |POWER
10       DQ5            NC            0.035      3.31nH         1.01pF  |dqbuff
...
60       DQ12           NC            0.041      3.38nH         1.09pF  |dqbuff
61       VDDQ           POWER         0.043      4.18nH         1.13pF  |POWER
62       DQ13           NC            0.045      4.72nH         1.17pF  |dqbuff
63       DQ14           NC            0.046      4.96nH         1.20pF  |dqbuff
64       VSSQ           GND           0.045      5.28nH         1.23pF  |GND
65       DQ15           NC            0.043      5.61nH         1.27pF  |dqbuff
66       VSS            GND           0.034      4.77nH         4.59pF  |GND
|
|************************DIFF PIN*****************************************
[Diff_pin]     inv_pin     vdiff     tdelay_typ     tdelay_min     tdelay_max
|
    45           46          .360V      0ns              NA             NA
|
```

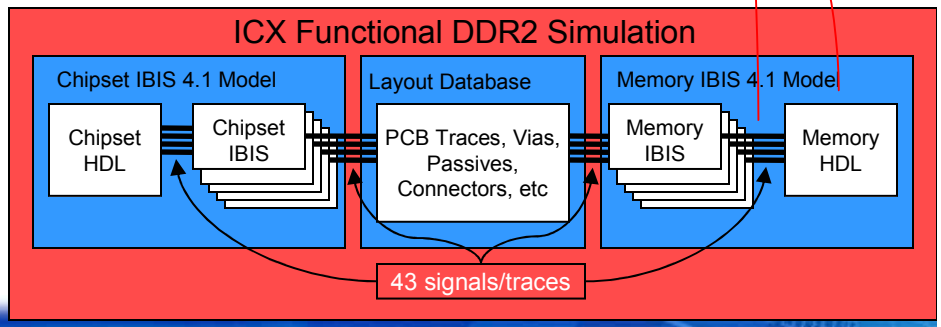
IBIS File

(screen 3)

New IBIS 4.1 Circuit Call

Memory HDL Model

```
|************************EXTERNAL MODELS*************************************
[node declarations]
| For the Memory:
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15
UDQS LDQS UDM LDM DQE A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13
BA0 BA1 RAS_N CAS_N WE_N CS_N CKE CLK CLK_N GND VDD TEST
[end node declarations]
|
|Instantiate the VHDL Model
[circuit call] MT46V64M16
|Port_map port pad/node
|Map DQ bits
Port_map DQ0   DQ0
Port_map DQ1   DQ1
Port_map DQ2   DQ2
...
|Start DQS, DM mapping
Port_map UDQS  UDQS
Port_map LDQS  LDQS
Port_map UDM   UDM
Port_map LDM   LDM
|Start Address/Command port mapping
Port_map A0    A0
Port_map A1    A1
Port_map A2    A2
Port_map A3    A3
Port_map A4    A4
...
|Start Control bit port mapping
Port_map CS_N  CS_N
Port_map CKE   CKE
|Map CLK Signals
Port_map CLK   CLK
Port_map CLK_N CLK_N
|Misc.
Port_map DQE   DQE
[end circuit call]
```



IBIS File

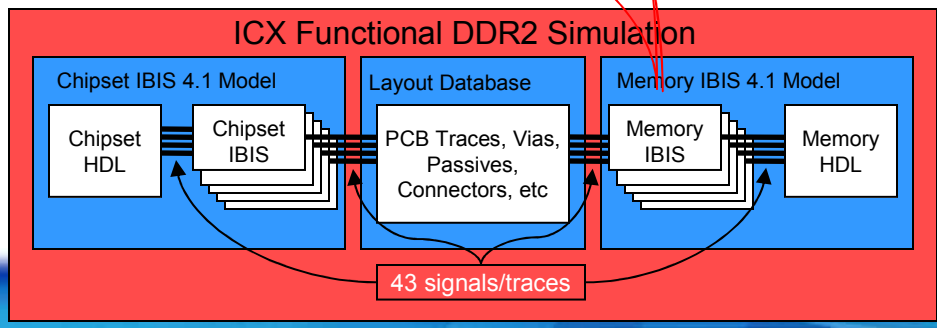
(screen 4)

New IBIS 4.1 Circuit Calls

Instances of traditional IBIS table models

```
|
| IBIS Model Instantiation (Needed for each individual signal)
|Port_map port pad/node
[circuit call]          clk_input
Port_map A_signal       45
Port_map D_receive      CLK
Port_map A_gnd          GND
Port_map A_gcref        GND
Port_map A_pcref        VDD
[end circuit call]
|
[circuit call]          clk_input
Port_map A_signal       46
Port_map D_receive      CLK_N
Port_map A_gnd          GND
Port_map A_gcref        GND
Port_map A_pcref        VDD
[end circuit call]
|
|DQ Models:
|DQ0:
[circuit call] dq_full
port_map a_signal 2
port_map d_drive Dq0
port_map d_enable Dq_oe
port_map d_receive Dq0
port_map a_gnd gnd
port_map a_GCREF gnd
port_map a_pcref vdd
port_map a_puref vdd
port_map a_pdref gnd
[end circuit call]

|DQ1:
[circuit call] dq_full
port_map a_signal 4
...
```



IBIS File

(screen 5)

New IBIS 4.1 External Circuit

Declaration of the AMS Power Supply, HDL Models, and Traditional IBIS table model.

```
| *** External Circuit Declarations
|Power Supply Circuit Call:
[external circuit]      Power
Language VHDL-AMS
Corner Typ supply.vhd supply(ideal)
Ports VDD GND
[end external circuit]
|
|Declare the VHDL DRAM model
[external circuit] MT46V64M16
Language VHDL-AMS
Corner Typ mt46v64m16.vhd MT46V64M16(behave)
Ports DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15
Ports LDQS UDQS A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 BA0 BA1
Ports CLK CLK_N CKE CS_N RAS_N CAS_N WE_N UDM LDM DQE
[end external circuit]
|
|
|**************************END EXTERNAL MODEL************************************
|
|**************************IBIS TABLE MODELS*************************************
|
[Model]          dq_full
Model_type       I/O
|
Vinl = 940.000mV
Vinh = 1.560V
Vmeas = 1.250V
Vref = 1.250V
Cref = 30.000pF
Rref = 50.000Ohm
|
|                                typ                 min                 max
|
C_comp                         3.460pF             3.190pF             3.730pF
|...
```

IBIS File (flow)

```
[Pin]    signal_name    model_name    R_pin      L_pin          C_pin
1        VDD            POWER         0.034      5.02nH         4.29pF  |POWER
2        DQ0            NC            0.043      5.22nH         1.26pF  |dqbuff
...
65       DQ15           NC            0.043      5.61nH         1.27pF  |dqbuff
66       VSS            GND           0.034      4.77nH         4.59pF  |GND
...
|************************EXTERNAL MODELS*************************************
[node declarations]
DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8 DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15
UDQS LDQS UDM LDM DQE A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13
BA0 BA1 RAS_N CAS_N WE_N CS_N CKE CLK CLK_N GND VDD TEST
[end node declarations]
| IBIS Model Instantiation
|DQ Models:
|DQ0:
[circuit call] dq_full
port_map a_signal 2
port_map d_drive Dq0
port_map d_enable Dq_oe
port_map d_receive Dq0
port_map a_gnd gnd
port_map a_GCREF gnd
port_map a_pcref vdd
port_map a_puref vdd
port_map a_pdref gnd
[end circuit call]
|
|Instantiate the VHDL Model
[circuit call] MT46V64M16
|Map DQ bits
Port_map DQ0    DQ0
Port_map DQ1    DQ1
...
Port_map DQE    DQE
[end circuit call]
|
```

```
|**IBIS TABLE MODELS****
|
[Model]          dq_full
Model_type       I/O
|
Vinl = 940.000mV
Vinh = 1.560V
Vmeas = 1.250V
Vref = 1.250V
Cref = 30.000pF
Rref = 50.0000hm
...
```

```
|Declare the VHDL DRAM model
[external circuit] MT46V64M16
Language VHDL-AMS
Corner Typ mt46v64m16.vhd MT46V64M16(behave)
Ports DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7 DQ8
Ports DQ9 DQ10 DQ11 DQ12 DQ13 DQ14 DQ15
Ports LDQS UDQS A0 A1 A2 A3 A4 A5 A6 A7
Ports A8 A9 A10 A11 A12 A13 BA0 BA1
Ports CLK CLK_N CKE CS_N RAS_N CAS_N WE_N
Ports UDM LDM DQE
[end external circuit]
|
```

AMS File

(screen 1)

Memory HDL File

I/O declaration and declaration of Internal Signals

```
1   ------------------------------------------------------------------
2   LIBRARY IEEE;
3       USE IEEE.STD_LOGIC_1164.ALL;
4       USE IEEE.STD_LOGIC_UNSIGNED.ALL;
5       USE IEEE.STD_LOGIC_ARITH.ALL;
6
7   ENTITY MT46V64M16 IS
8      PORT (
9         dq0 : inout STD_LOGIC:='Z';
10        dq1 : inout STD_LOGIC:='Z';
11        ...
12        Addr0 : IN    STD_LOGIC;
13        Addr1 : IN    STD_LOGIC;
14        ...
15        Clk   : IN    STD_LOGIC;
16        Clk_n : IN    STD_LOGIC;
17        Ras_n : IN    STD_LOGIC;
18        Cas_n : IN    STD_LOGIC;
19        We_n  : IN    STD_LOGIC;
20        DqE   : OUT   STD_LOGIC
21      );
22  END MT46V64M16;
23
24  architecture behave of MT46V64M16   is
25      -- Array for Read pipeline
26      TYPE Array_Read_cmnd IS ARRAY (8 DOWNTO 0) OF STD_LOGIC;
27      TYPE Array_Read_bank IS ARRAY (8 DOWNTO 0) OF STD_LOGIC_VECTOR
28      TYPE Array_Read_cols IS ARRAY (8 DOWNTO 0) OF STD_LOGIC_VECTOR
29
```

AMS File

(screen 2)

```
-- Commands Decode
Active_enable    <= NOT(Cs_in) AND NOT(Ras_in) AND     Cas_in  AND     We_in;
Aref_enable      <= NOT(Cs_in) AND NOT(Ras_in) AND NOT(Cas_in) AND     We_in;
Burst_term       <= NOT(Cs_in) AND     Ras_in  AND     Cas_in  AND NOT(We_in);
Ext_mode_enable  <= NOT(Cs_in) AND NOT(Ras_in) AND NOT(Cas_in) AND NOT(We_in);
Mode_reg_enable  <= NOT(Cs_in) AND NOT(Ras_in) AND NOT(Cas_in) AND NOT(We_in);
Prech_enable     <= NOT(Cs_in) AND NOT(Ras_in) AND     Cas_in  AND NOT(We_in);
Read_enable      <= NOT(Cs_in) AND     Ras_in  AND NOT(Cas_in) AND     We_in;
Write_enable     <= NOT(Cs_in) AND     Ras_in  AND NOT(Cas_in) AND NOT(We_in);
```

HDL code to decode Commands

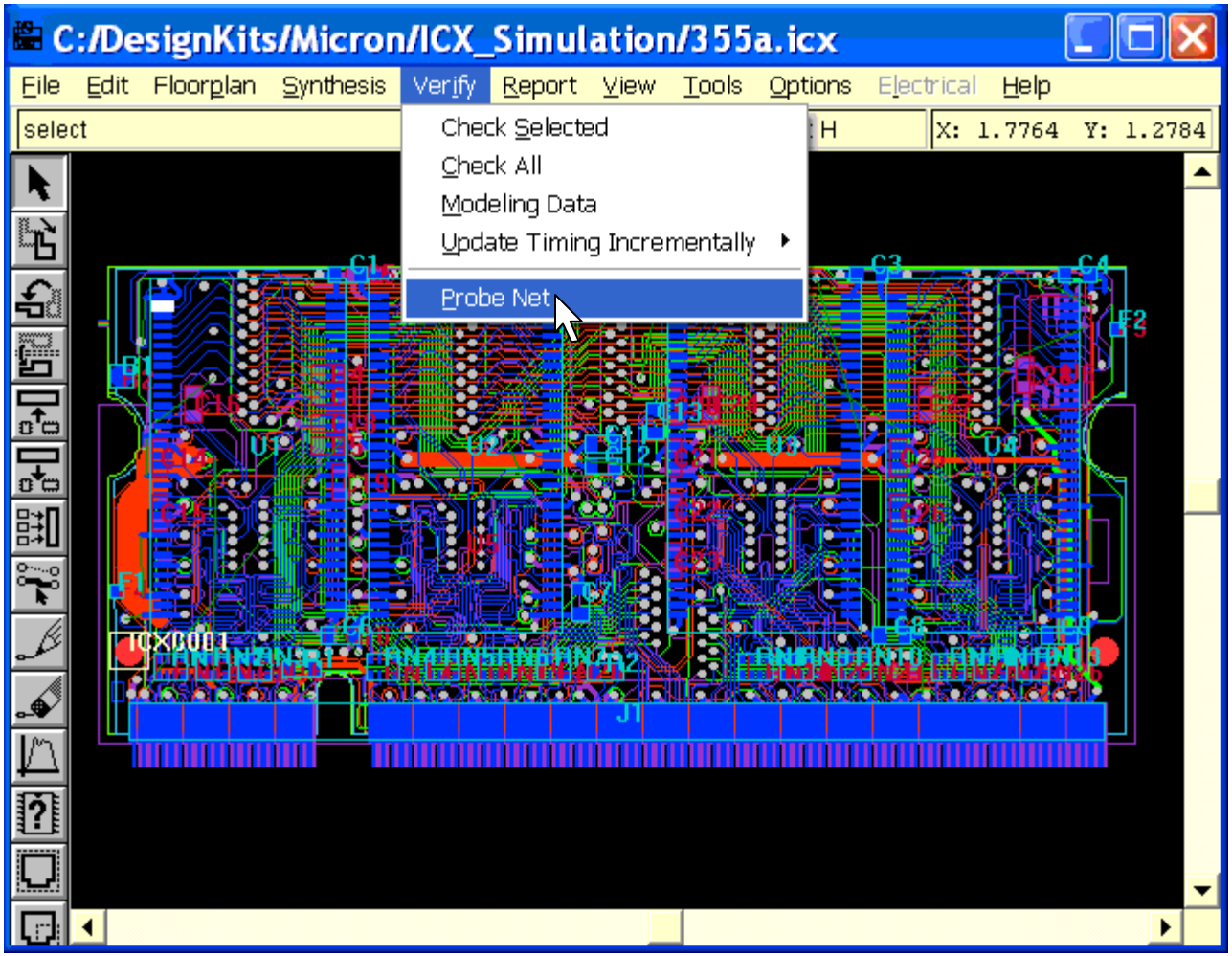
AMS File

(screen 3)

Code for Timing checks

```
Hold_check : PROCESS
BEGIN
    WAIT ON Sys_clk'DELAYED (tIH);
    IF Sys_clk'DELAYED (tIH) = '1' THEN
        ASSERT(Cke'LAST_EVENT >= tIH)
            REPORT "CKE Hold time violation -- tIH"
            SEVERITY WARNING;
        ASSERT(Cs_n'LAST_EVENT >= tIH)
            REPORT "CS# Hold time violation -- tIH"
            SEVERITY WARNING;
        ASSERT(Cas_n'LAST_EVENT >= tIH)
            REPORT "CAS# Hold time violation -- tIH"
            SEVERITY WARNING;
        ASSERT(Ras_n'LAST_EVENT >= tIH)
            REPORT "RAS# Hold time violation -- tIH"
            SEVERITY WARNING;
        ASSERT(We_n'LAST_EVENT >= tIH)
            REPORT "WE# Hold time violation -- tIH"
            SEVERITY WARNING;
        ASSERT(Addr'LAST_EVENT >= tIH)
            REPORT "ADDR Hold time violation -- tIH"
            SEVERITY WARNING;
        ASSERT(Ba'LAST_EVENT >= tIH)
            REPORT "BA Hold time violation -- tIH"
            SEVERITY WARNING;
    END IF;
END PROCESS;
```

Verification Procedure



1) Import layout

2) Import Models

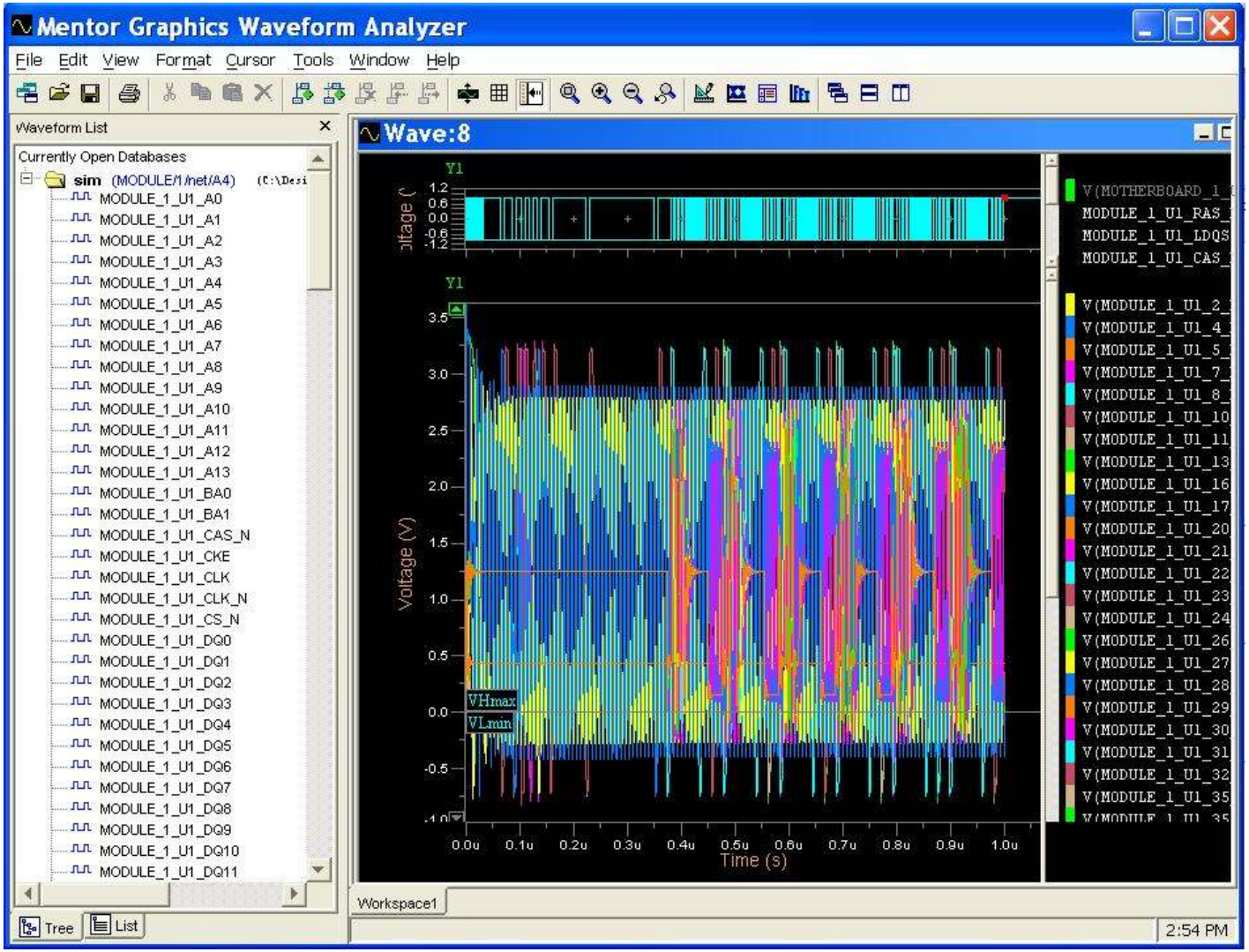
3) Assign Models

4) Probe Any Net

… 5 minutes later …

Verification Procedure (continued)

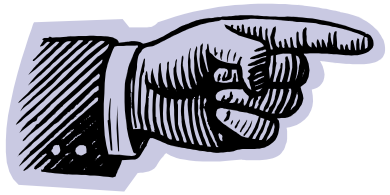
5) Analyze Results



Verification Procedure

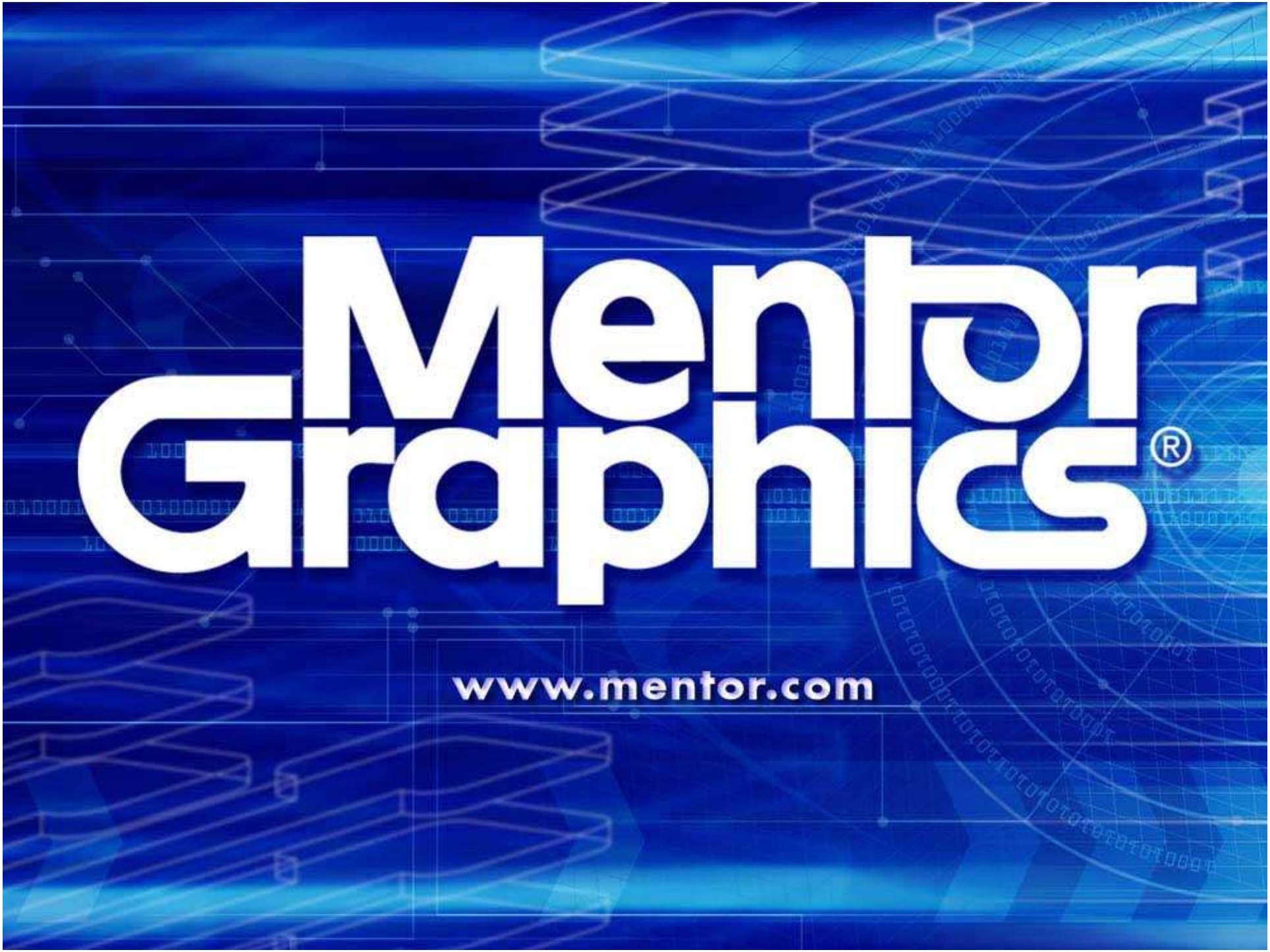
(continued)

5) Analyze Results



C:\WINDOWS\system32\cmd.exe - ismb

```
C:\DesignKits\Micron\ICX_Simulation>ismb
;; System Level Interconnect Synthesis
;; Version: 3.5.03_02    Date: Wed Nov 16 16:33:27 2005
;; Copyright Mentor Graphics Corporation 1994-2005
;; All Rights Reserved
;;
;; UNPUBLISHED, LICENSED SOFTWARE.
;; CONFIDENTIAL AND PROPRIETARY INFORMATION
;; WHICH IS THE PROPERTY OF MENTOR GRAPHICS CORPORATION
;; OR ITS LICENSORS.
;;
;;              Restricted Rights Legend
;;
;;    Use, duplication or disclosure is subject
;;    to restrictions stated in contract number
;;      MDA972-93-C-0045 with Mentor Graphics
;;                    Corporation
;; icx1                  Version: 3.5.03_02  Nov 16 2005 14:39:12
;; schemer               Version: 3.5.03_02  Nov 16 2005 14:39:12
;; charter               Version: 3.5.03_02  Nov 16 2005 14:39:12
;; ismb                  Version: 3.5.03_02  Nov 16 2005 14:39:12
;; Note: Resolving subsystem at C:/DesignKits/Micron/ICX_Simulation/355a.ifc
;; Note: Resolving subsystem at C:/DesignKits/Micron/ICX_Simulation/vt8633_1
;; Note: Using ICX_IBIS_SEARCH_PATH for mated models search path.
;; Note: Mated Model file search path is  .
;; is                    Version: 3.5.03_02  Nov 16 2005 14:39:12
;; Note: Opening design "C:/DesignKits/Micron/ICX_Simulation/355a.icx".
;; Note: Analyzing ElectricalNet A4
;;
;; No Errors Detected
```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