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SSO Simulation with IBIS

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Overview

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- Motivation
- SSN with IBIS in 2000
  - Simulation setup
  - BEHAVIOR – model with Voltage-Controlled Current Sources
  - very good concordance with transistor based models
- Table driven kssn-multiplier
  - Multiplier extraction
  - Results HSPICE vs. VCCS-BEHAVIOR
  - Lacking concordance
- Enhanced VCCS-BEHAVIOR
  - Additional RC – Timing coeficient
  - Improved results
- Summary

Acknowledgements

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INFINEON TECHNOLOGIES

- HYB18T512160AF
- DDR2 - Memory

TEXAS INSTRUMENTS

- CDCE706
- PROGRAMMABLE 3-PLL CLOCK SYNTHESIZER / MULTIPLIER / DIVIDER

SSO Simulation Setup
(m+1 switching outputs)

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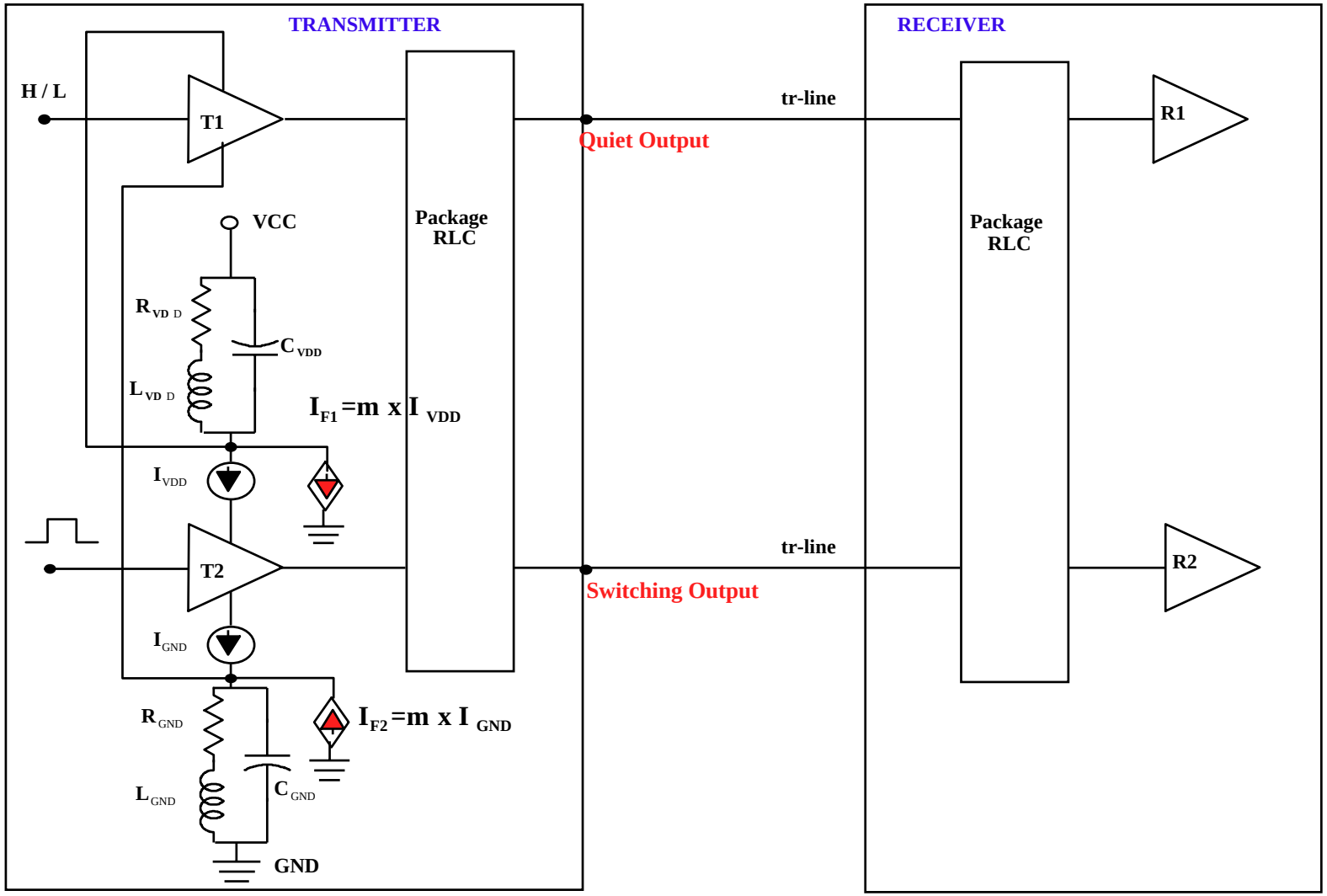

VCCS-Model enhancement

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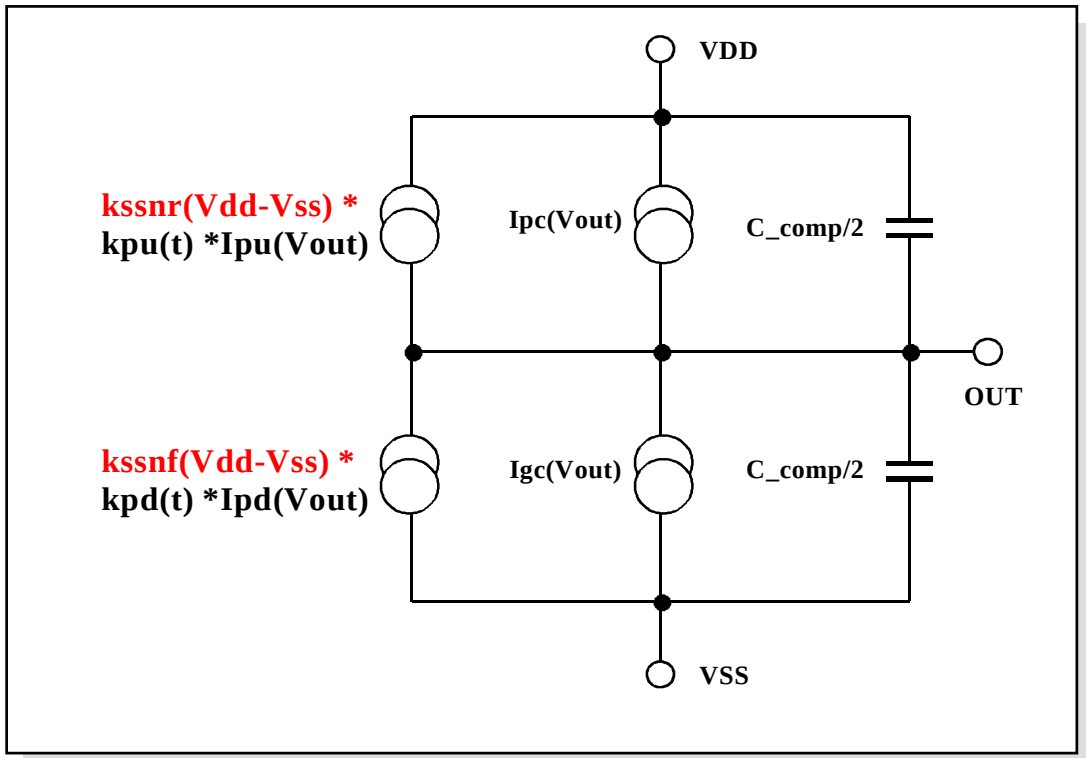

- A second multiplier for rising (**kssnr**) and falling (**kssnf**) edges
- Both multipliers are controlled by the (Vdd-Vss) voltage drop
- *Feedback on the gate source voltage of the output transistors*
- Multiplier generation:
  - ➢Pullup/down V/I-tables as a function of Vdd
  - ➢SSO-V/t-table (Golden Waveform)

VCX16244 SSN analysis results (rising edge)

Enhanced two waveform behavioral model Number of SSO = 6

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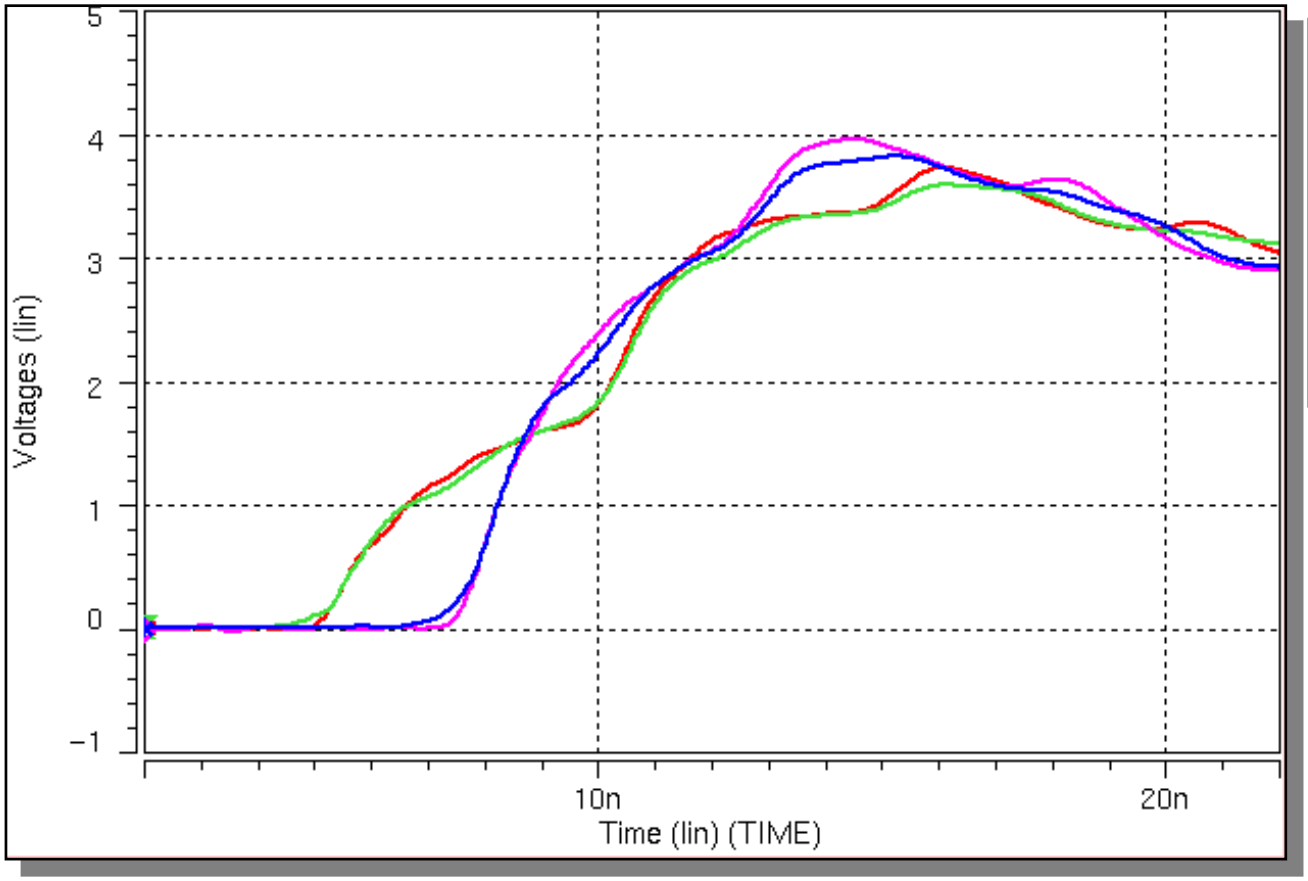

Node OUT:
Transistor based
Behavioral

Node END:
Transistor based
Behavioral

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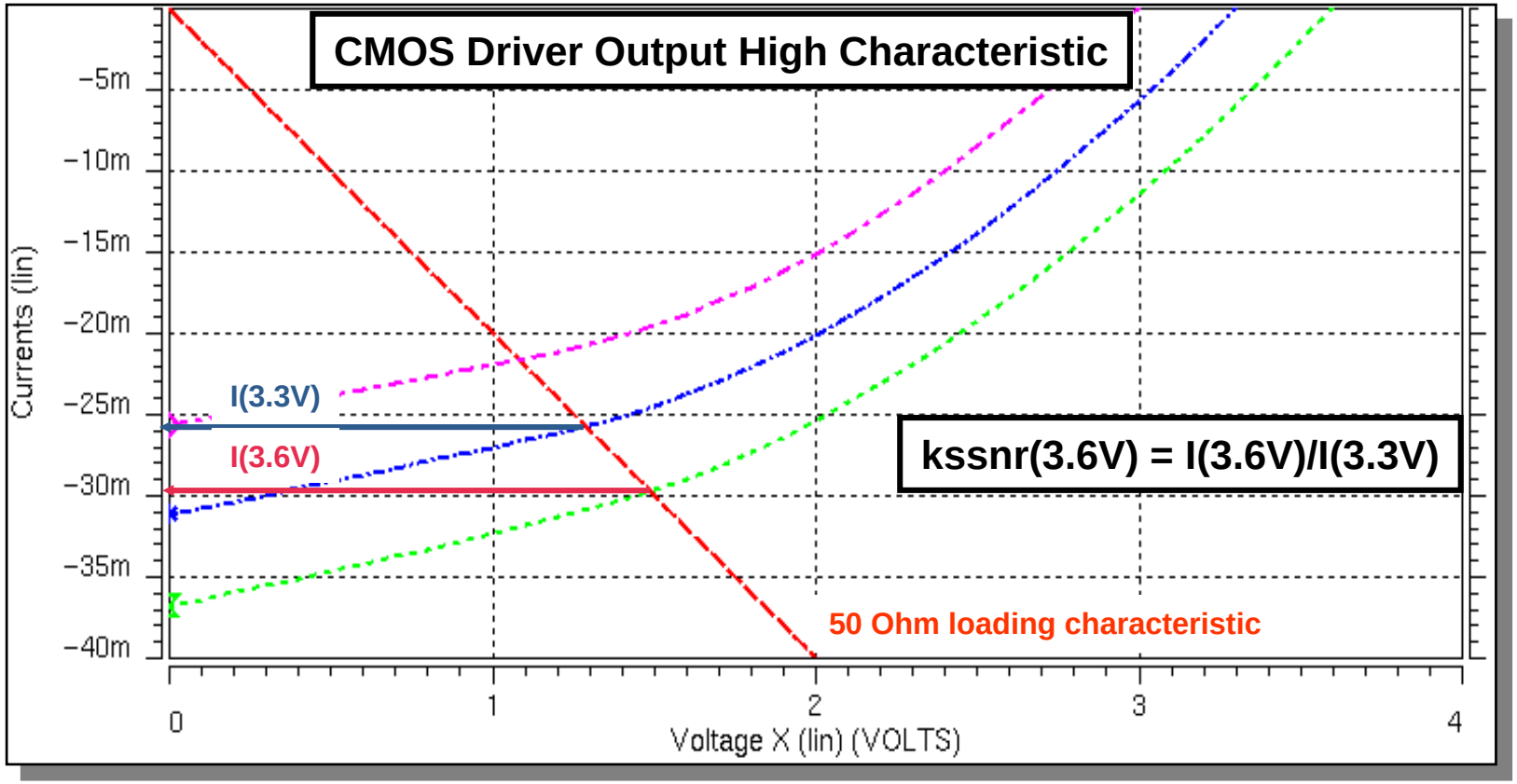
kssnr/f Multiplier Generation Method



kssn rising coefficient extraction HYB18T512160AF (DDR2) INFINEON

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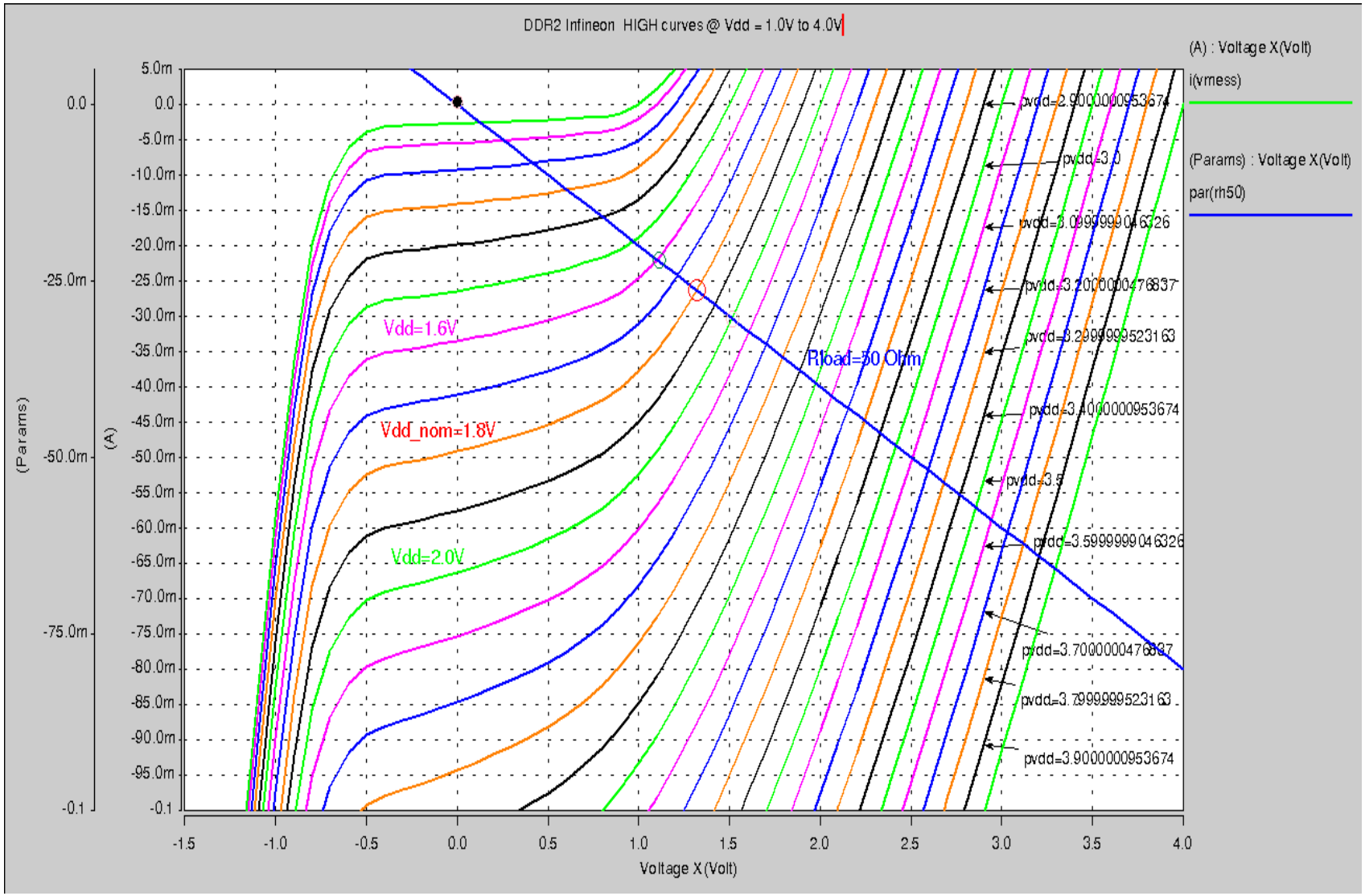

kssn falling coefficient extraction HYB18T512160AF (DDR2) INFINEON

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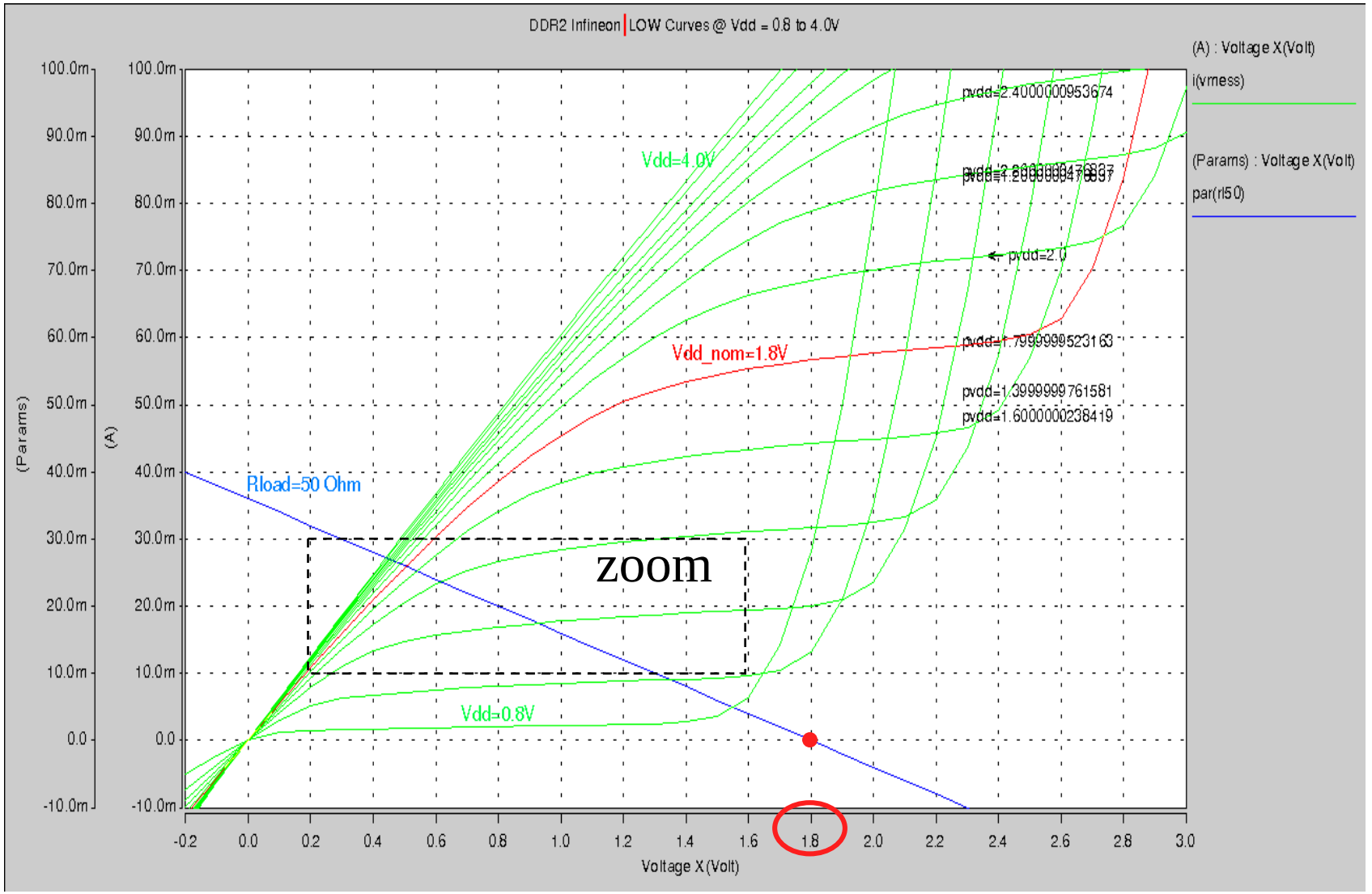
Overview

SSN 2000

kssn - table

Enhanced VCCS model

Summary



kssn falling coefficient extraction (zoom) HYB18T512160AF (DDR2) INFINEON

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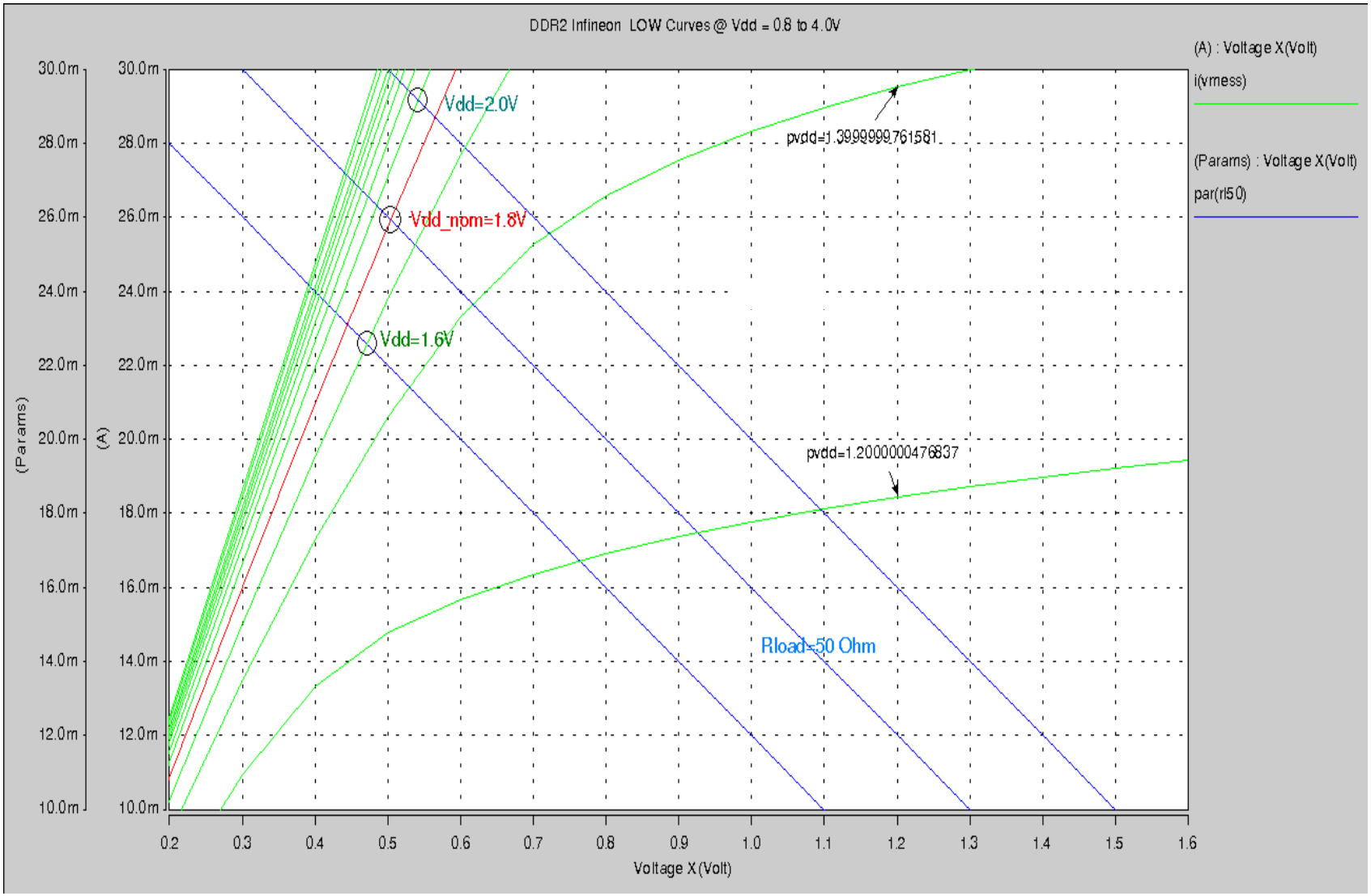

HYB18T512160AF / INFINEON
kssn rising/falling @ Vdd = 0.5V to 3.6V (1.8V nom.)

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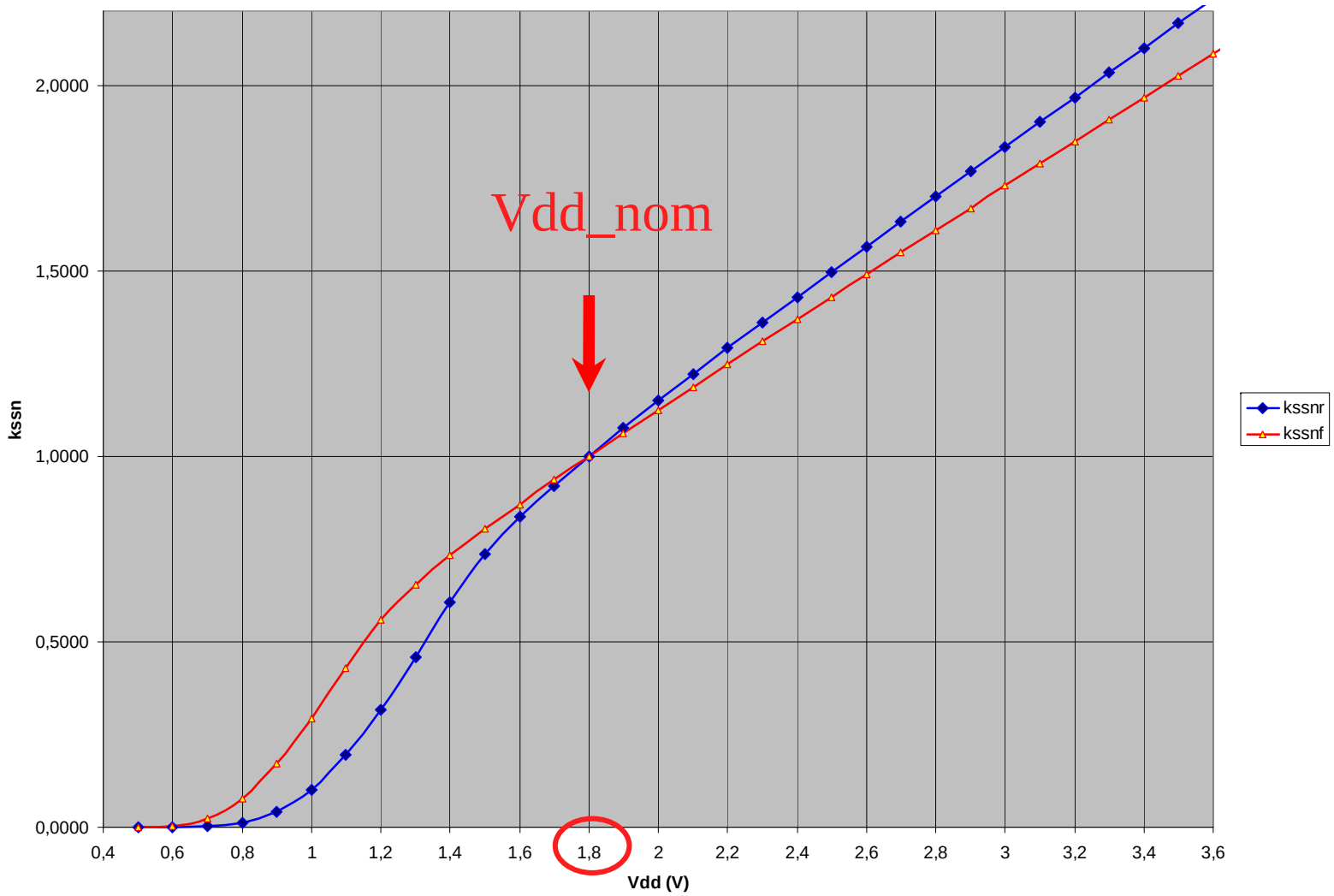

TI CDCE706 TEXAS INSTRUMENTS
kssn rising/falling @ Vdd = 0.5V to 5V (3.3V nom.)

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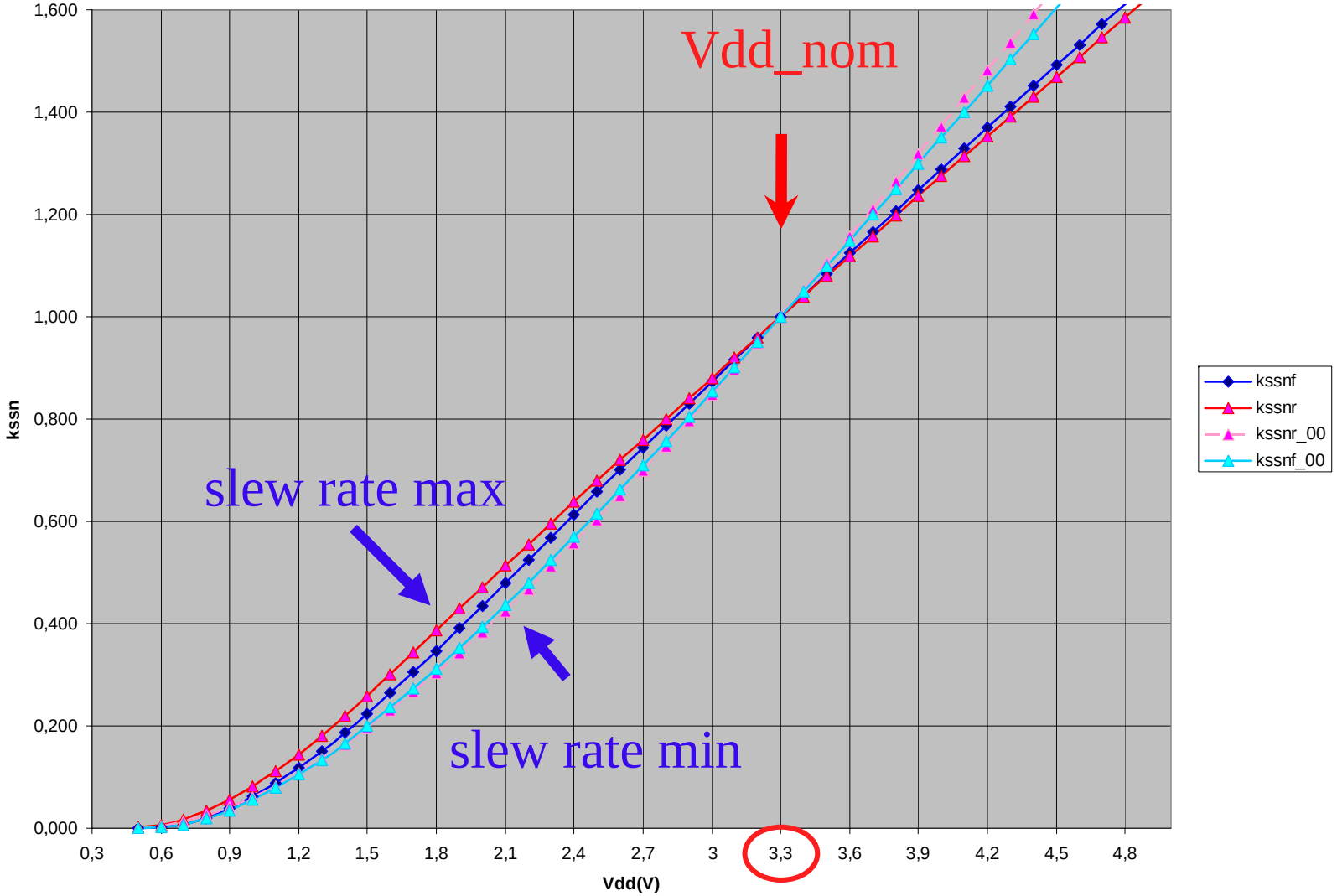
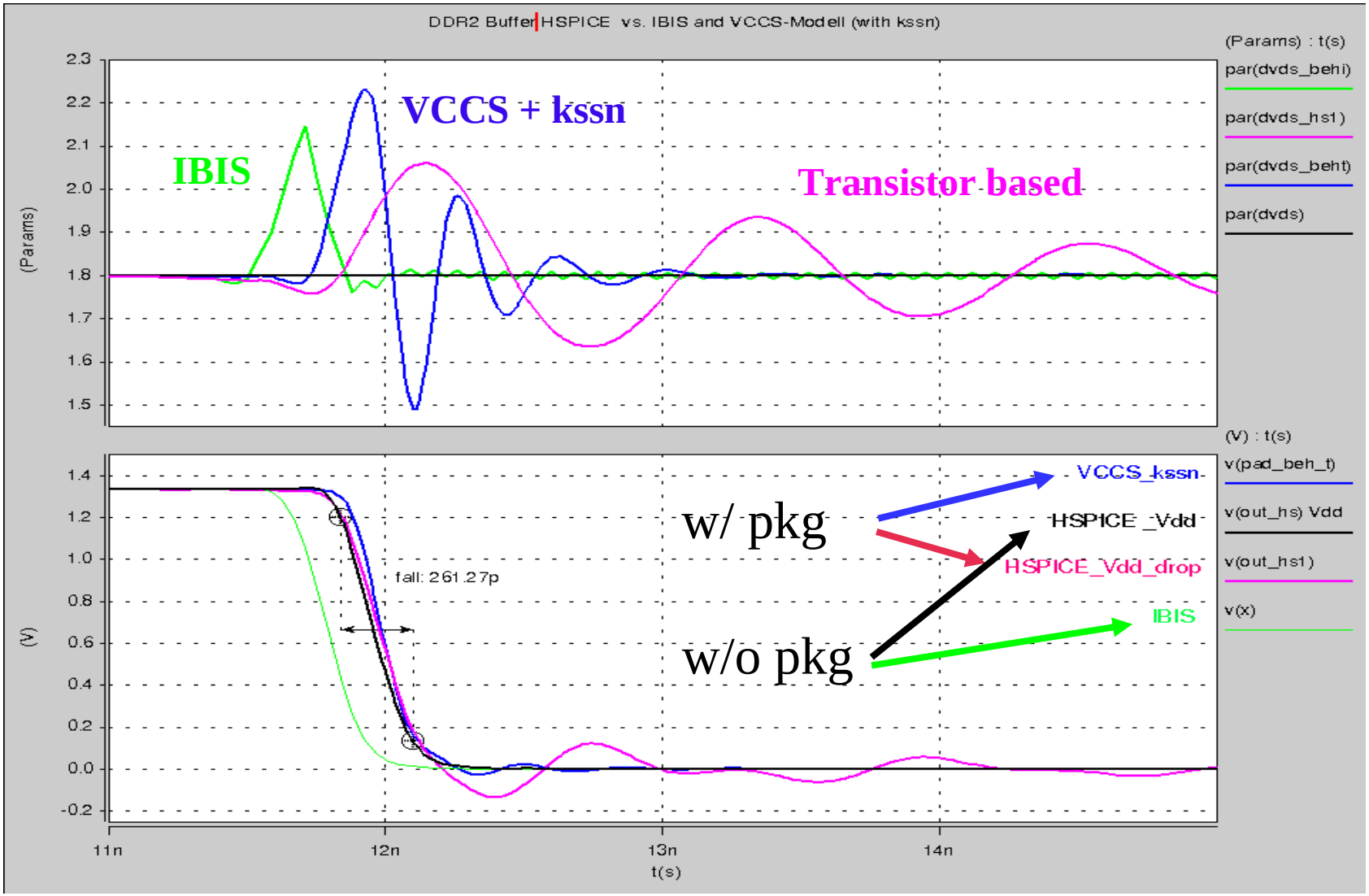


DDR2 buffer Infineon
Supply voltage drop (L=2x1nH) / Load Tline Zo=50 Ohm



TI CDCE706 / **Voltage drop** / **Rising edge**
VCCS-model with kssn table (L=2x3nH)

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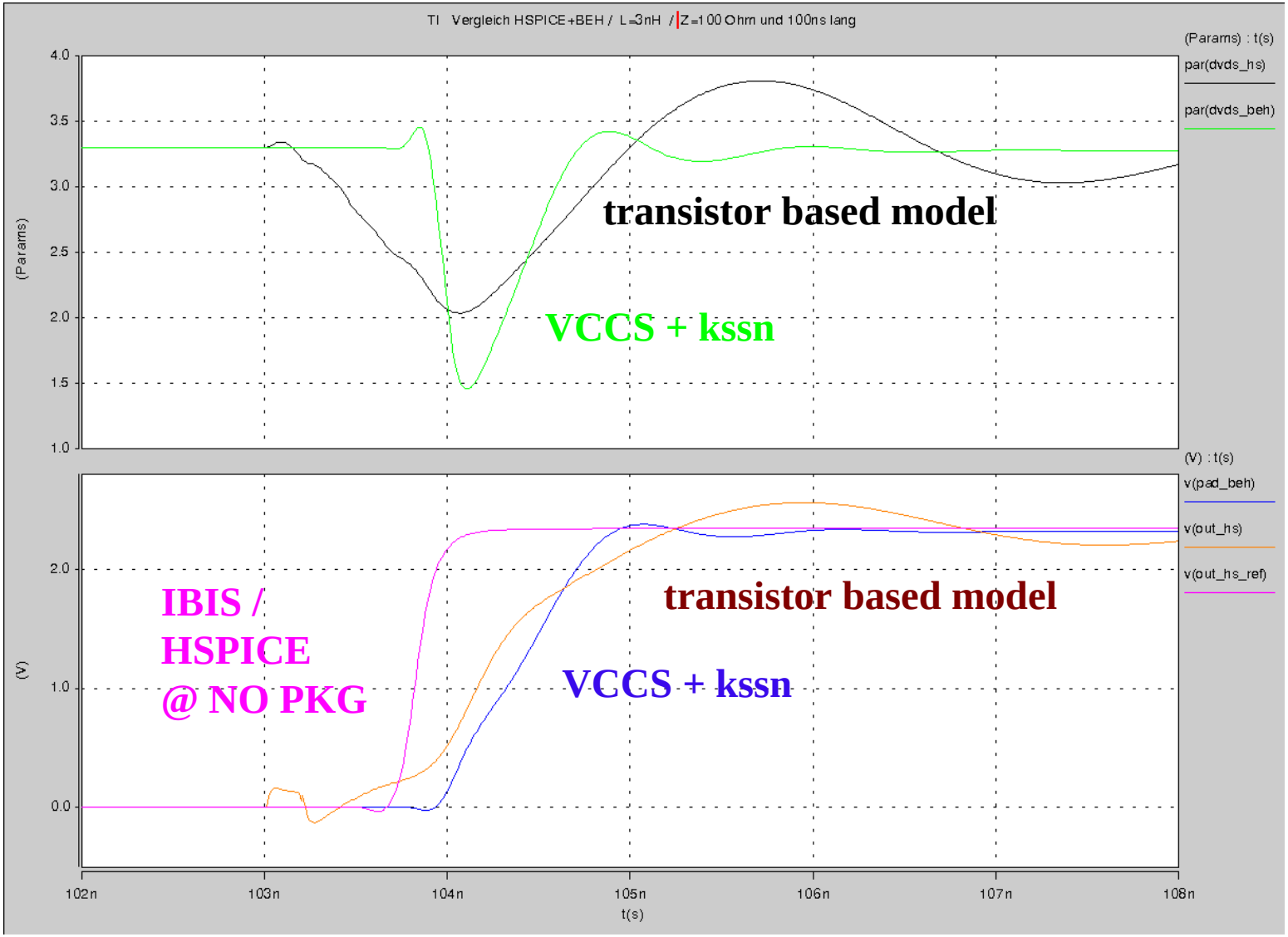

TI CDCE706 Rising edge vs. Vdd drop
Transistor based model

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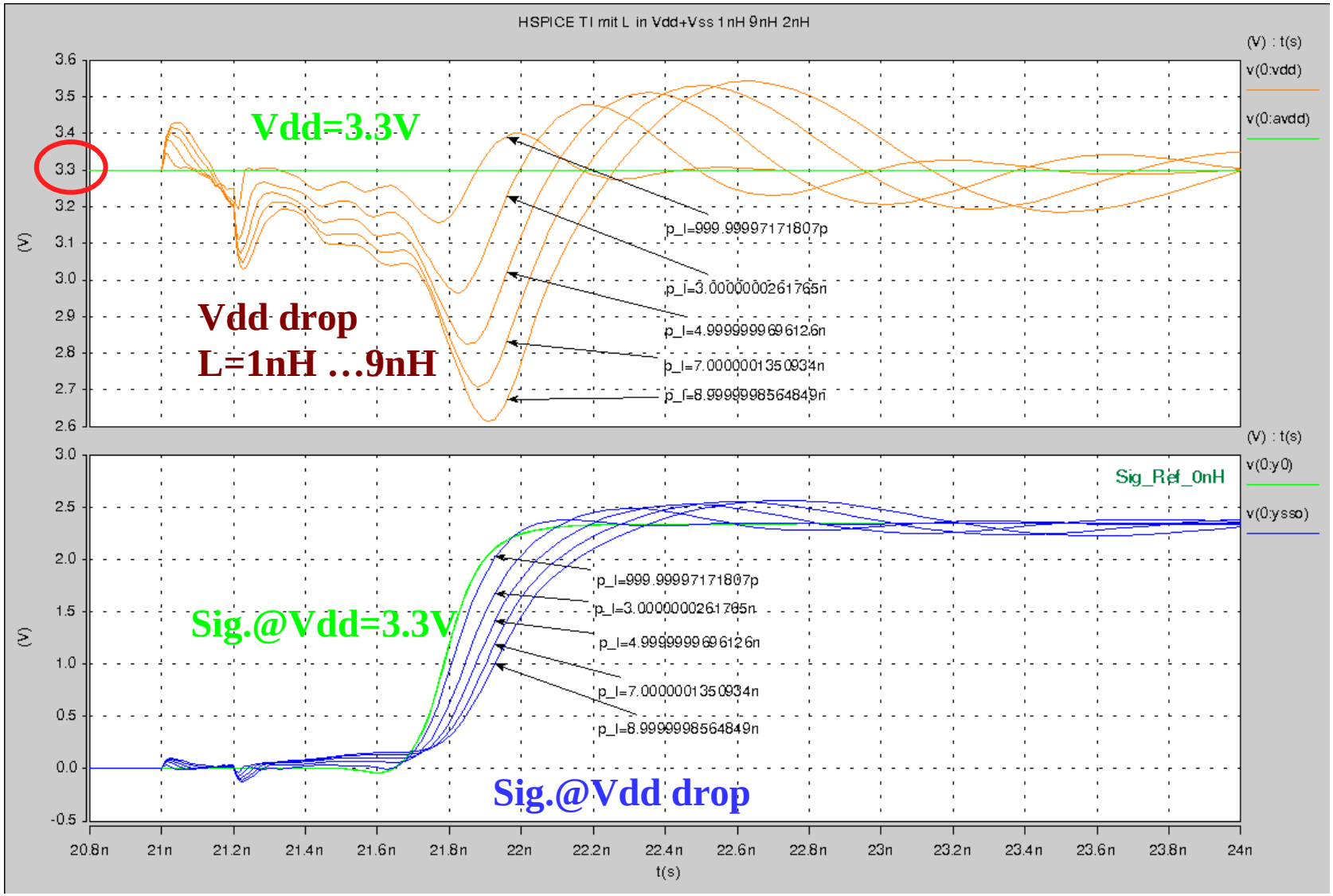

TI CDCE706 **Falling edge vs. Vdd drop**
Transistor based model

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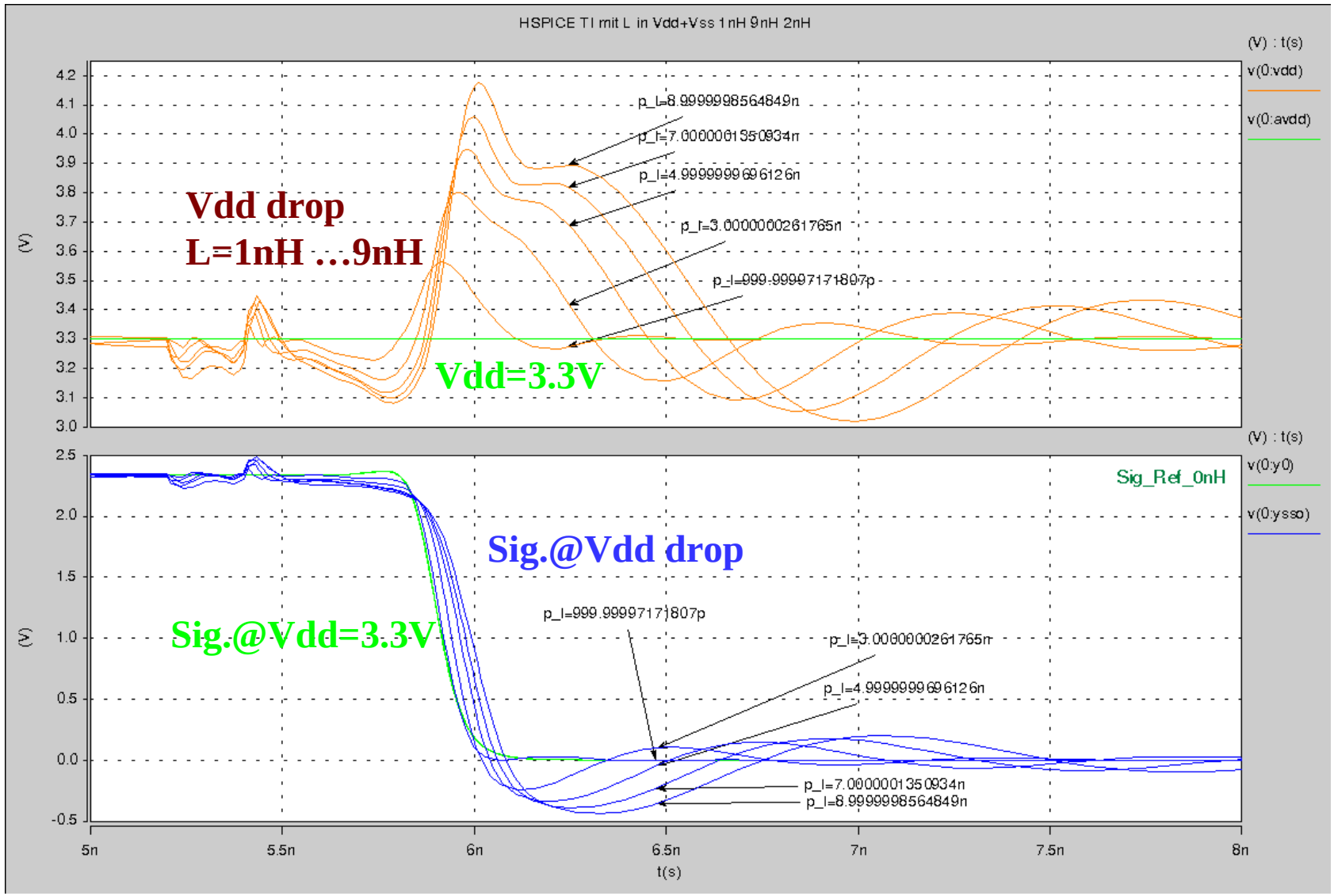

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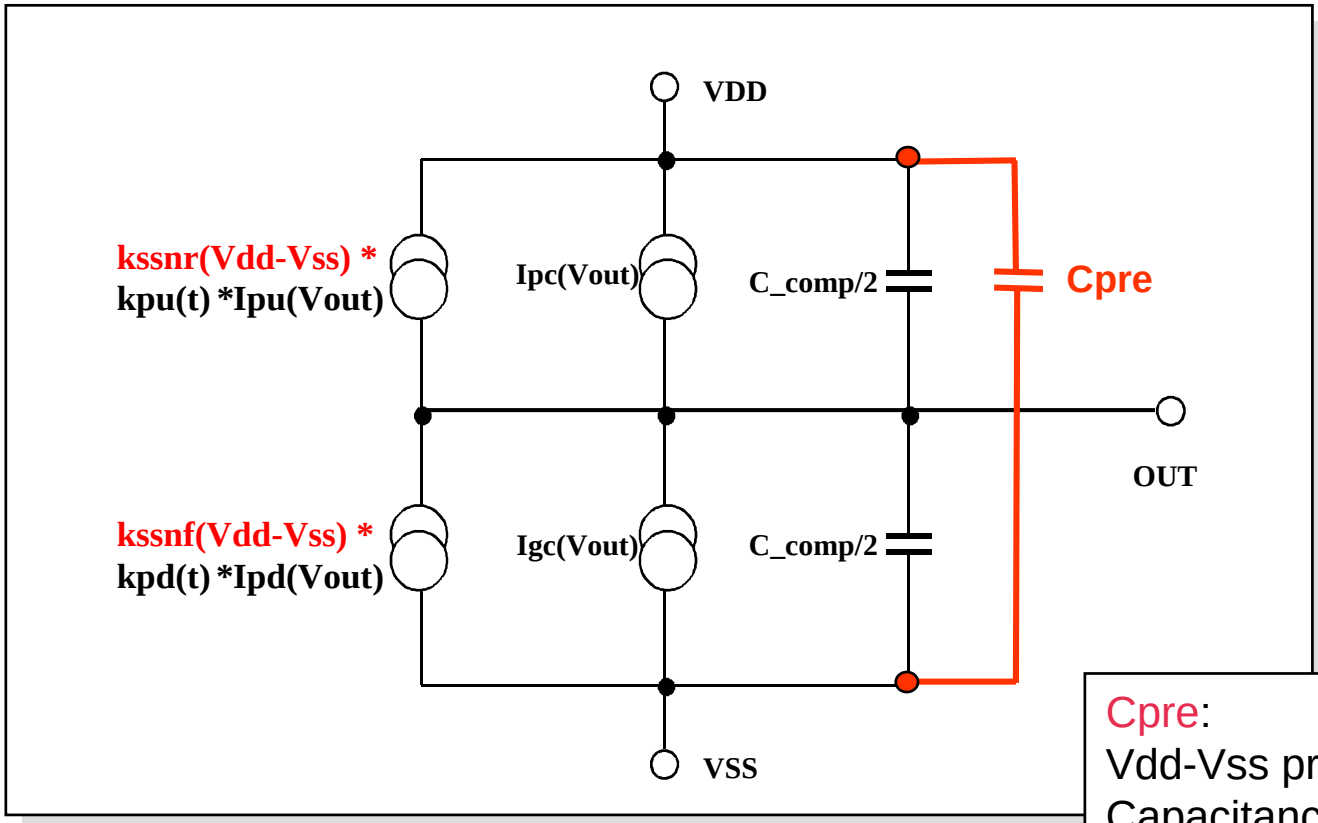
Differences VCCS 2000 vs. 2006

	VCCS 2000	VCCS 2006
❑ Transition Time	ca. 5ns	<500ps
❑ Operation Point	saturation region	linear region
❑ Vdd/GND drop		
➢ amplitude	ca. 15%Vdd	ca. 40% Vdd
➢ width	ca. 7ns	ca. 1ns
❑ Design of the OUTPUT stage		
➢ Time domains	NO	YES
➢ Slew rate control	NO/YES	YES
➢ Vdd-drop Feed back	NO	YES
➢ Prestage @Vdd_int	NO/YES	YES
➢ On-die capacitance	NO	YES

Improvement with prestage capacitance Cpre



Cpre:
Vdd-Vss prestage Capacitance

Evaluation:
SPICE simulation using a capacitance bridge

Vdd drop improvement with Cpre=30pF
CDCE706 with PKG L=2x3nH 10 SSO

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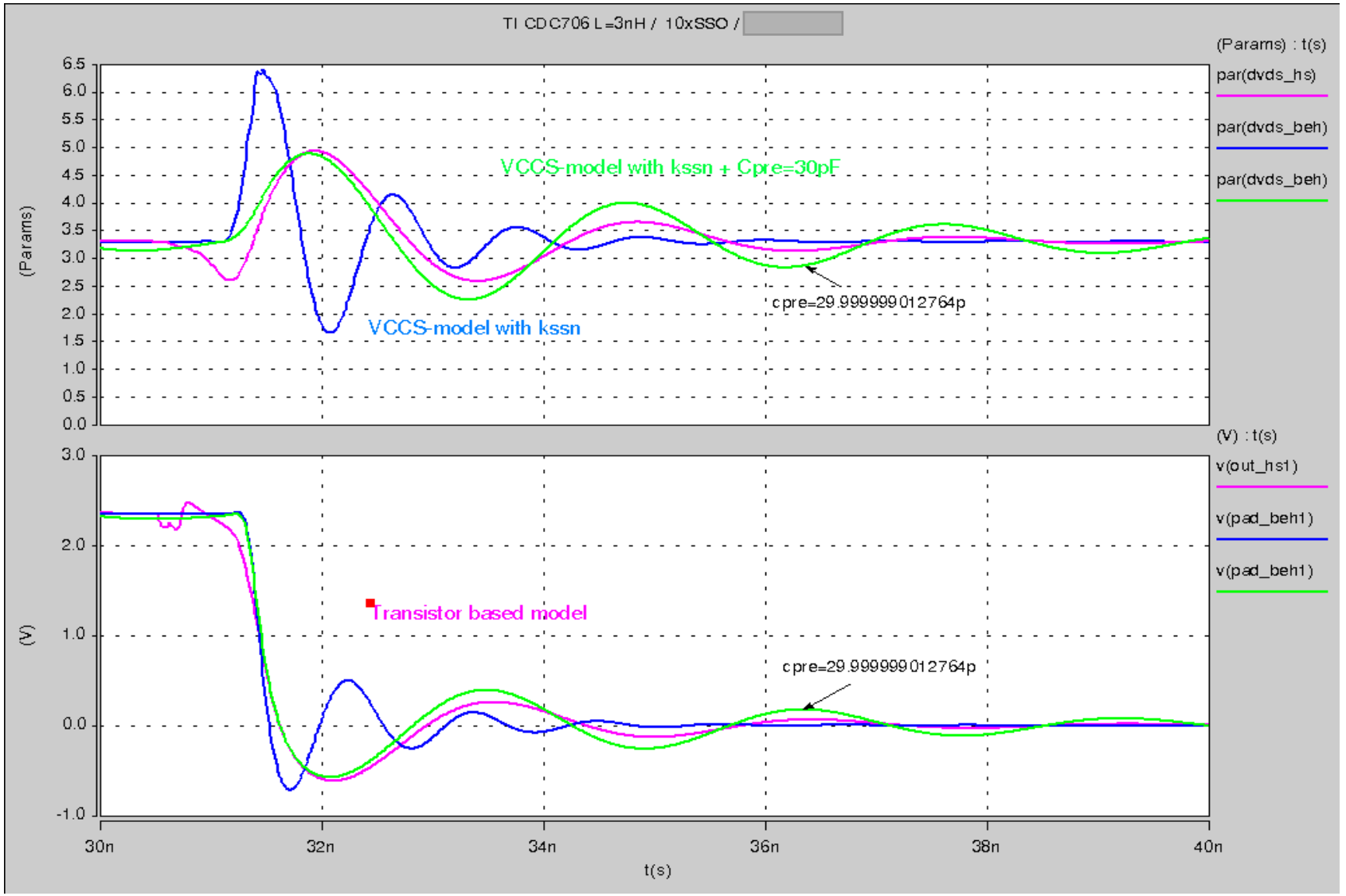

Vdd drop improvement with Cpre=30pF CDCE706 with PKG L=2x3nH 10 SSO

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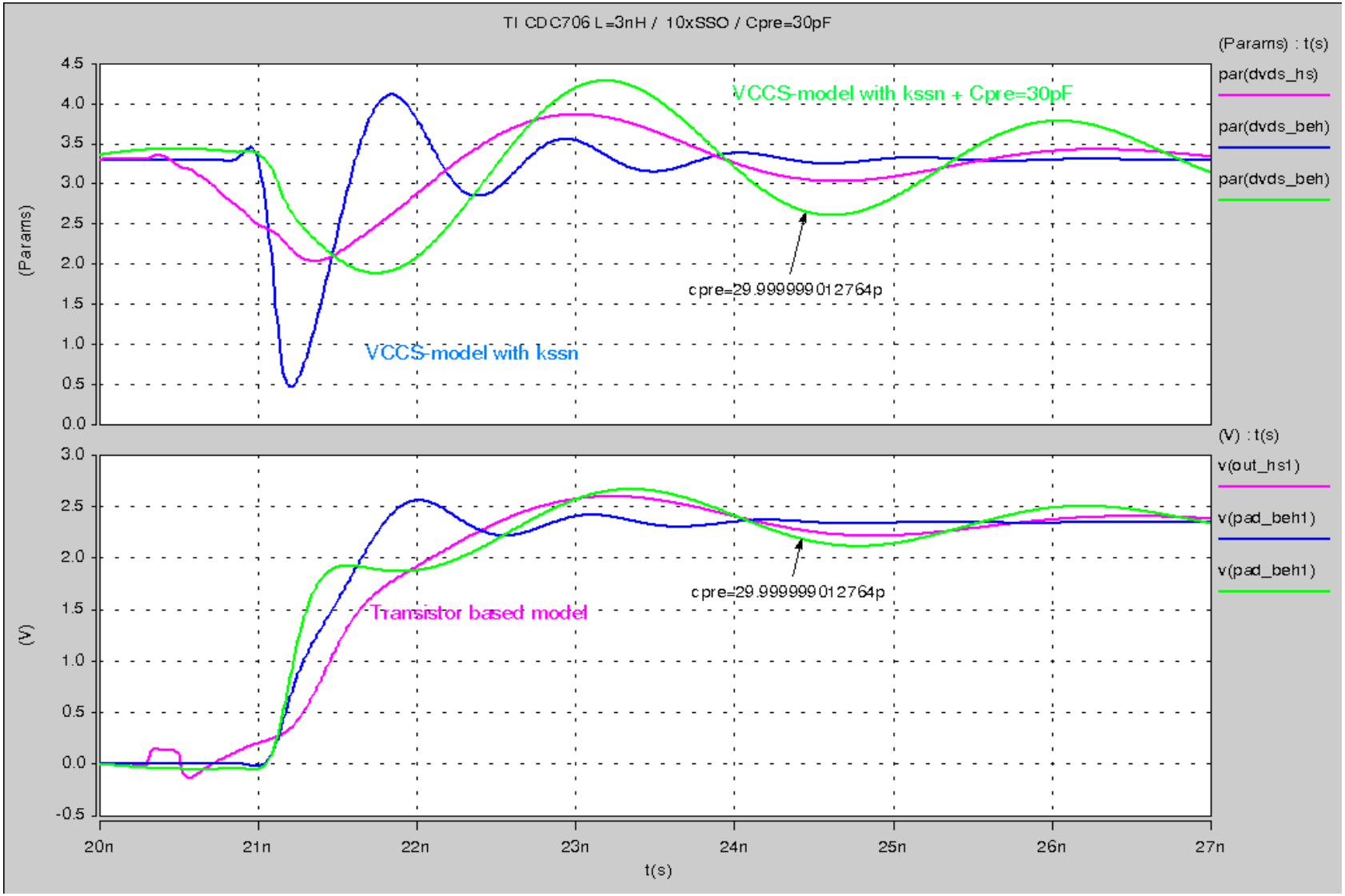

Enhanced VCCS-Behavior Model
with kssn (static) and td_RC (dynamic) coefficients

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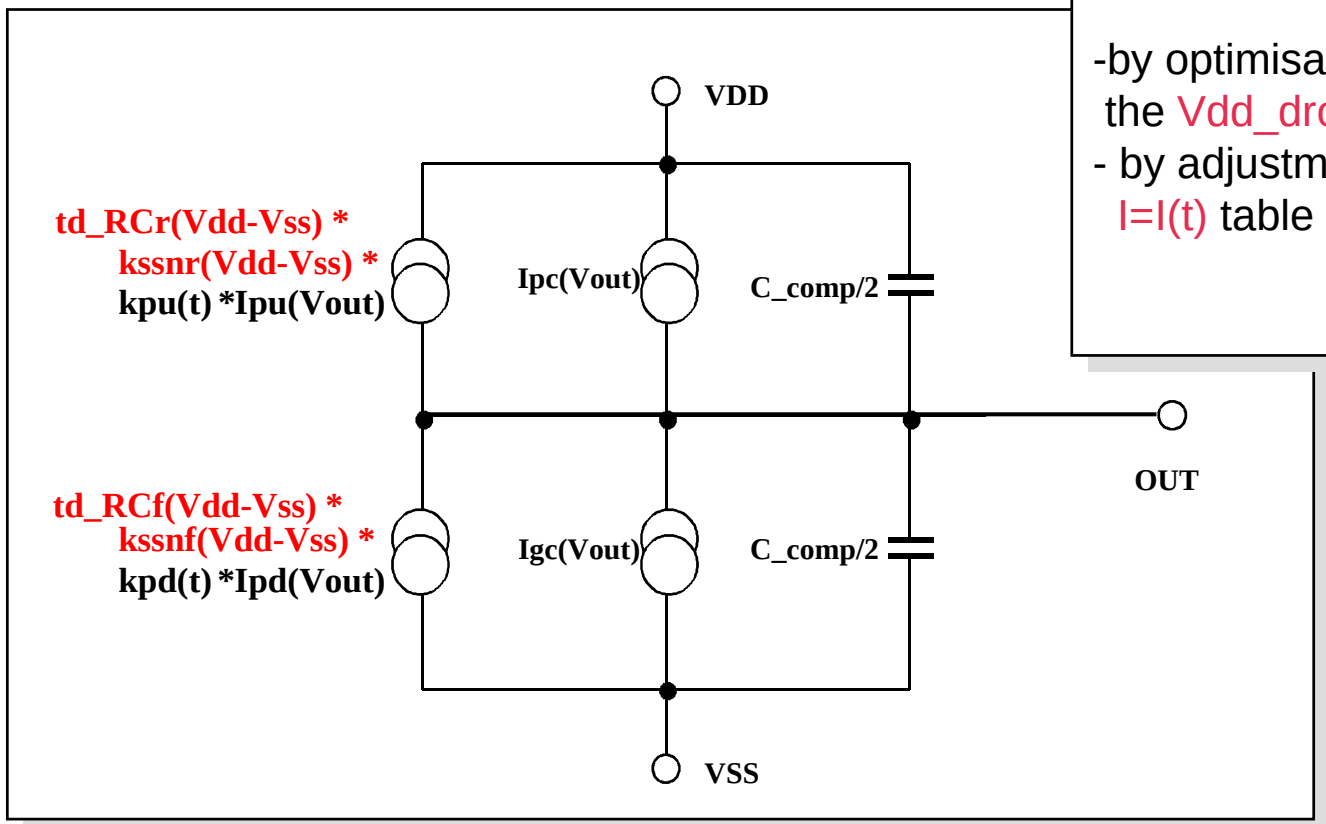

td_RC determination

-by optimisation through the Vdd_drop @ known L
- by adjustment from I=I(t) table @ L

Vdd drop improvement
DDR2 with PKG L=2x3nH 5 SSO

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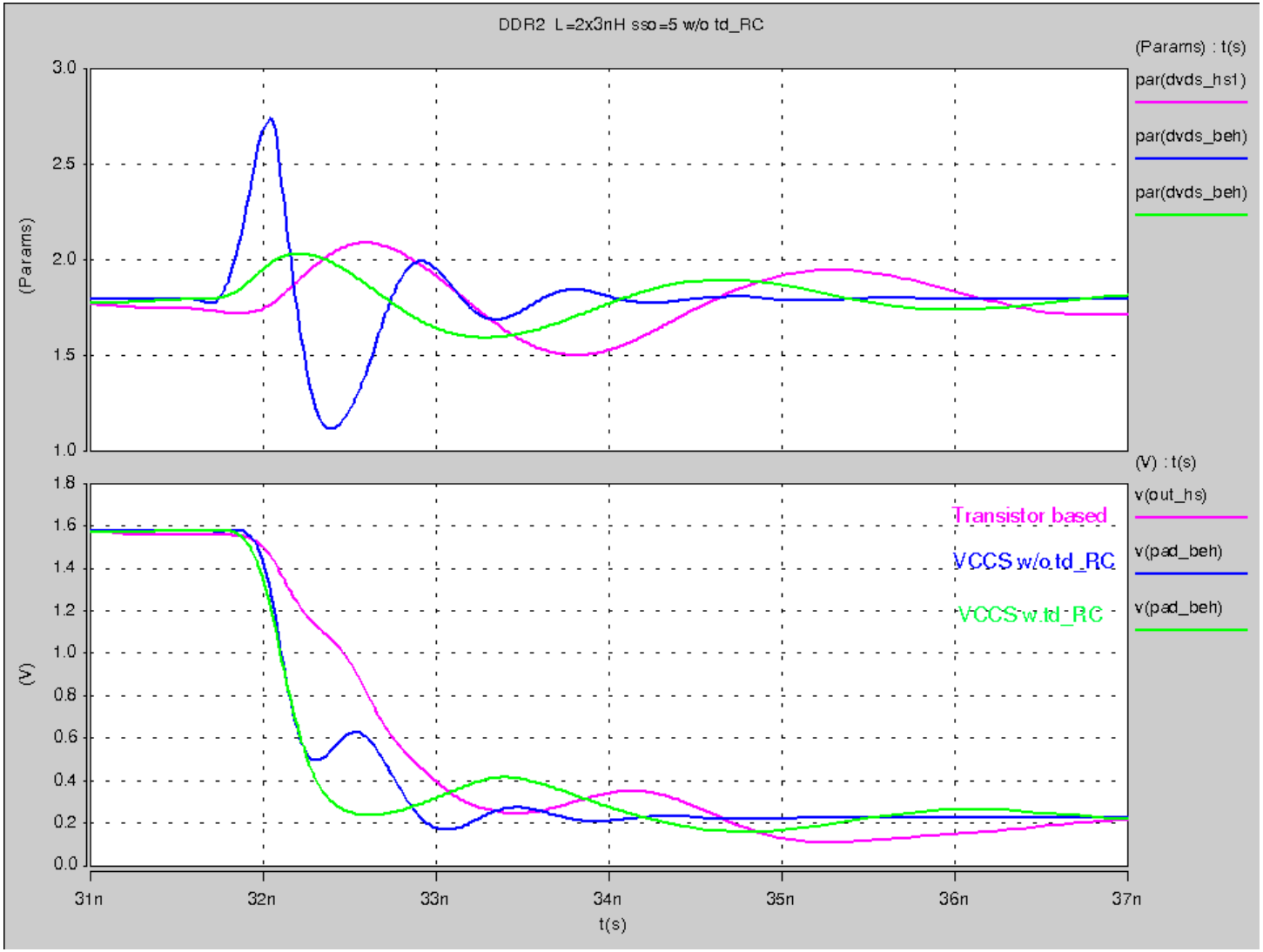

Vdd drop improvement
CDCE706 with PKG L=2x3nH 10 SSO

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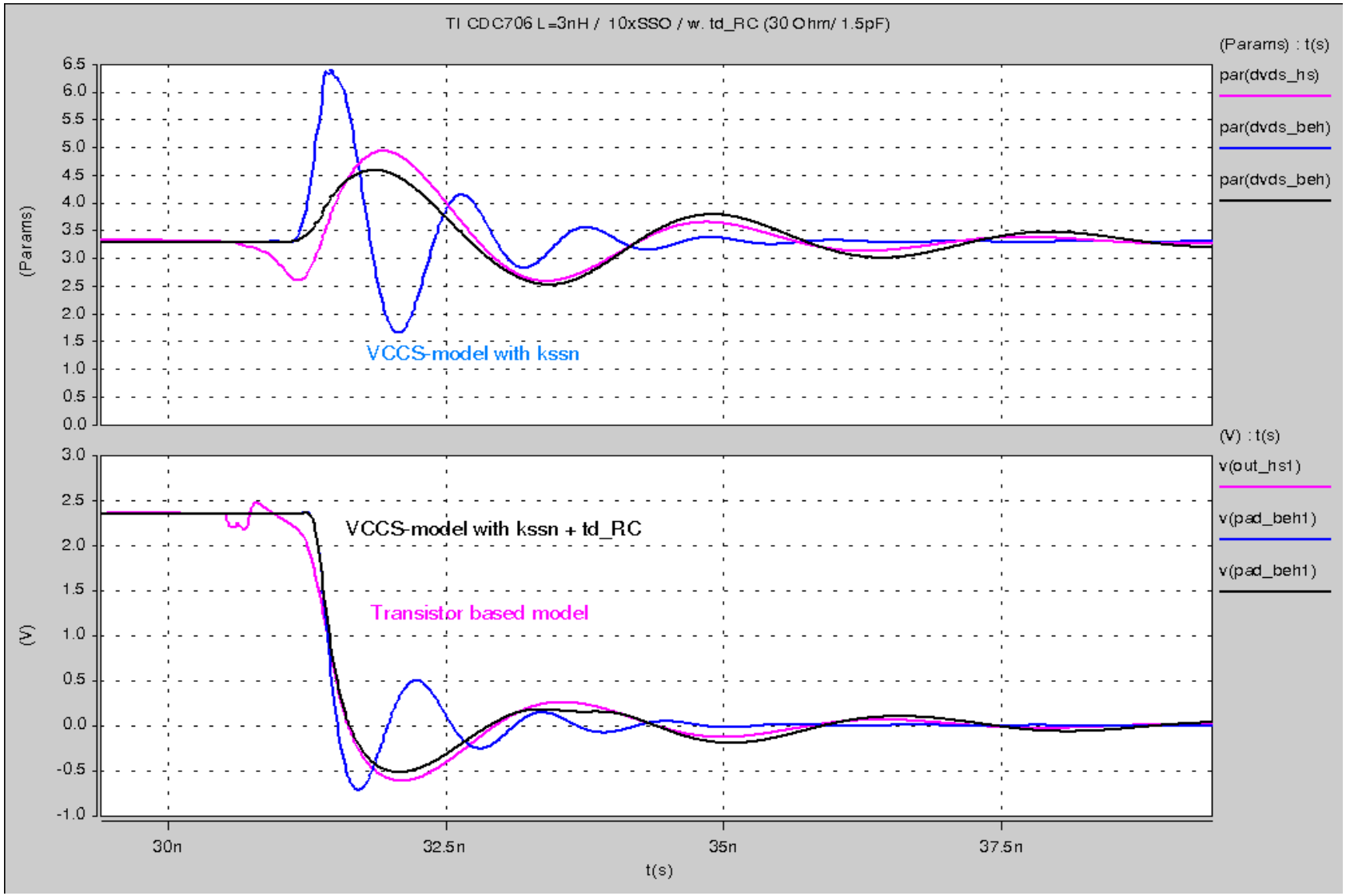

Summary

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- With improved IBIS models, SSO can be simulated in a better concordance with transistor based models, IF
  - kssn – table information (BIRD 97.x)
  - current vs. time tables @ known RLC environment (BIRD 95)
- Advantages
  - Signal integrity analysis
    - PDS – Voltage drop
    - Timing simulation
- More investigations have to be done, to evaluate for different technologies, the validity range and the accuracy of the proposed improvement

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Questions