

IBIS Open Forum Minutes

Meeting Date: June 5, 2014 Meeting Location: DAC IBIS Summit, San Francisco, CA, USA

VOTING MEMBERS AND 2014 PARTICIPANTS

Agilent Technologies	Radek Biernacki, Nilesh Kamdar, Colin Warwick, Graham Riley, Pegah Alavi*, Fangyi Rao,
	Heidi Barnes, Dimitrios Drogoudis
Altera	David Banas*, Kundan Chand, Hsinho Wu
ANSYS	(Steve Pytel)
Applied Simulation Technology	Fred Balistreri, Norio Matsui
Cadence Design Systems	Ambrish Varma, Brad Brim*, Joy Li, Kumar Keshavan, Ken Willis, Yingxin Sun, Joshua Luo, John Phillips
Ericsson	Anders Ekholm, Zilwan Mahmod
Infineon Technologies AG	(Christian Sporrer)
Intel Corporation	Michael Mirmak*, Jon Powell, Riaz Naseer
	Udy Shrivastava, Mustafa Yousuf, Jimmy Jackson Pietro Brenner
IO Methodology	Lance Wang, Michelle Coombs
LSI (Avago)	Xingdong Dai, Min Huang, Anaam Ansari, Brian Burdick Venkatesh Avula*
Mentor Graphics	Arpad Muranyi, John Angulo, Fadi Deek, Chuck Ferry Thomas Groebli
Micron Technology	Randy Wolff
Qualcomm	Jaimeen Shah, Srinivasa Rao
Signal Integrity Software	Mike LaBonte, Walter Katz*, Todd Westerhoff, Michael Steinberger
Synopsys	Ted Mido, Scott Wedge, Kevin Cameron*, Rita Horner*
Teraspeed Consulting Group	Bob Ross*, Tom Dagostino, Scott McMorrow
Xilinx	Ravindra Gali
ZTE Corporation	(Shunlin Zhu)
Zuken	Michael Schaeder, Amir Wallrabenstein, Griff Derryberry Reinhard Remmert

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Continental Automotive	Catalin
CST	Stefan
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Pangeya	Edgar Aguirre
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SAE International	Chris Denham
Tabula	Ben Zhou*
Technische Universität Hamburg	Torsten Reuschel
Toshiba	Hiroyuki Ikegami*, Toshihiro Tsujimura*
University of Illinois	José Schutt-Ainé
Vitesse	Siris Tsang

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Meeting Number	Meeting Password
June 20, 2014	205 475 958	IBIS

For teleconference dial-in information, use the password at the following website:

https://ciscosales.webex.com/ciscosales/j.php?J=205475958

All teleconference meetings are 8:00 a.m. to 9:55 a.m. US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

OFFICIAL OPENING

The IBIS Open Forum Summit was held in San Francisco, California at the Moscone Center during the 2014 DAC conference. About 23 people representing 19 organizations attended.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.eda.org/ibis/summits/jun14/

Michael Mirmak welcomed everyone to the Summit, opening the meeting at 8:30AM. He thanked the event co-sponsor, the EDA Consortium. Michael asked all the participants to introduce themselves.

CHAIR'S STATUS REPORT

Michael Mirmak, Intel

Michael Mirmak began by showing how long versions of IBIS have been active before they were replaced by updated versions. Most versions have lived for more than a year. 12 BIRDs are currently open and most are package related, with the longest outstanding BIRD having been open for more than 3 years. Michael detailed the requirements needed to move to a 1-year release schedule. This is based on feedback from DesignCon regarding the 6-month update proposal being too short. He also detailed a date-based version numbering scheme, and combined membership and parser contribution fee structure for 2015.

Bob Ross pointed out that multiple parsers are supported by IBIS and also that the presentation has three separable proposals, each of which could be approved or rejected independently of the others. Walter Katz expressed agreement with the proposals presented. Michael concluded by stating that the proposals would be subject to formal Open Forum votes.

INTRODUCTION OF P2401 LSI-PACKAGE-BOARD STANDARD FORMAT

Genichi Tanaka, Renesas

Genichi Tanaka opened his presentation by stating that IEEE P2401 work had just started, with working group membership being entity-based, for advanced IEEE Standards Association members. Several Japanese companies are currently represented in the working group. The group was formed because sometimes LSI (large-scale integrated circuits), package, and board designers work independently, but coordination of their work is needed. The industry generally wants to have a shared format for exchanging information in these areas, to shorten design and production cycles. Product development phases are long, and sometimes miss market windows. Having IBIS model simulations at each stage is desirable, but simulations take more time at each stage as development progresses. Simulation under LPB would take place from product planning, through circuit design, layout and SI/PI/EMC checking.

LPB is JEITA's first formal international standard effort. The LPB approach contains five different formats within it, including netlist, geometry, project, component and rule, identified by leading letters (i.e., M-, N-, C-, R-, and G-format). The C- and G- formats are used by CAD/CAE teams, while the N-format is used by system designers.

N-format is netlist, using Verilog. The R-format covers design rules, and is constraint-based, including material characteristics and constraints. G-format covers geometries using XFL, while the C-format covers components, in its own unique language approach. IBIS would fall under the C-format.

Files can be modified throughout life cycle stages by different engineers. This format standardization avoids issues with human error.

The LPB group's objective is to have an IEEE standard by December 2015. The team's next meeting is in July, and the Summit participants were invited to join.

Walter Katz suggested that obtaining pinlists in computer-readable form is incredibly difficult. He also advised making the geometry format comprehensive rather than "light" as described in the presentation.

IBIS INTERCONECT BIRD

Walter Katz, Signal Integrity Software (SiSoft)

Walter Katz described the recent proposal to describe interconnects in IBIS and related specifications as being discussed in the IBIS Interconnect Task Group. He summarized IBIS-ISS (the IBIS Interconnect SPICE Subcircuits specification), noting that it was made possible with the kind support of Synopsys and their donation of the relevant HSPICE manuals. Walter provided an overview of the proposal so far, and the yet-to-be-resolved items, including the naming convention for "terminals" vs. nodes vs. ports. He also noted that the proposal as written distinguishes between die pads used for signals and power connections, as well as between pre-layout and post-layout IBIS files. Some discussions continue as to treatments for unused terminations and corners. Terminal treatments may be limited to post-layout. Next steps include creating refined IBIS and EBD BIRDs.

Corner treatments include impedance, speed, crosstalk corners (e.g., for a 27 corner model), with other models to cover statistical variations. Walter noted that the IBIS document assumptions about the arrangement of capacitance, resistance, and inductance in a package are not noted by rules but only by a diagram. As a result, simulators may not make common assumptions on the arrangement of these terms.

Bob Ross suggested that a key problem is the "mix-and-match" model, where one file is typical, but includes multiple corner subcircuits. Walter replied that a very classical package would have the same via structure at pin/ball, with common trace width, impedance, etc. Only the length varies, so a single circuit is usable here. He suggested that the biggest issues in interconnect modeling today are loss and discontinuities affecting loss (e.g., ILD).

David Banas asked whether IBIS will avoid "the C_comp debacle", where a parameter is ordered contrary to the corner of the model's behavior. Walter noted that corner names won't be checked for order, and that names like "fast" or "slow" might be better. David replied that there

might be objections to using speed as a naming convention, as buffer and package behaviors may not vary in intuitive ways with temperature, etc.

IBISCHK5/6 SPECIFICATION DOCUMENT UPDATE

Bob Ross* and Mike LaBonte**, Teraspeed Consulting Group*, SiSoft**

Bob Ross summarized how the IBIS Quality Task Group has produced a guide to the assumptions and output messages used by the ibischk parser. He noted how the parser specification is organized, with message categories and per-module descriptions for the provided code and outputs. Numbered messages are provided, to enable easy identification of message types, but not all tools support the numbered messages today. The "Note" output type is only being used for non-monotonic concerns today.

Over 1200 unique messages are now available and supported. The ibischk5 draft document is not yet ready for upload, chiefly out of concern that the index of errors may be as long as the rest of the document contents.

Michael Mirmak asked about issues outside the standard, for example, the maximum value of C_comp capacitance before a warning is generated. Bob suggested that ibischk generates between 20 and 50 such messages. Waveform matching is one major such area. C_comp checking and maximum current checking are others.

ELECTION OF OFFICERS

Bob Ross and David Banas acted as returning officers to accept nominations and votes. The current officers had already been nominated and indicated their willingness to serve an additional term. Bob and David called for additional nominations from the attendees. No other nominations were received. The nominated officer slate was:

Michael Mirmak - chair Lance Wang - vice-chair Randy Wolff - secretary Mike LaBonte - webmaster Mike LaBonte - postmaster Anders Ekholm - model librarian

Walter Katz moved to approve the slate by acclimation. Venkatesh Avula seconded the motion. The motion carried without objection.

IBIS FILE INSPECTION USING IBISINF - A BASIC UTILITY FOR THE 80/20 RULE

Michael Schaeder, Zuken Presented by Bob Ross, Teraspeed Consulting Group

Bob Ross presented material originally delivered at the European IBIS Summit, on behalf of Michael Schaeder. The ibisinf tool generates quick synopses of selected models, rather than forcing the user to search through and edit a large file; these include the load conditions, parameters at corners, and the like. The tool was originally on the Zuken website, but it has been donated to IBIS recently, and updated to cover ibischk 5.1.4.

Output can be redirected to text file output, and the tool itself could be integrated with ibischk.

Walter Katz asked why the presentation refers to the 80/20 rule. Bob suggested that this was because the tool helps the user easily obtain 80% of the data, but the final 20% takes more digging.

Walter asked about pad vs. pin measurements for V-T tables and Ramp data. The group's consensus response was that the buffer pad is the measurement point for all V-T data. C_comp is measured looking into the buffer at the die pad. Walter asked about the biggest contributor to C_comp. David Banas and Bob noted that the ESD structures, not on-die interconnect, contribute most to C_comp.

Walter noted that I-V and V-T curves don't work well for 10 GHz signaling. A straight-line risetime at the maximum frequency for an [External Model] may not be appropriate, as this would be a non-band limited input signal to the IBIS model. He suggested that a 1/e squared waveform shape would be more appropriate as a stimulus (aka exponential or Gaussian or Bessel function). The shape of the input must be limited. Bob challenged this, as the stimulus for a SPICE circuit could be pre-processed.

SOLVING RECEIVER ELECTRICAL TEST CHALLENGES USING IBIS AMI MODELING TECHNIQUES

Venkatesh Avula, Avago

Venkatesh Avula described a simple topology that can use IBIS-AMI models: a PCIe device link connected through miniSAS connectors. The challenge is to determine the output at the receiver without probing in the laboratory. MiniSAS is a non-standard form factor for PCIe, and the link uses retimers, which are also non-standard. A compliance test board is needed, which does not exist for miniSAS PCIe links. The problem is to determine the worst-case channels and performance based upon compliance testing, to see if the design satisfies interoperability requirements. The solution is to create an IBIS-AMI model of the stress signal generator used for compliance testing. This model can include many factors. For PCIe, such a model can be used with SigTest, the standard test software for PCIe, which includes equalization modeling. Venkatesh showed what such a model would look like, including the controls and model-specific parameters required. Correlation is good, though the receiving IBIS-AMI model must correlate to actual receiver SerDes IC over PVT for best results.

David Banas asked about the transmitter parameters used. These include SSC jitter, HF jitter, periodic jitter, de-emphasis, etc.

THE BACKCHANNEL CROSSROADS

Ken Willis, Ambrish Varma, Kumar Keshavan, and Brad Brim, Cadence Design Systems Presented by Brad Brim, Cadence Design Systems

Brad Brim summarized the adaptive backchannel communication proposal defined in BIRD147. The fundamental difference between BIRD147 and the SiSoft proposal is the use of a separate file, called a BCI file, to provide guidance on how to perform the training. This file provides one location for architectural information in common for the models to refer to, where the tool simply passes TX and RX information back and forth between the models. This avoids IBIS Open Forum involvement in BCI file generation. IBIS as an organization can be involved but doesn't

have to be. The BCI approach also enables private (secret) BCI files to be passed back and forth. These could be encrypted and/or included in the DLL. Brad contrasted this to the SiSoft proposal by drawing attention to "hard-coding" of parameters, suggesting this approach has not been successful in the past.

Kevin Cameron suggested looking at IP-XACT, an Accellera XML specification, as an alternative way of exchanging this information, which can support both a single file database and a multi-file database.

CO-OPTIMIZATION OF SERDES CHANNELS USING AMI MODELING

Walter Katz, Signal Integrity Software (SiSoft)

Walter Katz provided an overview of the SiSoft adaptive equalization proposal, which he called "co-optimization". He noted that the primary concern for most system engineers is optimizing the output of the receiver eye when the transmitter and receiver can communicate about their respective settings. The problem to solve is one of simultaneous adjustment between the transmitter and receiver. This relies on training, which may not exist for all SerDes interfaces. Simulation can be used to explore different metrics/targets for optimization of settings.

IBIS still has a problem, in that channel training is not supported. Co-optimization can target many metrics, including eye height, eye width, eye area and power as well. Using additional Reserved Parameters in IBIS-AMI, this optimization proposal supports both Init and GetWave, and assumes tap configuration will be published for the transmitter, with Reserved Parameters for the RX. Private training is supported, and the proposals allow the use of existing TX DLLs and reporting mechanisms.

Brad Brim and Walter then formed a panel for discussion of the two proposals, including the major differences. These include whether the individual parameters and/or description files require IBIS approval, and whether existing transmitter algorithmic models needed modification or not.

IBIS SUMMARY DOCUMENTS

Bob Ross, Teraspeed Consulting Group

Bob Ross provided an overview of several official and unofficial documents that help to explain aspects of the specification. These include "tree" documents on available keywords, subparameters, and features, plus an evolution document that shows the hierarchy between keywords (examples are given showing which keywords are "top-level" and which are not).

Separate documents show the IBIS-AMI parameter syntax, including what the parameter structure is. The Reserved Parameters are classified by their Usages, Types, and Formats.

Bob recommended these as useful references for development and for specification understanding. Michael Mirmak suggested that these would help model makers understand exactly what keywords and features are required for a given device, to select the version of IBIS appropriately. Brad Brim suggested that additional guidance is needed on power-aware buffer modeling and how this interacts with IBIS-AMI. Cookbook updates may be needed here.

Pierre Dermy asked about where a model author should begin to learn about IBIS extraction. Several participants suggested reading the cookbook. Pegah Alavi mentioned an LVDS and IBIS white paper originally from National, now reissued by Texas Instruments, as a good reference.

CONCLUDING ITEMS

Michael Mirmak thanked EDAC, the presenters, organizers, and attendees for their support in making the Summit possible.

The meeting concluded at approximately 4:30 PM.

NEXT MEETING

The next IBIS Open Forum teleconference will be held June 20, 2014 from 8:00 a.m. to 10:00 a.m. US Pacific Time.

NOTES

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This meeting was conducted in accordance with ANSI guidance.

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To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

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clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs as well as tschk2 parser BUGs. The BUG Report Form for ibischk resides along with reported BUGs at:

http://www.eda.org/ibis/bugs/ibischk/ http://www.eda.org/ibis/bugs/ibischk/bugform.txt

The BUG Report Form for tschk2 resides along with reported BUGs at:

http://www.eda.org/ibis/tschk_bugs/ http://www.eda.org/ibis/tschk_bugs/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/ http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eda.org/ibis

Check the IBIS file directory on eda.org for more information on previous discussions and results:

http://www.eda.org/ibis/directory.html

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IBIS – SAE STANDARDS BALLOT VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

		Standards				
Organization	Interest Category	Voting Status	April 25, 2014	May 14, 2014	May 23, 2014	June 5, 2014
Agilent Technologies	User	Active	Х	Х	Х	Х
Altera	Producer	Active	Х	-	Х	Х
ANSYS	User	Inactive	-	-	-	-
Applied Simulation Technology	User	Inactive	-	-	-	-
Cadence Design Systems	User	Inactive	Х	-	-	Х
Ericsson	Producer	Inactive	-	Х	-	-
Infineon Technologies AG	Producer	Inactive	-	-	-	-
Intel Corp.	Producer	Active	Х	Х	Х	Х
IO Methodology	User	Inactive	-	-	Х	-
LSI (Avago)	Producer	Inactive	-	-	-	Х
Mentor Graphics	User	Active	Х	Х	Х	-
Micron Technology	Producer	Active	Х	Х	Х	-
Qualcomm	Producer	Inactive	-	-	Х	-
Signal Integrity Software	User	Active	Х	-	Х	Х
Synopsys	User	Inactive	-	-	-	Х
Teraspeed Consulting	General Interest	Active	Х	-	Х	Х
Xilinx	Producer	Inactive	-	-	-	-
ZTE	User	Inactive	-	-	-	-
Zuken	User	Inactive	-	Х	-	-

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
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