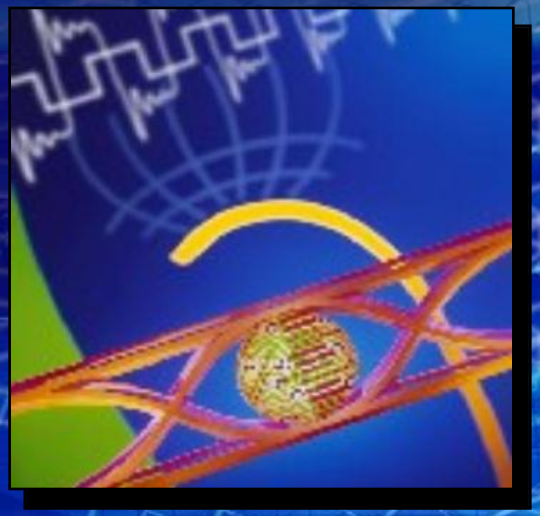
Should IBIS Support Eye Mask Definitions?



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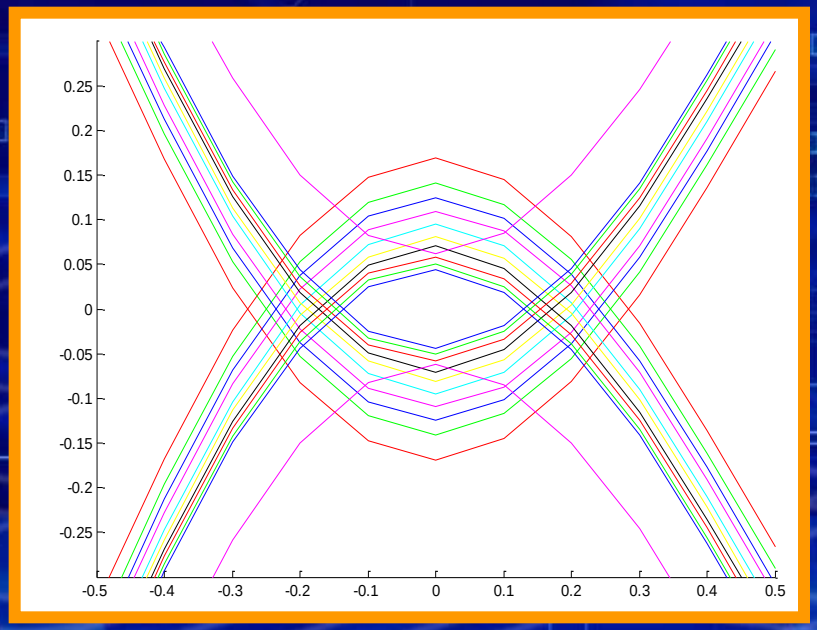
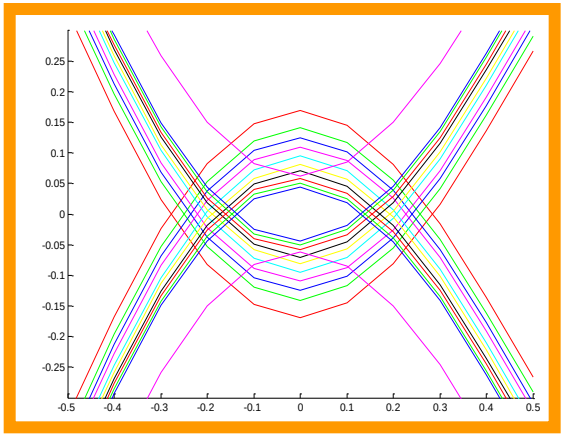


Arpad Muranyi

Mentor Graphics®

Should IBIS Support Eye Mask Definitions?



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1. What are eye diagrams and eye contours?
2. What is in the IBIS specification?
3. Why would eye masks be useful?
4. Philosophical questions
5. Conclusion

What are eye diagrams and eye masks?

- A Google search for "`eye mask setup hold`" gave me a link to:

Advanced Signal Integrity for High-Speed Digital Designs
By Stephen H. Hall, Howard L. Heck

http://books.google.com/books?id=IdlnVkxjw7YC&lpg=SA10-PA131&ots=wMNjMztDBM&dq=eye%20mask%20setup%20hold&pg=SA10-PA130#v=onepage&q=eye%20mask%20setup%20hold&f=false

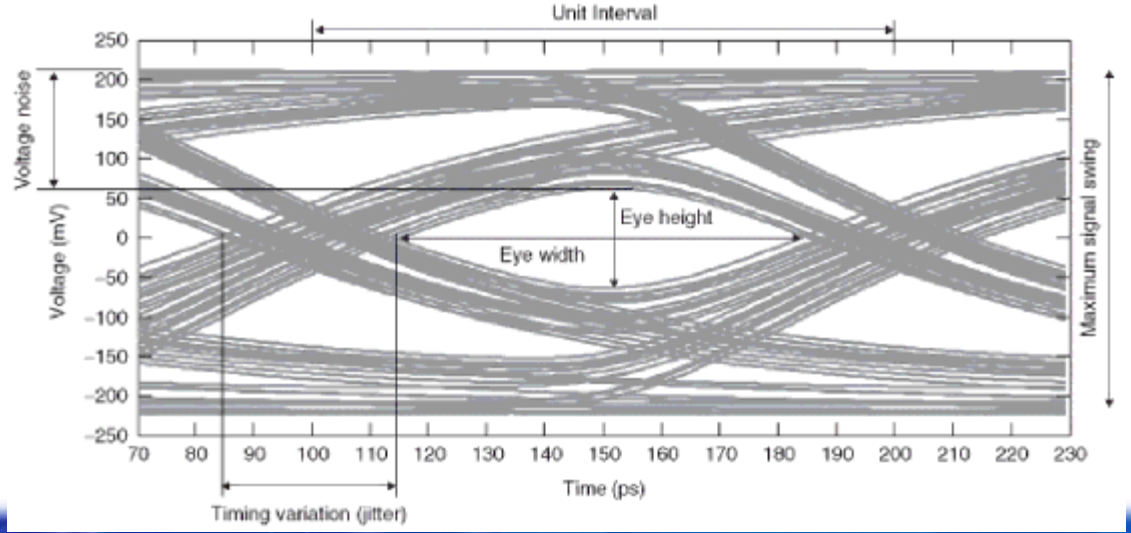
- This book contains good definitions for eye diagrams and eye masks, as shown on the next two pages (red underline emphasis added)

13.1 EYE DIAGRAM

Most high-speed designs use the eye diagram to evaluate system performance. We show an example eye diagram for a 10-Gb/s 100-bit data sequence in Figure 13-1. An eye diagram is constructed by slicing the time-domain signal waveform into sections that are a small number of symbols in length, and overlaying them. The horizontal axis of the eye diagram represents time and is typically one or two symbols wide, while the vertical axis represents the amplitude of the signal. Figure 13-2 illustrates the eye diagram construction process for both a "perfect" eye and one that is distorted by losses and/or reflections.

As the figures show, distortion of the signal causes the data eye to close. Conceptually, we want the eye to be as "open"as possible, as a larger eye opening implies that we have more margin to the voltage and timing requirements. From a quantitative standpoint, the minimum height and width of the data at the receiver are key metrics for evaluating link performance. The eye must be wide enough to provide adequate time to satisfy the setup and hold requirement of the receiver, and have sufficient height to ensure that the voltage levels meet υ_{ih} and υ_{il} requirements in a system that may possess multiple sources of noise. This allows the receiver to resolve the input signals successfully into digital values.

Figure 13-1 Example received eye diagram for a 10-Gb/s 100-bit data sequence.



Later on, the same chapter says the following:

The mask represents a forbidden region that the actual eye must not cross, and it includes the receiver setup and hold window and voltage specs, and all jitter and noise terms.

What is in the IBIS specification?

- **Vinh, Vinl under [Model]**
- **Enhanced versions of the above under [Model Spec]**

```
|               Vinh              Input voltage threshold high
|               Vinl              Input voltage threshold low
|               Vinh+             Hysteresis threshold high max Vt+
|               Vinh-             Hysteresis threshold high min Vt+
|               Vinl+             Hysteresis threshold low max Vt-
|               Vinl-             Hysteresis threshold low min Vt-
```

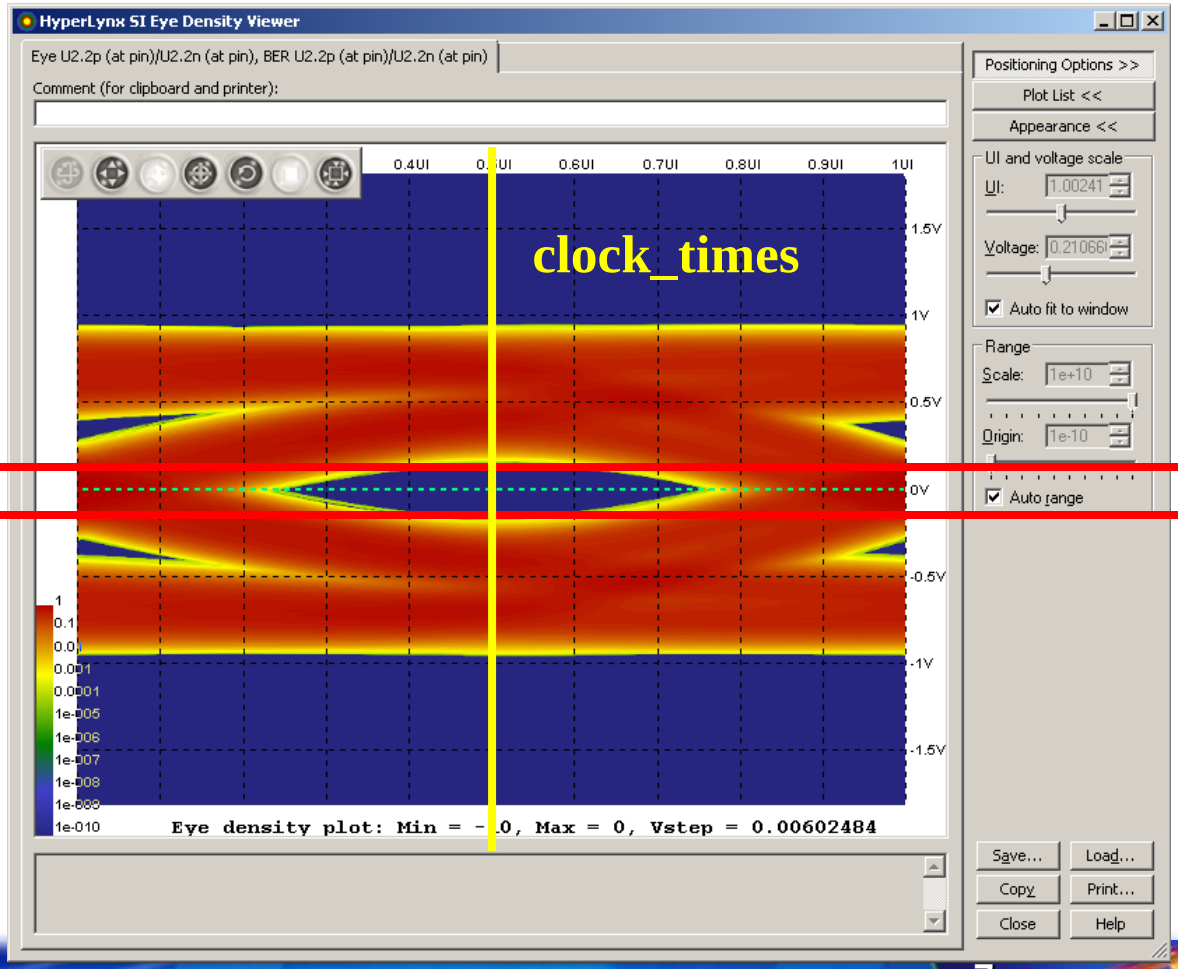
- **More stuff under [Receiver Thresholds]**

```
|     Keyword:  [Receiver Thresholds]
|    Required:  No
|  Sub-Params:  Vth, Vth_min, Vth_max, Vinh_ac, Vinh_dc, Vinl_ac, Vinl_dc,
|               Threshold_sensitivity, Reference_supply, Vcross_low,
|               Vcross_high, Vdiff_ac, Vdiff_dc, Tslew_ac, Tdiffslew_ac
```

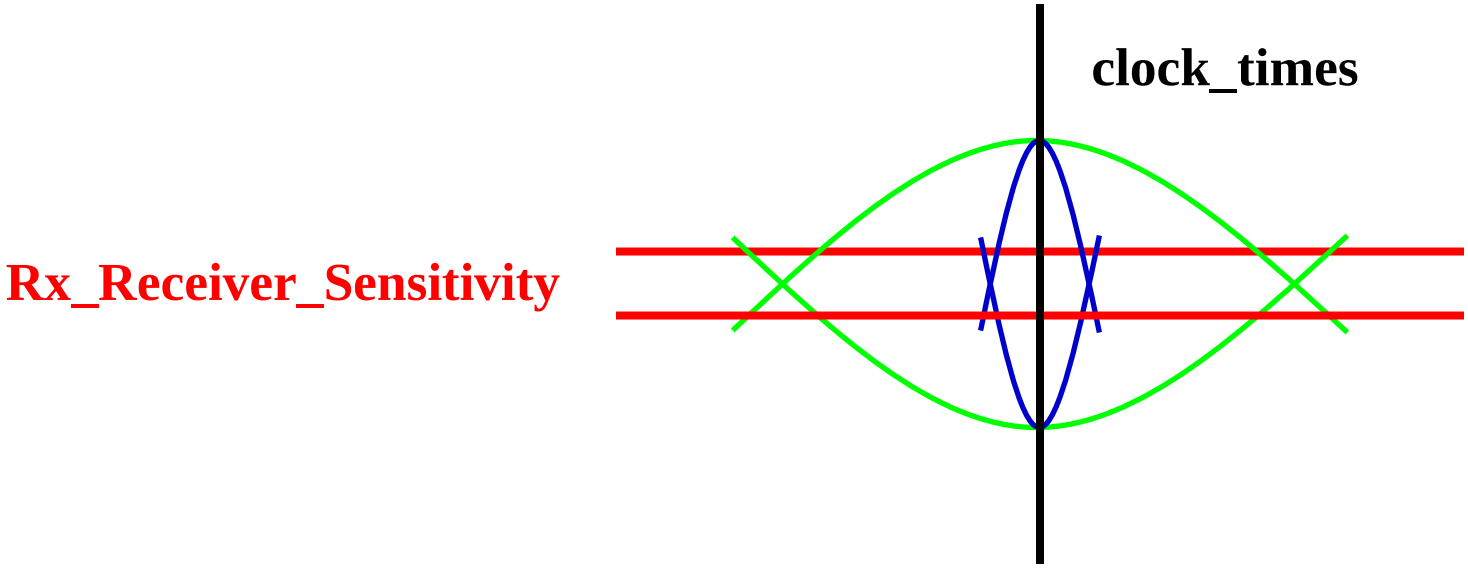
- **Rx_Receiver_Sensitivity in IBIS-AMI**
- **There is nothing in the IBIS specification to define the setup and hold requirements for an input**

The IBIS-AMI Rx_Receiver_Sensitivity

Rx_Receiver_Sensitivity tells the EDA platform the voltage needed at the receiver data decision point to ensure proper sampling of the equalized signal.



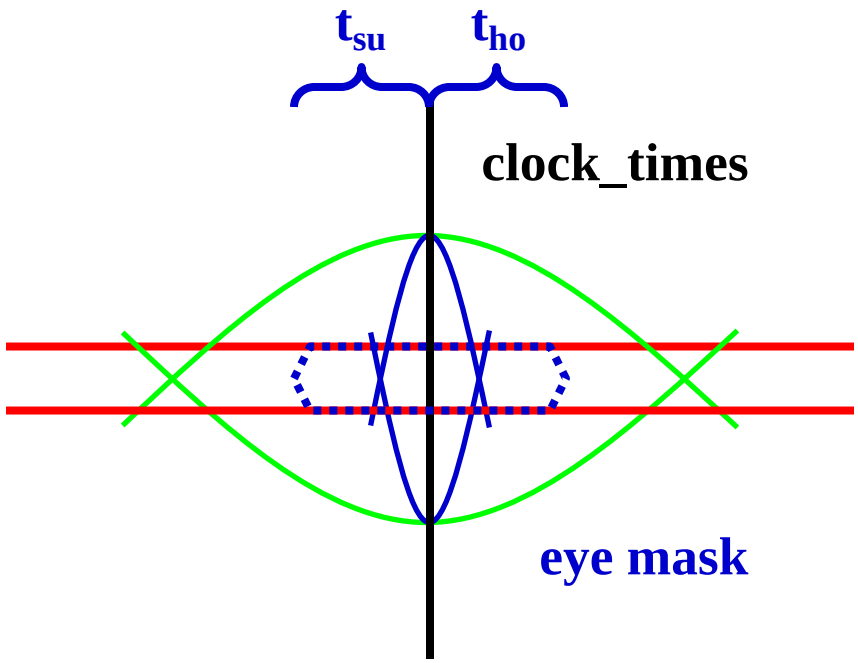
Which of these eye openings will work?



Not knowing the setup and hold requirements of the next input stage, both of these eye contours should pass, since they are both larger than the voltage levels defined by Rx_Receiver_Sensitivity

If we had an eye mask, we would know…

Rx_Receiver_Sensitivity



The eye mask includes the setup and hold requirements of the next input stage and reveals that the narrow blue eye contour is failing

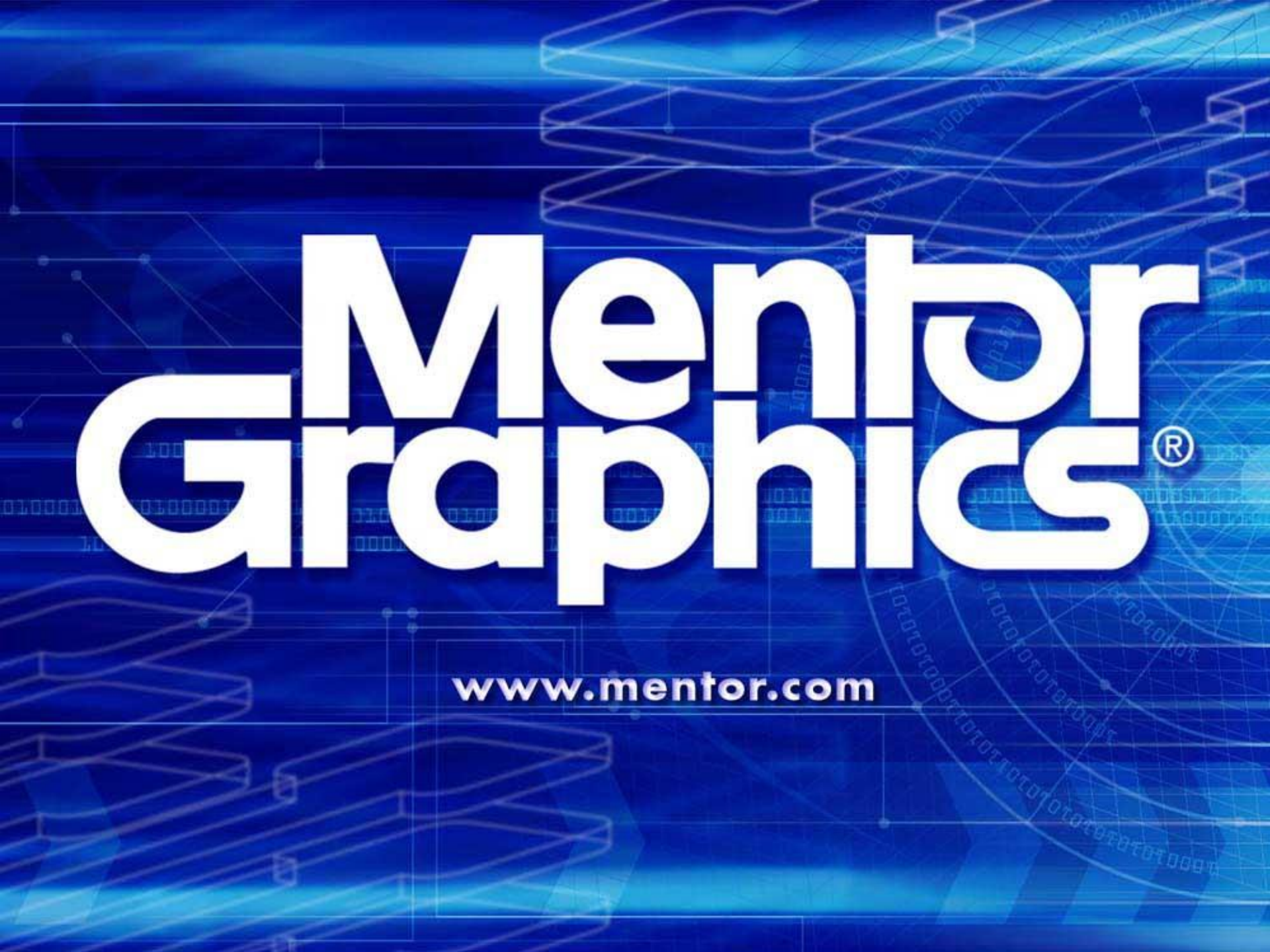
Philosophical questions

- **There are many predefined eye masks in various bus specifications, why should we include them in the IBIS model?**
  - Vinh and Vinl are not different from this, yet we still included them in the IBIS [Model]

    for example: TTL levels are 0.8 and 2.0 volts, yet most "plain vanilla" IBIS models included Vinl = 0.8 and Vinh = 2.0 in the [Model]
- **The eye mask may be used to describe a bus specification's requirements, or the actual behavior of the device**
  - this is how Vinh and Vinl works also
- **Would it make sense to add t_{su} and t_{ho} to complement Vinh and Vinl for legacy models?**
  - Input model types don't have clock inputs, so setup and hold could not influence the output state of the Rx (logic '1', '0', or 'X')
  - but it would still be useful in telling the EDA tool how to evaluate the waveforms
  - this is how Rx_Receiver_Sensitivity is used in AMI simulations

Conclusions

- It seems that and eye mask definition would be useful in the AMI portions of the IBIS specification
- We might want to consider to extend the legacy portions of the IBIS specifications with setup and hold parameters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