IBIS PDN Feature Studies

Randy Wolff – Micron Technology

Lance Wang – IO Methodology

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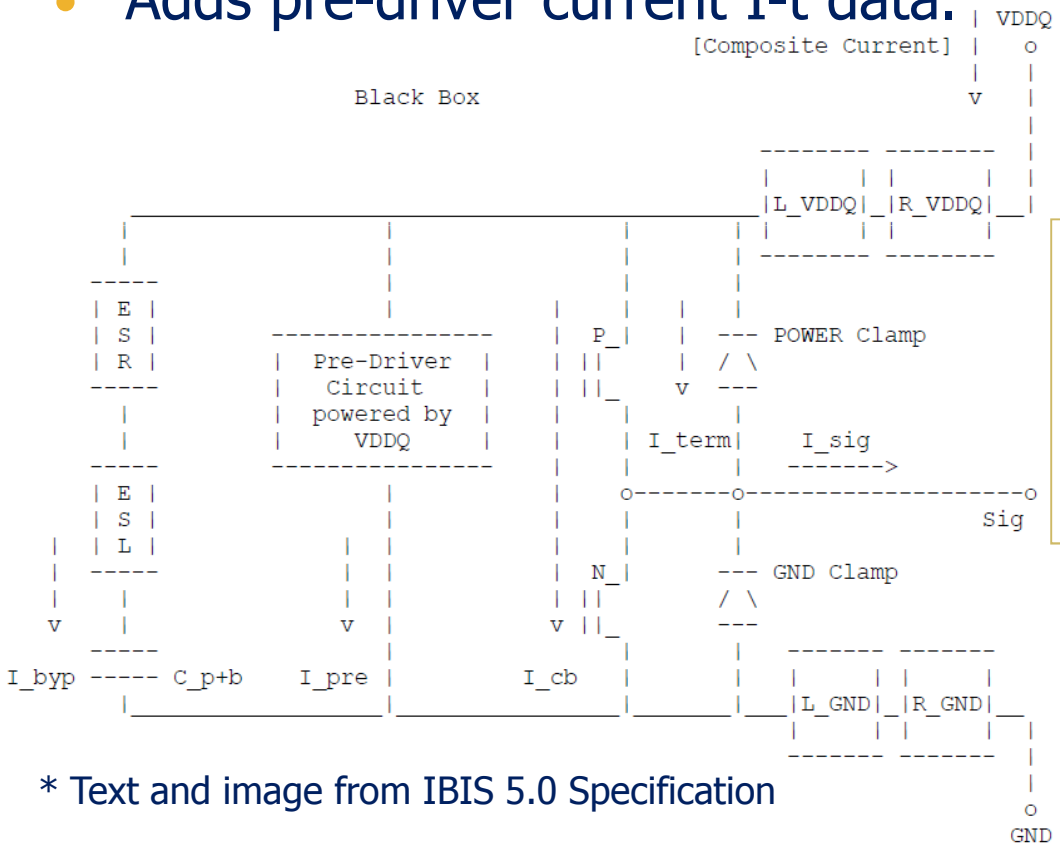
based on 2011 European IBIS Summit presentation and updates

Introduction

- [Composite Current] table data – added to IBIS 5.0 through BIRD95.
- [ISSO PD] and [ISSO PU] table data – added to IBIS 5.0 through BIRD98.
- Simulation done with two tools (available to authors) that include full/partial support for BIRD95 and BIRD98 in current releases.
- IBIS 5.0 DDR3 model developed and used to compare simulation tools to golden SPICE model results.

[Composite Current]

- Describes the shape of the rising and falling edge current waveforms from the power reference terminal of the buffer*.
- Adds pre-driver current I-t data.

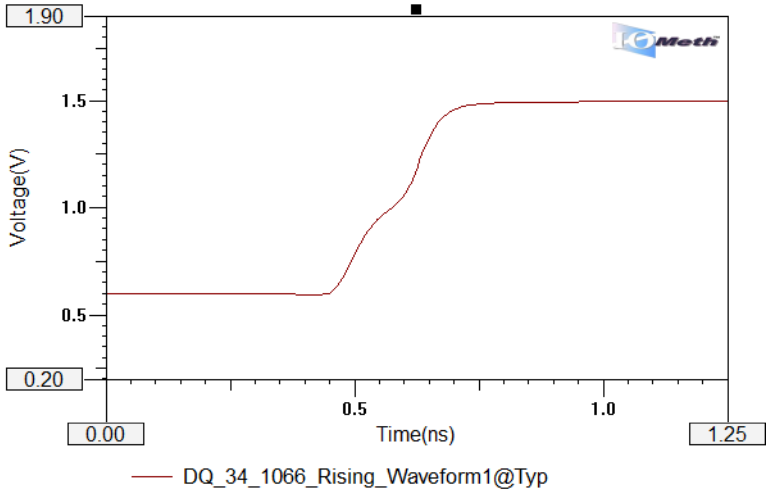


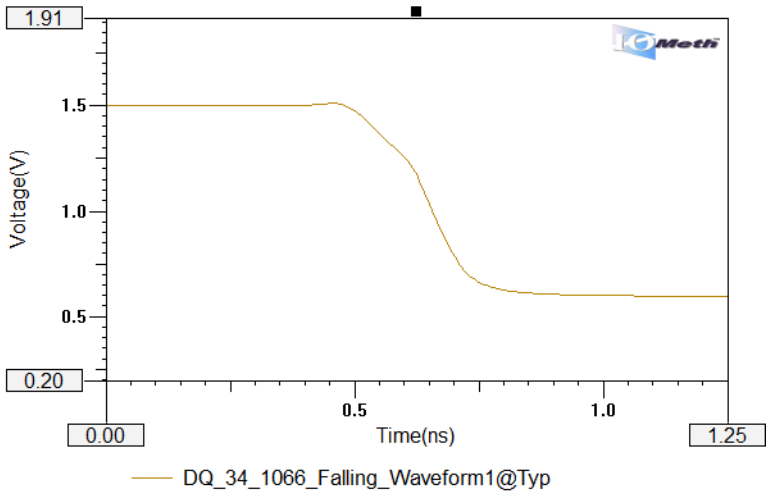
I_byp	- Bypass current
I_pre	- Pre-Driver current
I_cb	- Crow-bar current
I_term	- Termination current (optional)
L_VDDQ	- On-die inductance of I/O Power
R_VDDQ	- On-die resistance of I/O Power
L_GND	- On-die inductance of Ground
R_GND	- On-die resistance of Ground
C_p+b	- Bypass + Parasitic Capacitance
ESR	- Equivalent Series Resistance for on-die Decap
ESL	- Equivalent Series Inductance for on-die Decap

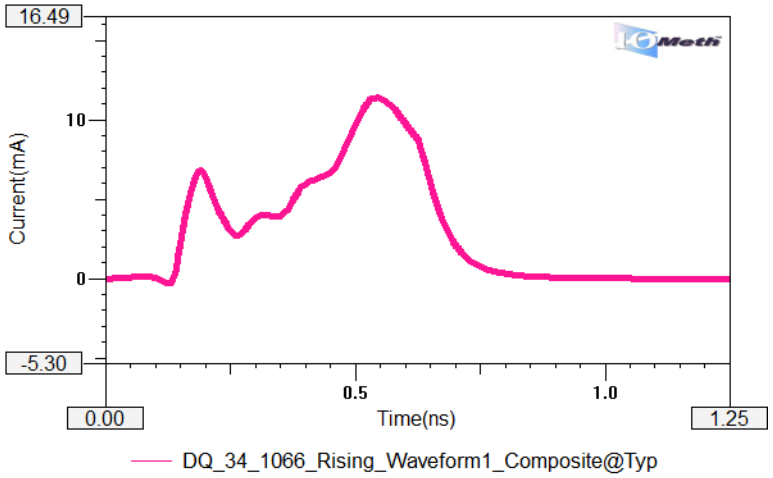
* Text and image from IBIS 5.0 Specification

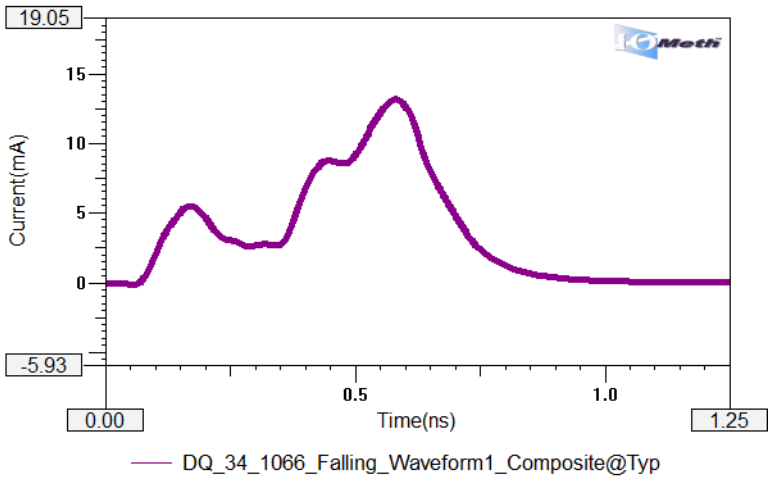
[Composite Current] Data

- Load = 50 ohms to [Pullup Reference]



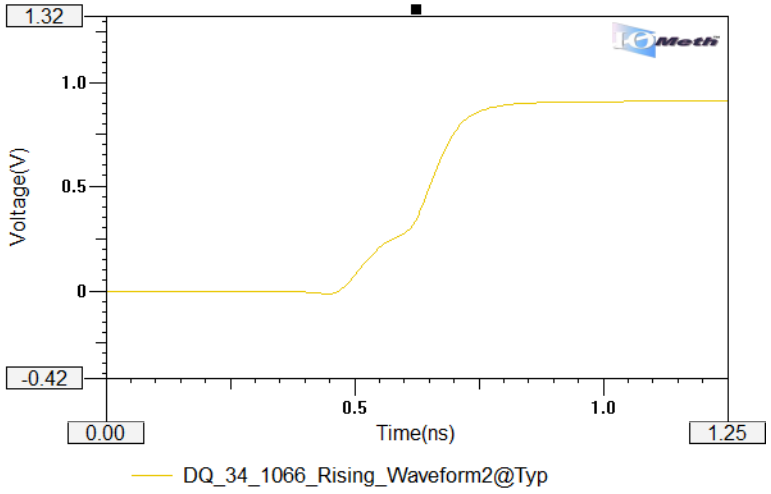


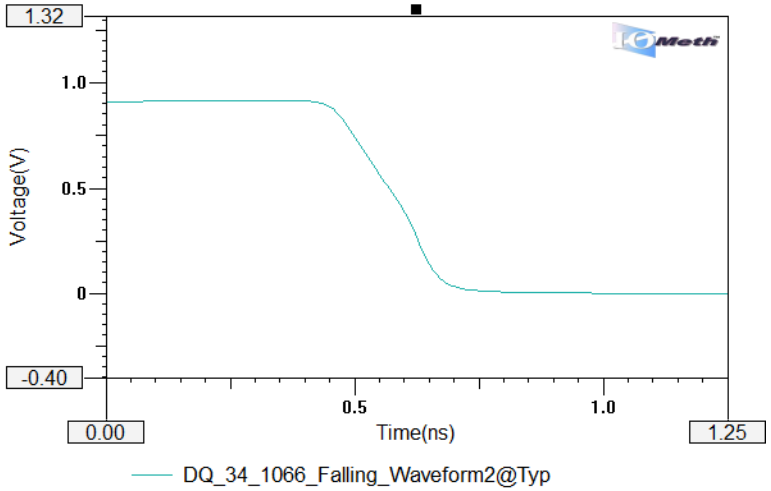


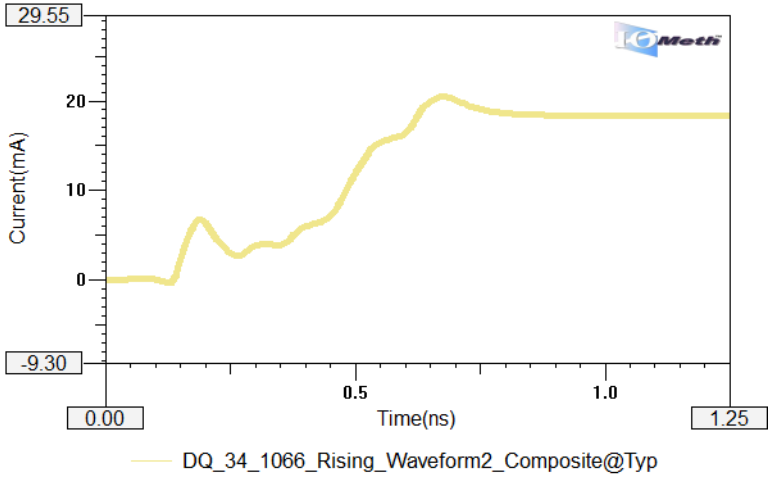


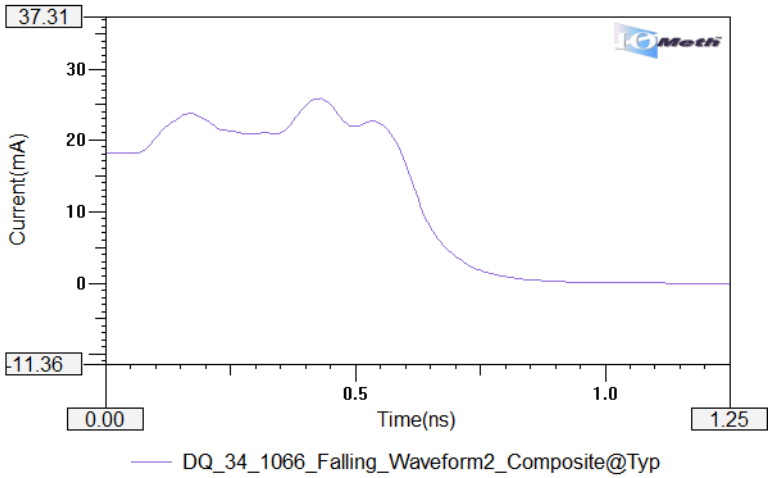
[Composite Current] Data

- Load = 50 ohms to [Pulldown Reference]



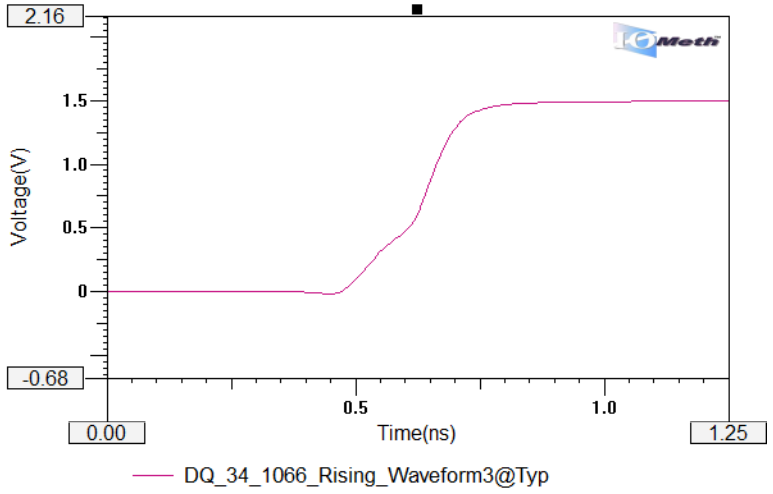


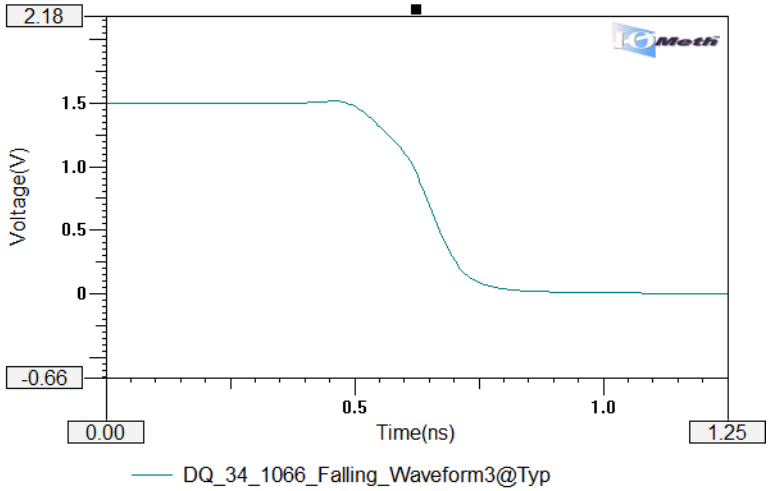


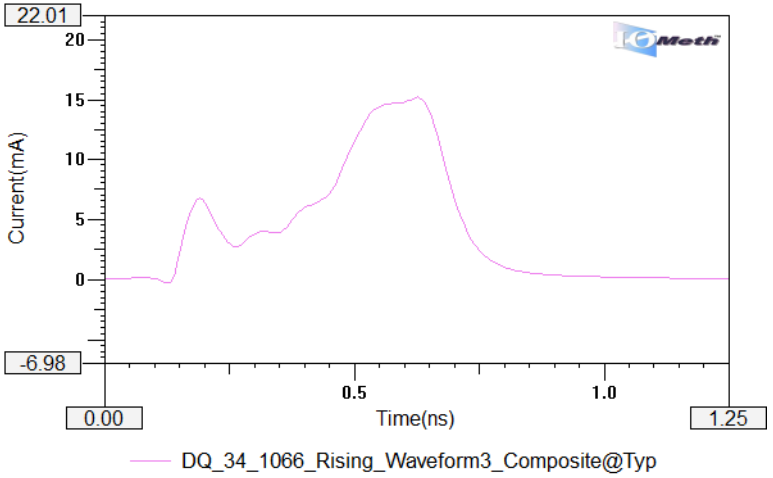


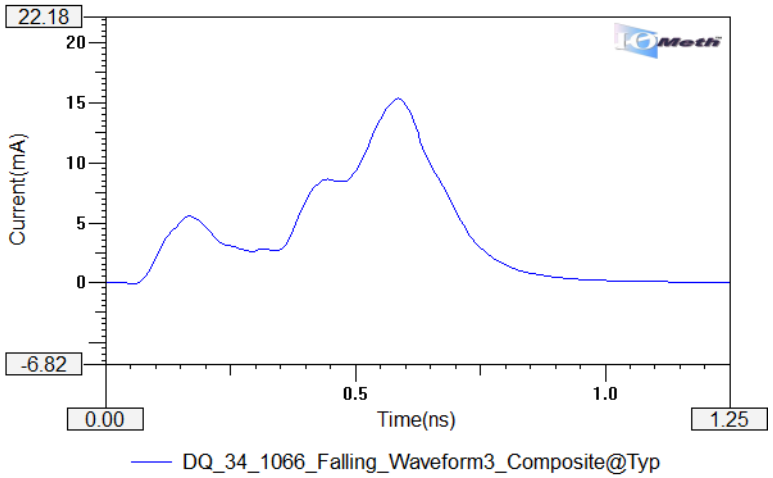
[Composite Current] Data

- Load = 1E9 ohms to [Pulldown Reference] (No load)







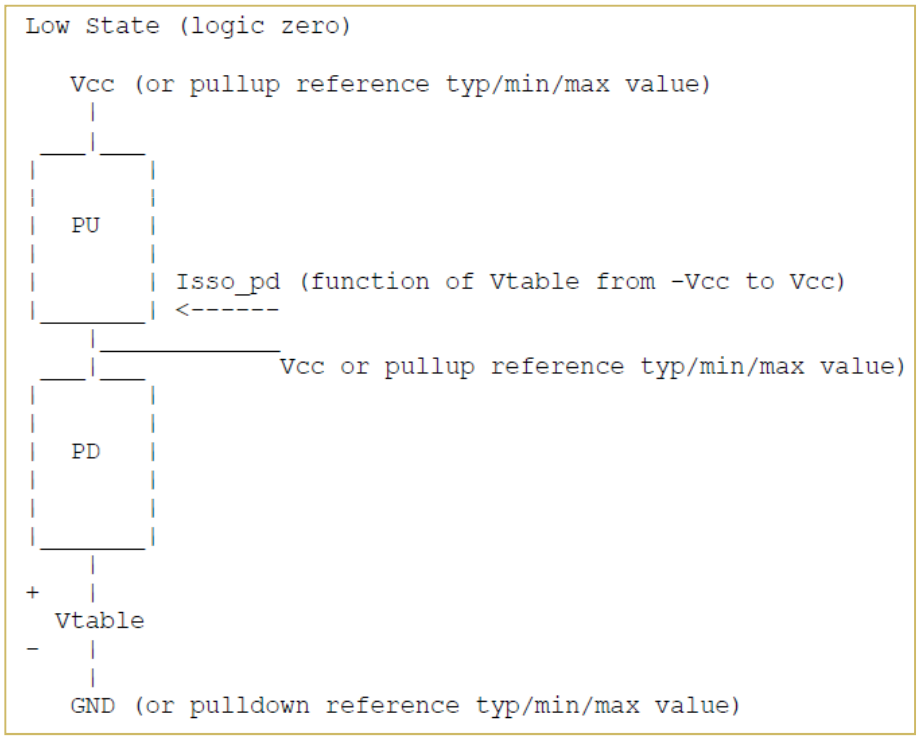


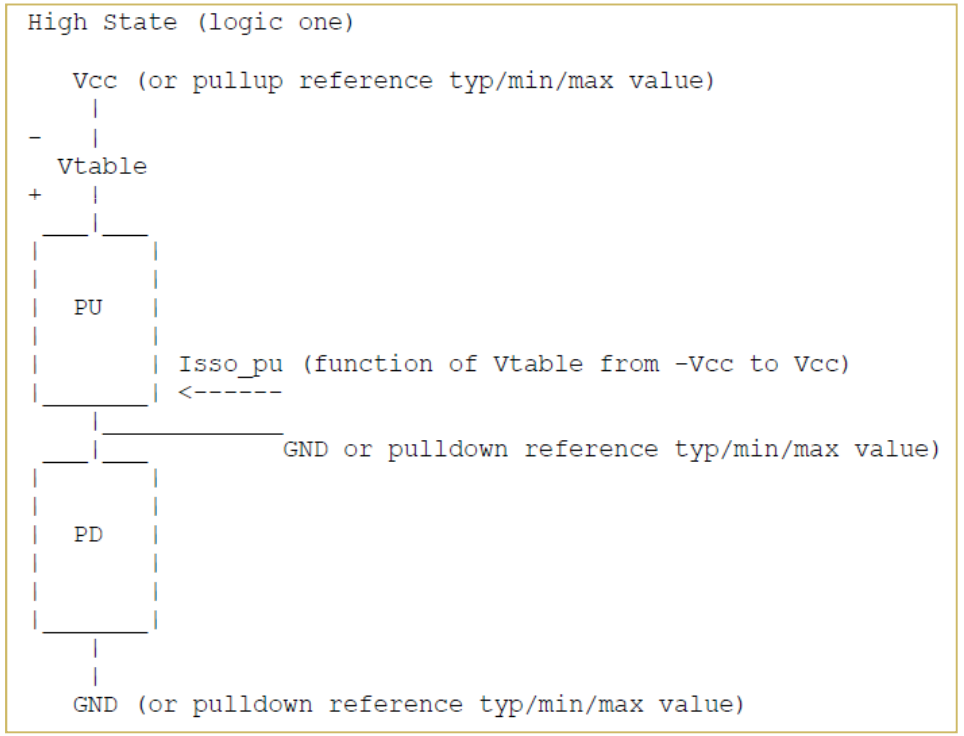
[Composite Current] Observations

- Significant 'dead time' must be added to beginning of V-t curves to correlate with time of pre-driver current.
  - This limits model switching rate – encourages overclocking.
  - Example model originally DDR3-1066, now DDR3-800.
- [Composite Current] only includes [Pullup Reference] supply current.
  - Algorithms can only assume that [Pulldown Reference] current is equal to [Pullup Reference] current.
  - Is this valid?

[ISSO PU] & [ISSO PD]

- Data tables define the effective current of the pullup/pulldown structures of a buffer as a function of the voltage on the pullup/pulldown reference nodes*.
- Adds modeling of the gate modulation effect on driver current (I_{DS} vs. V_{GS}).

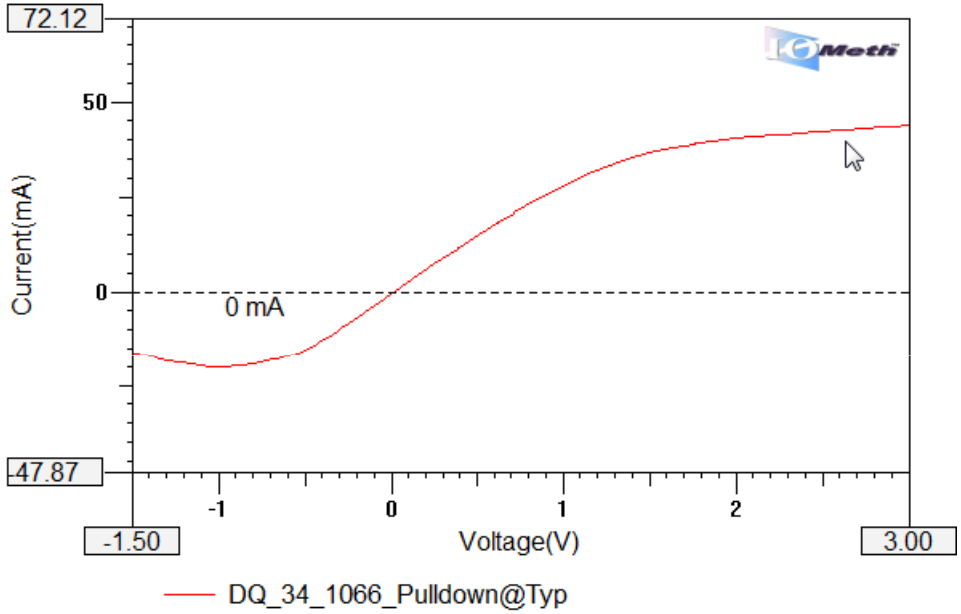




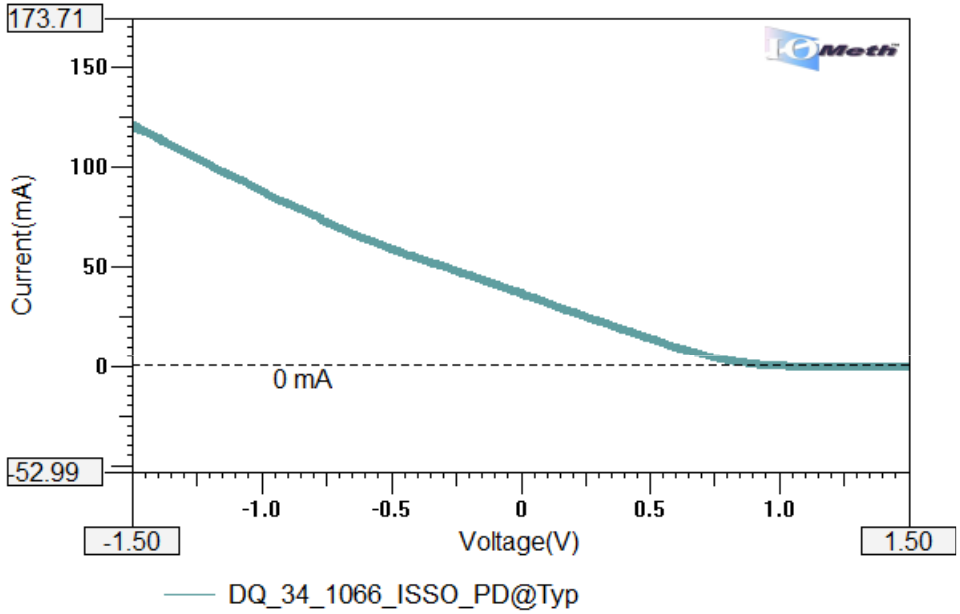
* Text and image from IBIS 5.0 Specification

[ISSO PD] Data

Pulldown



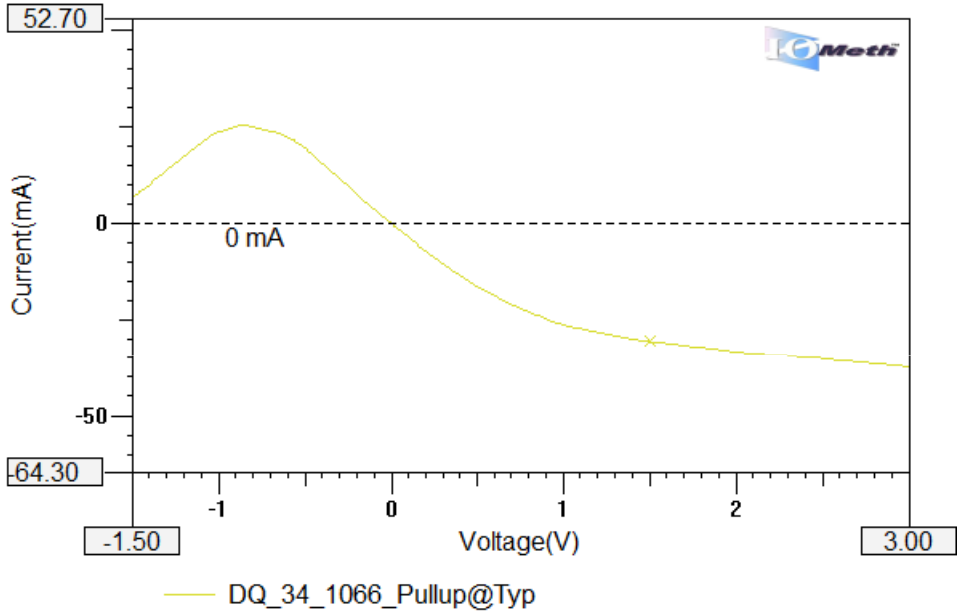
ISSO PD



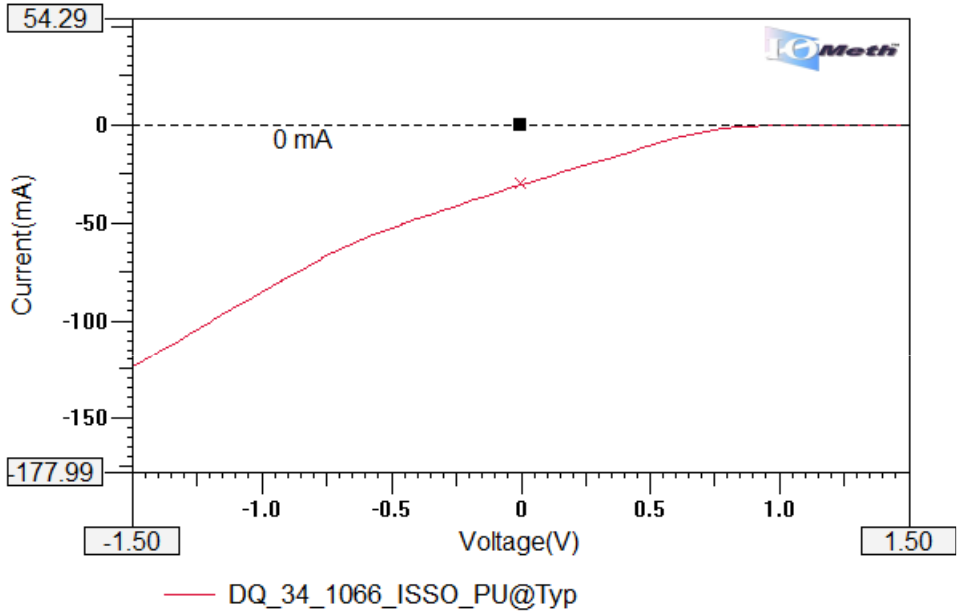
Name: DQ_34_1066_Pulldown@Typ Type: Crossing Y		Name: DQ_34_1066_ISSO_PD@Typ Type: Crossing Y	
X	Y	X	Y
1.500000e+000	3.697962e-002	0.000000e+000	3.713536e-002

[ISSO PU] Data

Pullup



ISSO PU



Name: DQ_34_1066_Pullup@Typ Type: Crossing Y		Name: DQ_34_1066_ISSO_PU@Typ Type: Crossing Y	
X	Y	X	Y
1.500000e+000	-3.012817e-002	0.000000e+000	-3.016485e-002

[ISSO PU] & [ISSO PD] data in IBISCHK5

- IBISCHK5 checks that Isso_pd(0)=Ipd(Vcc) and Isso_pu(0)=Ipu(Vcc).
  - Pulldown is 0.42% different, Pullup is 0.12% different (typ).
  - IBISCHK5 issues a WARNING. Is it too sensitive?
    - WARNING - Model DQ_34_1066: Minimum ISSO_PD current (0.031A) at 0V does not match Pulldown current (0.031A) at reference (1.425V)
- IBISCHK5 checks that Isso_pd(Vcc)=0 and Isso_pu(Vcc)=0.
  - Should a value of X nA cause a WARNING?
    - WARNING - Model DQ_34_1066: Minimum ISSO_PD current (-0.000A) at Pullup reference (1.425V) - table value (1.425V) is non-zero
  - Note that the number of significant digits reported in the WARNING messages are not enough to indicate a problem.

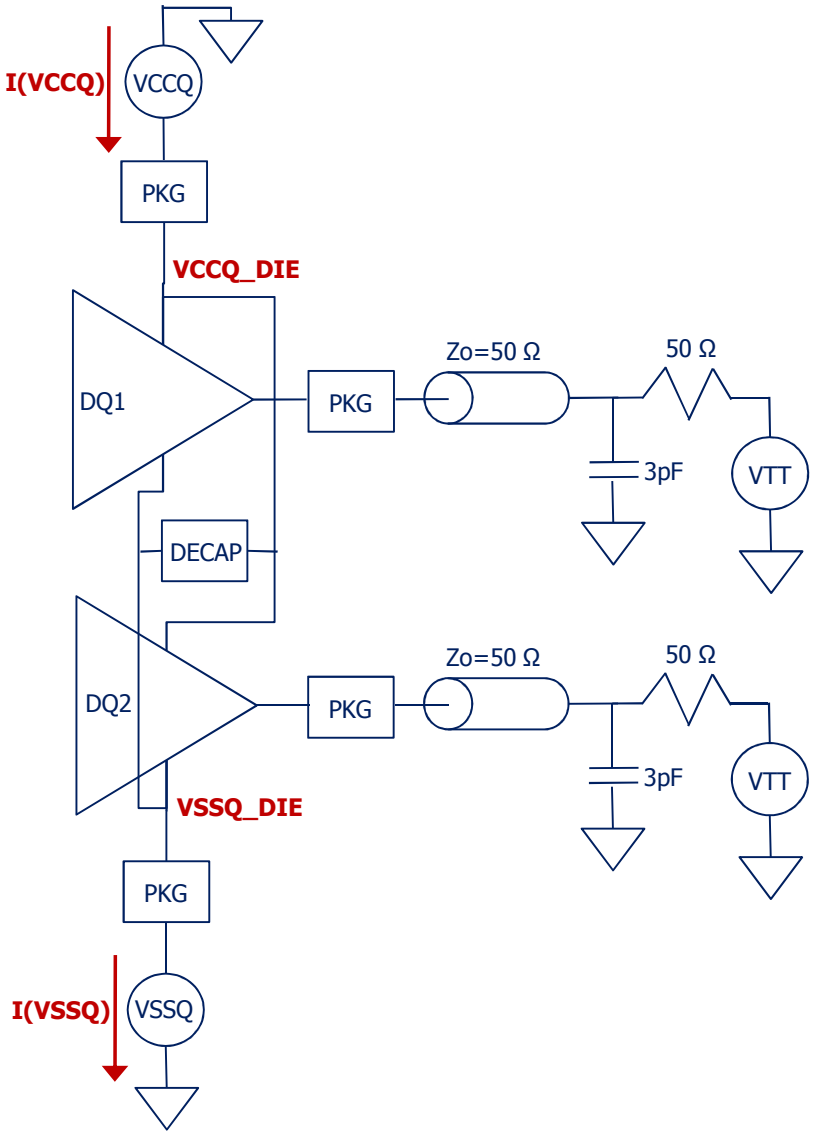
Using [ISSO PU] & [ISSO PD] data

- Modulation coefficients can be calculated from the data (Ksso_pu & Ksso_pd).
  - What is the Ksso_pu value for a 50mV drop in Vcc?
    - Ksso_pu(Vtable_pu) = Isso_pu(Vtable_pu)/Isso_pu(0)
    - Ksso_pu(50mV) = Isso_pu(50mV)/Isso_pu(0)
    - Ksso_pu = -28.1067mA/-30.16485mA = 0.9318
  - What is the Ksso_pd value for a 50mV rise in Vss?
    - Ksso_pd(Vtable_pd) = Isso_pd(Vtable_pd)/Isso_pd(0)
    - Ksso_pd(50mV) = Isso_pd(50mV)/Isso_pd(0)
    - Ksso_pd = 34.83905mA/37.13536mA = 0.9382
  - For this example, a 50mV drop in supply voltage translates to a ~7% reduction in the K scale factor.

Simulation Results

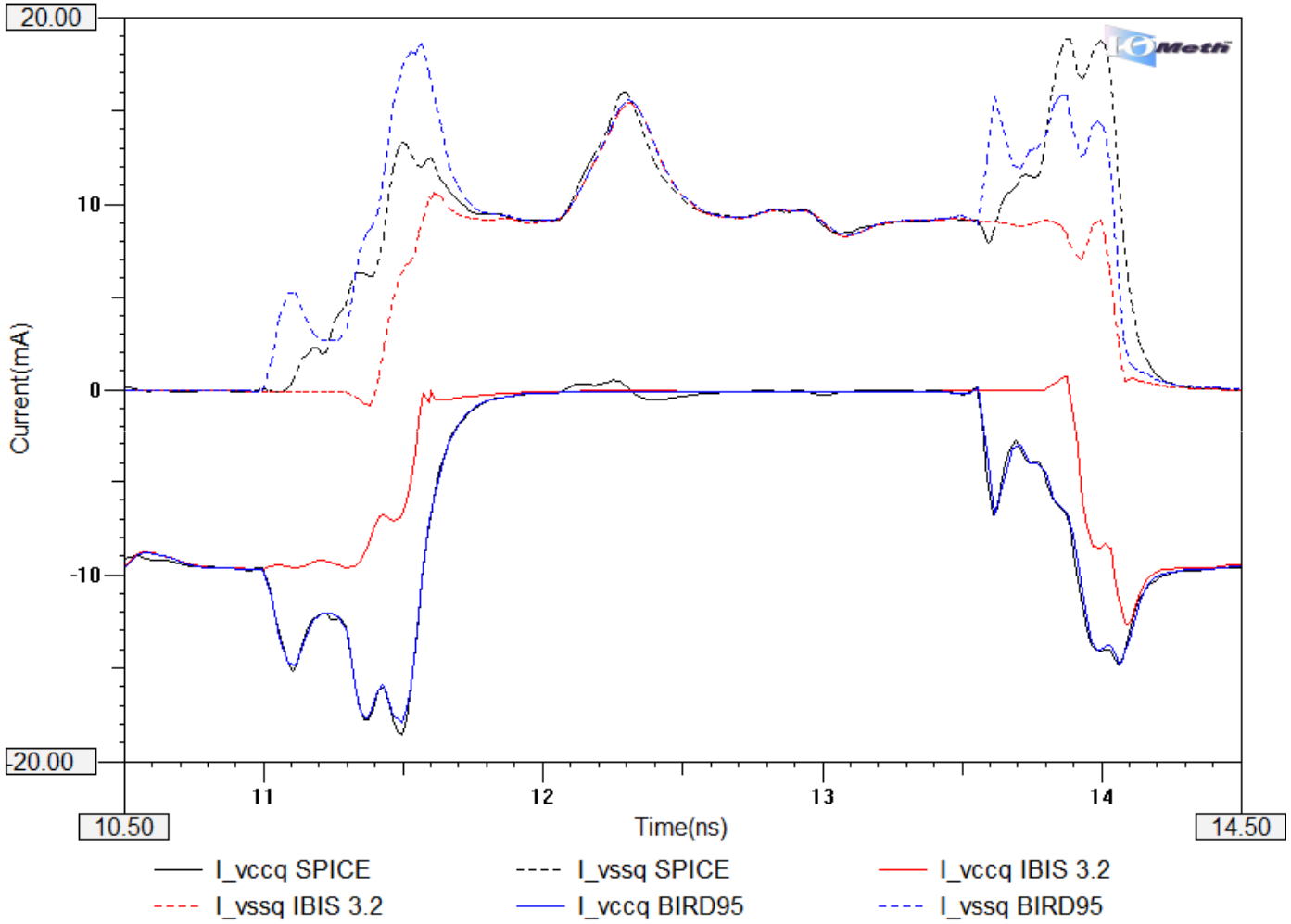
Comparing Tools A, B & C

Simulation Setups



- PRBS pattern, minimum bit width of 1.25ns.
- Typical corner only.
- On-die decoupling capacitance included.
  - No method to properly include through IBIS syntax (Series models attach to Pins, not die).
- Sim 1: DQ1 only, no package model
  - Compares BIRD95 directly to SPICE.
- Sim 2: DQ1 only, Rpkg = 5 Ω
  - Tests BIRD98 current scaling.
- Sim 3: DQ1 + DQ2 (in tri-state) with 8-port SPICE coupled package model
  - What happens with real package RLCs?
- Sim 4: DQ1 + DQ2 (with different PRBS) with SPICE package model
  - What happens with more than one buffer (real SSO conditions)?

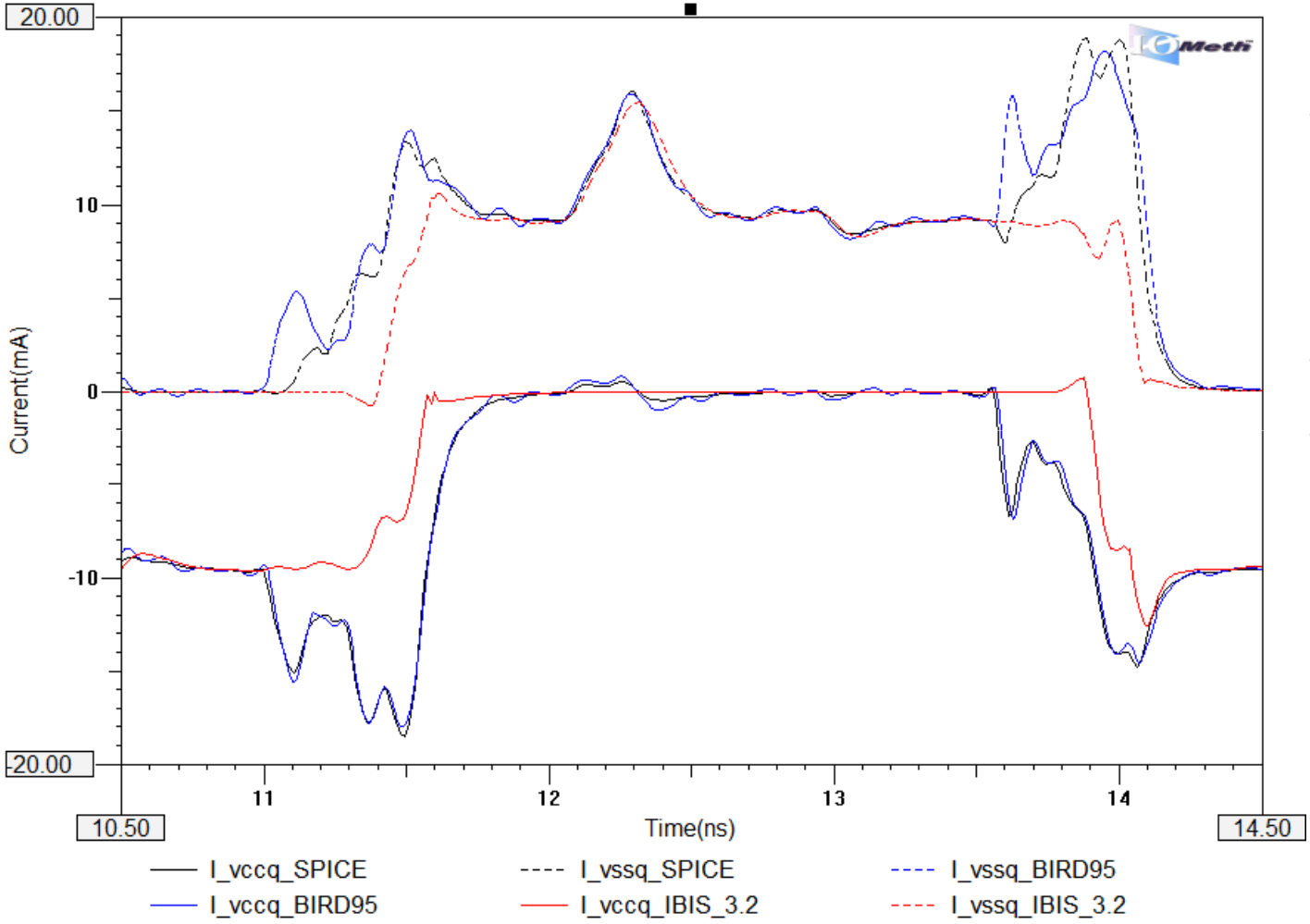
Sim 1, Tool A



VSSQ current improved over baseline.

VCCQ current matches well.

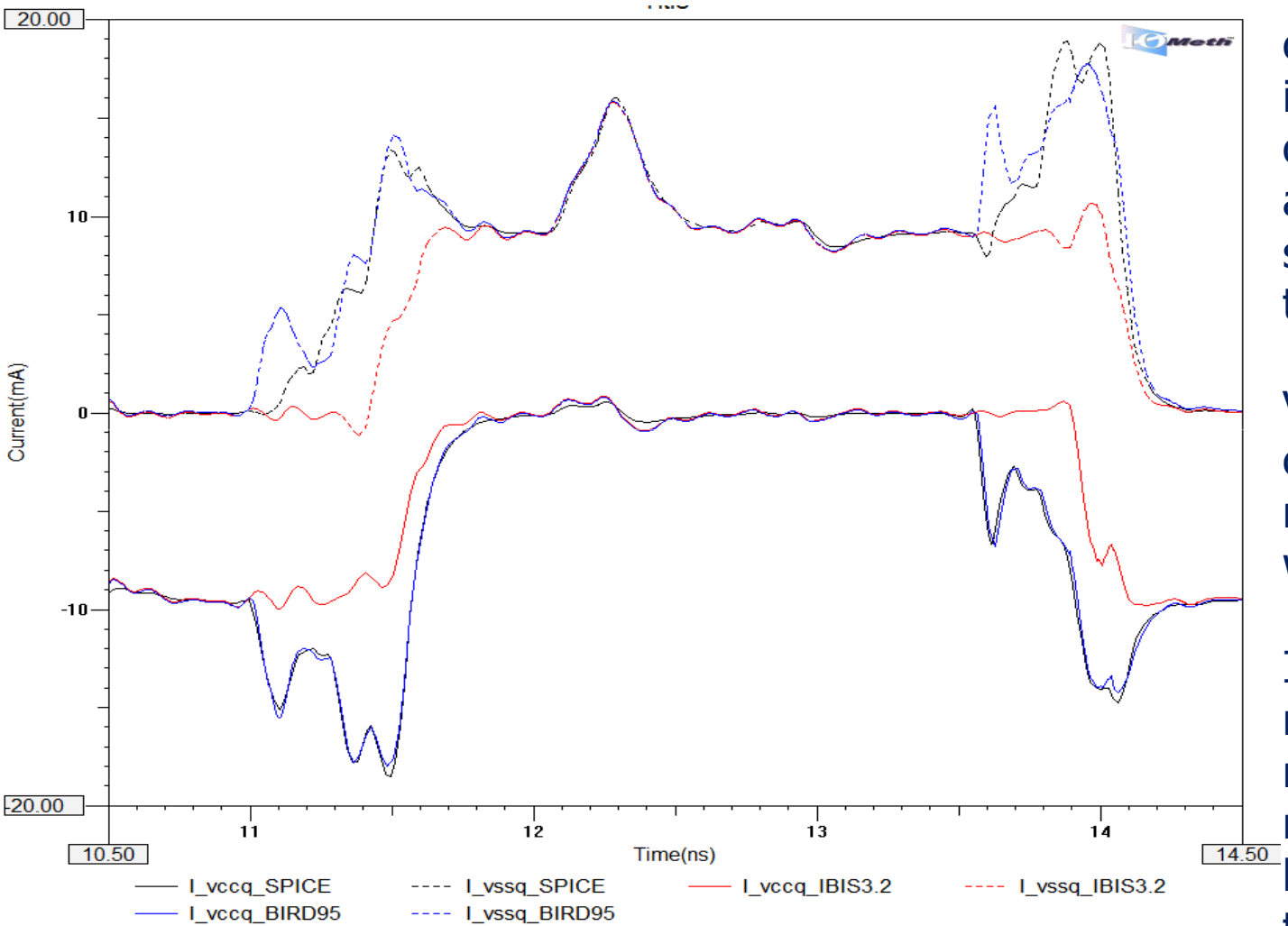
Sim 1, Tool B



VSSQ current improved over tool A.

VCCQ current matches well.

Sim 1, Tool C

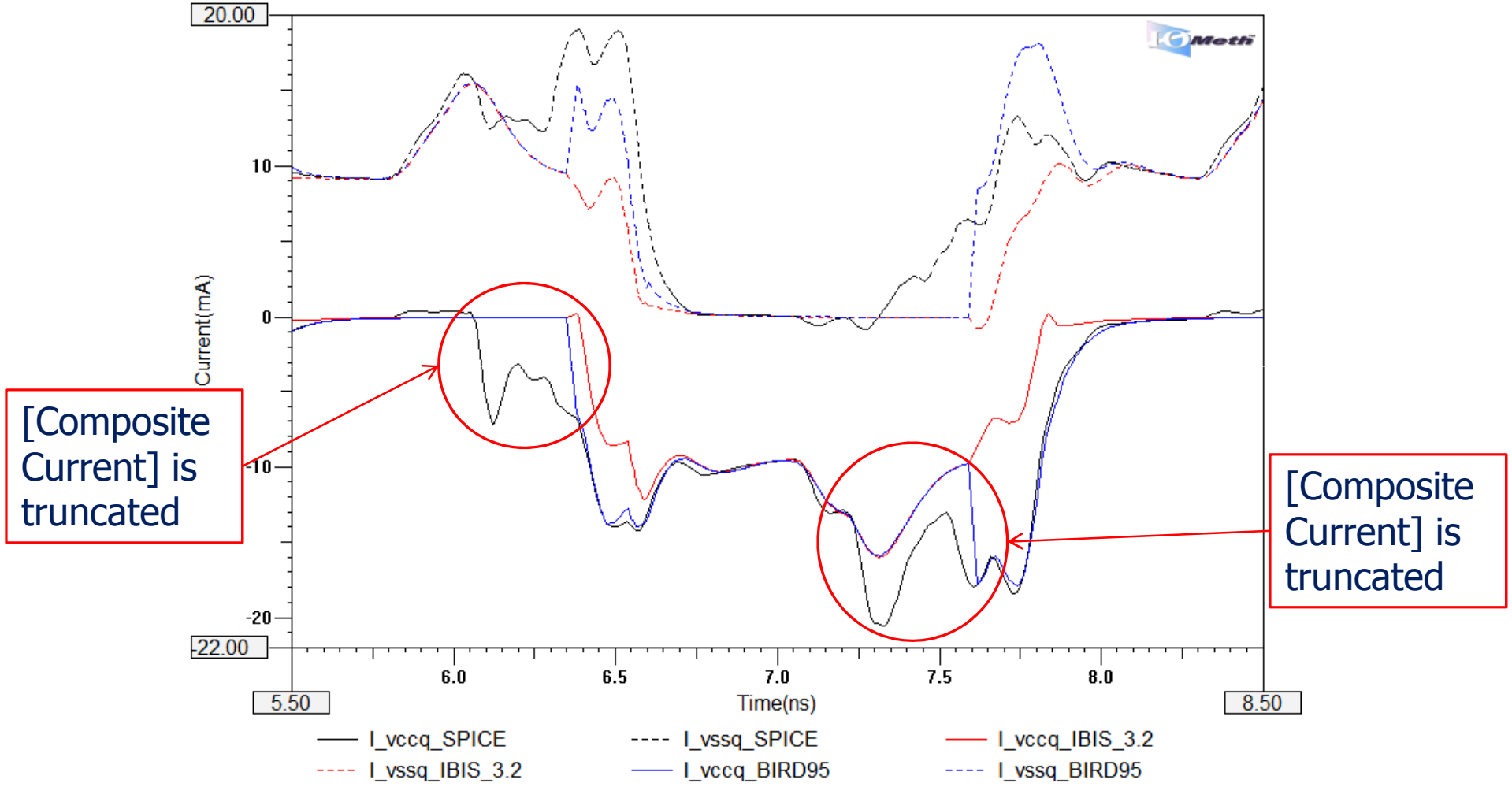


VSSQ current improved over tool A and very similar to tool B.

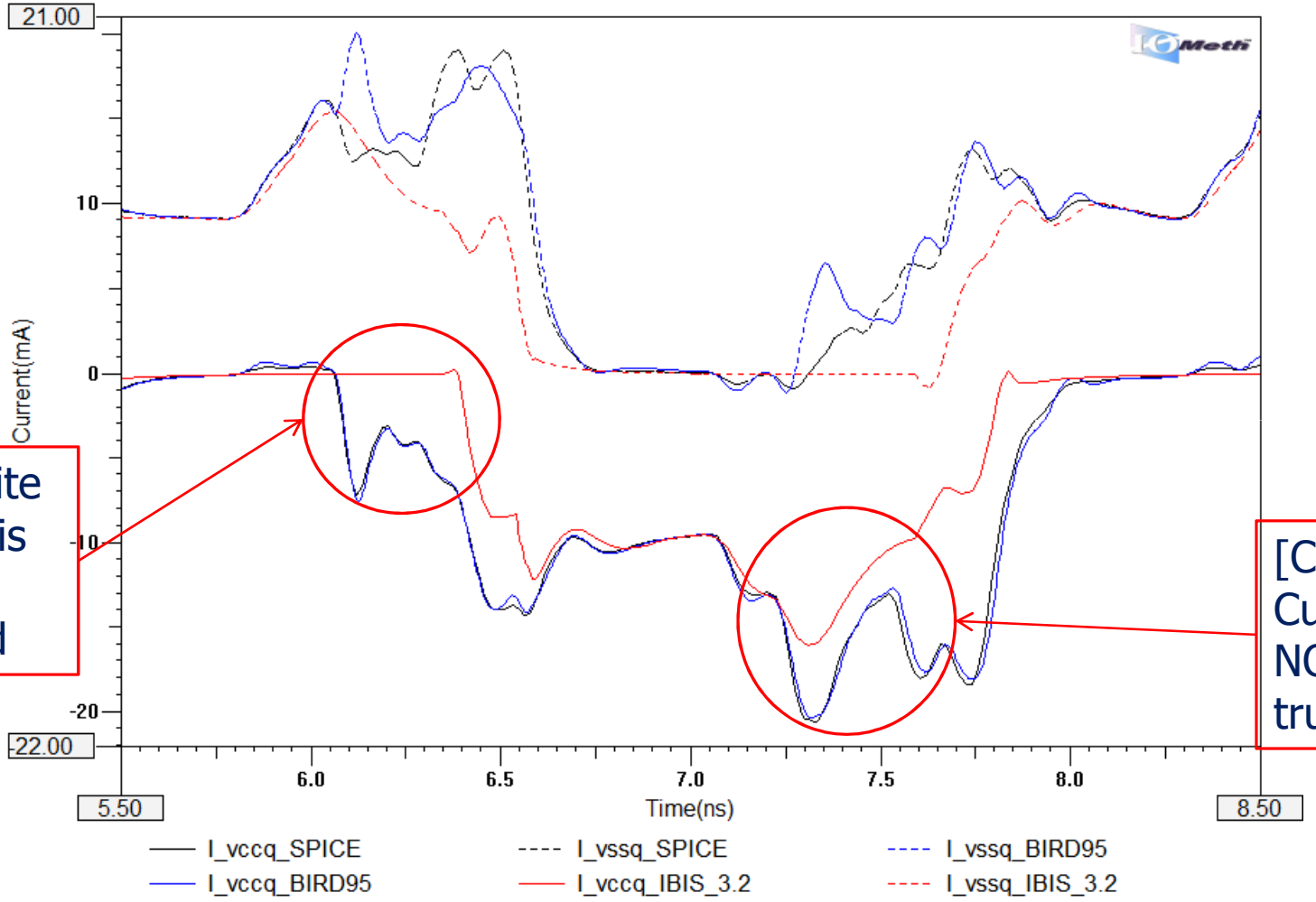
VCCQ current matches well.

IBIS 3.2 model results match better than tools A & B.

Sim 1, Tool A, 1.25ns Bit Width



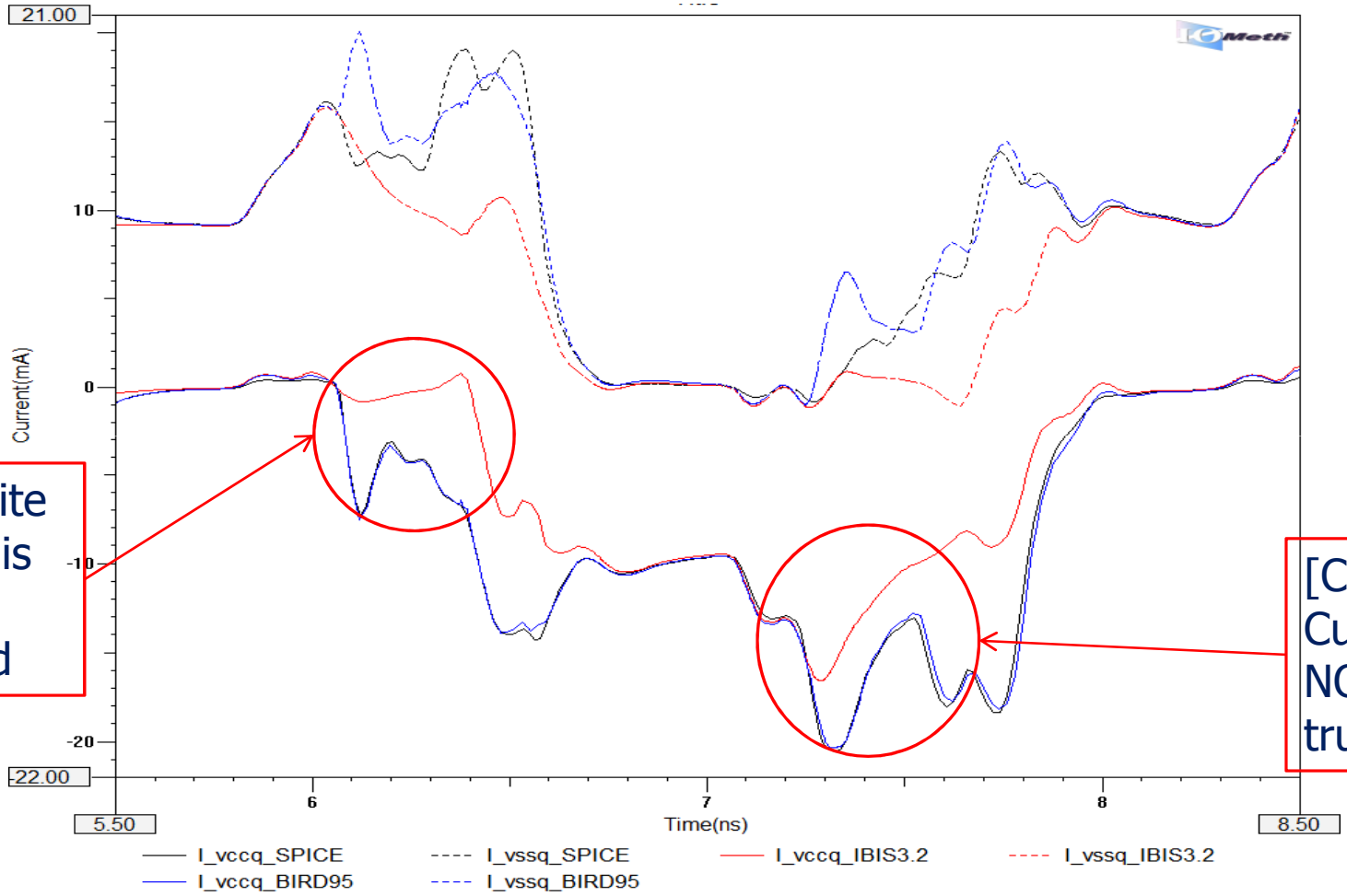
Sim 1, Tool B, 1.25ns Bit Width



[Composite Current] is NOT truncated

[Composite Current] is NOT truncated

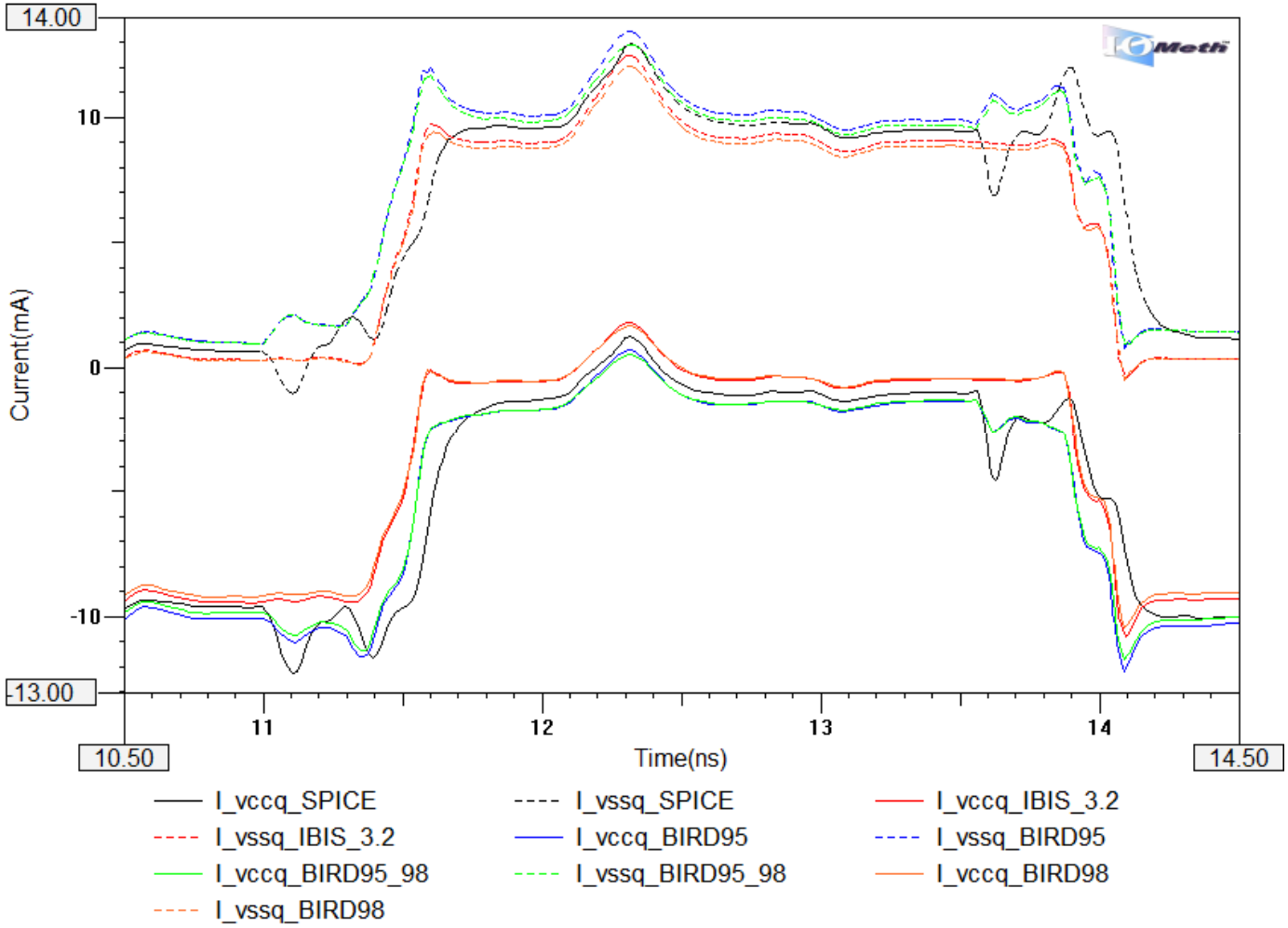
Sim 1, Tool C, 1.25ns Bit Width



[Composite Current] is NOT truncated

[Composite Current] is NOT truncated

Sim 2, Tool A

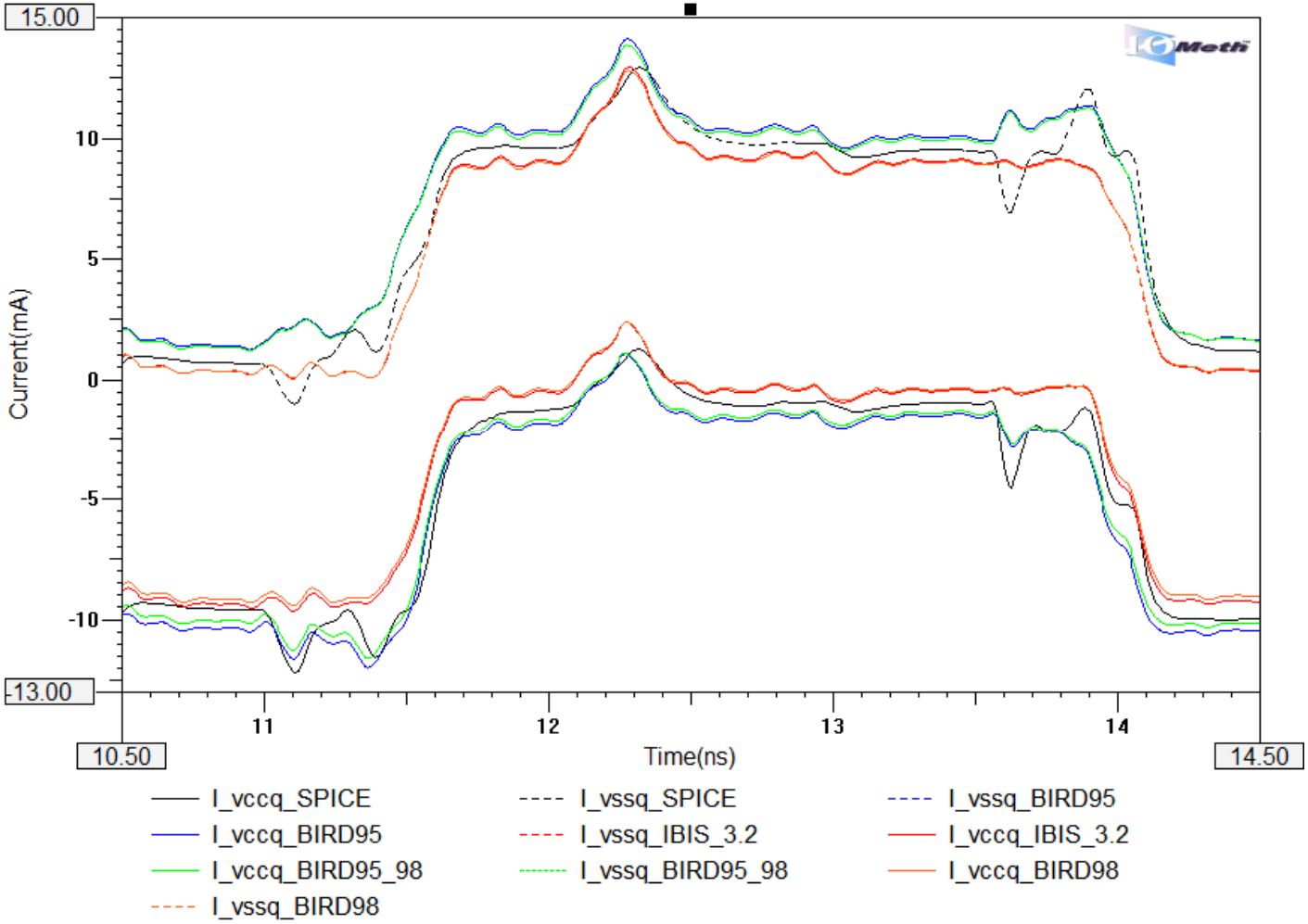


BIRD98 alone is a poor match.

BIRD98 improves BIRD95 results.

Matching to SPICE results ok.

Sim 2, Tool B

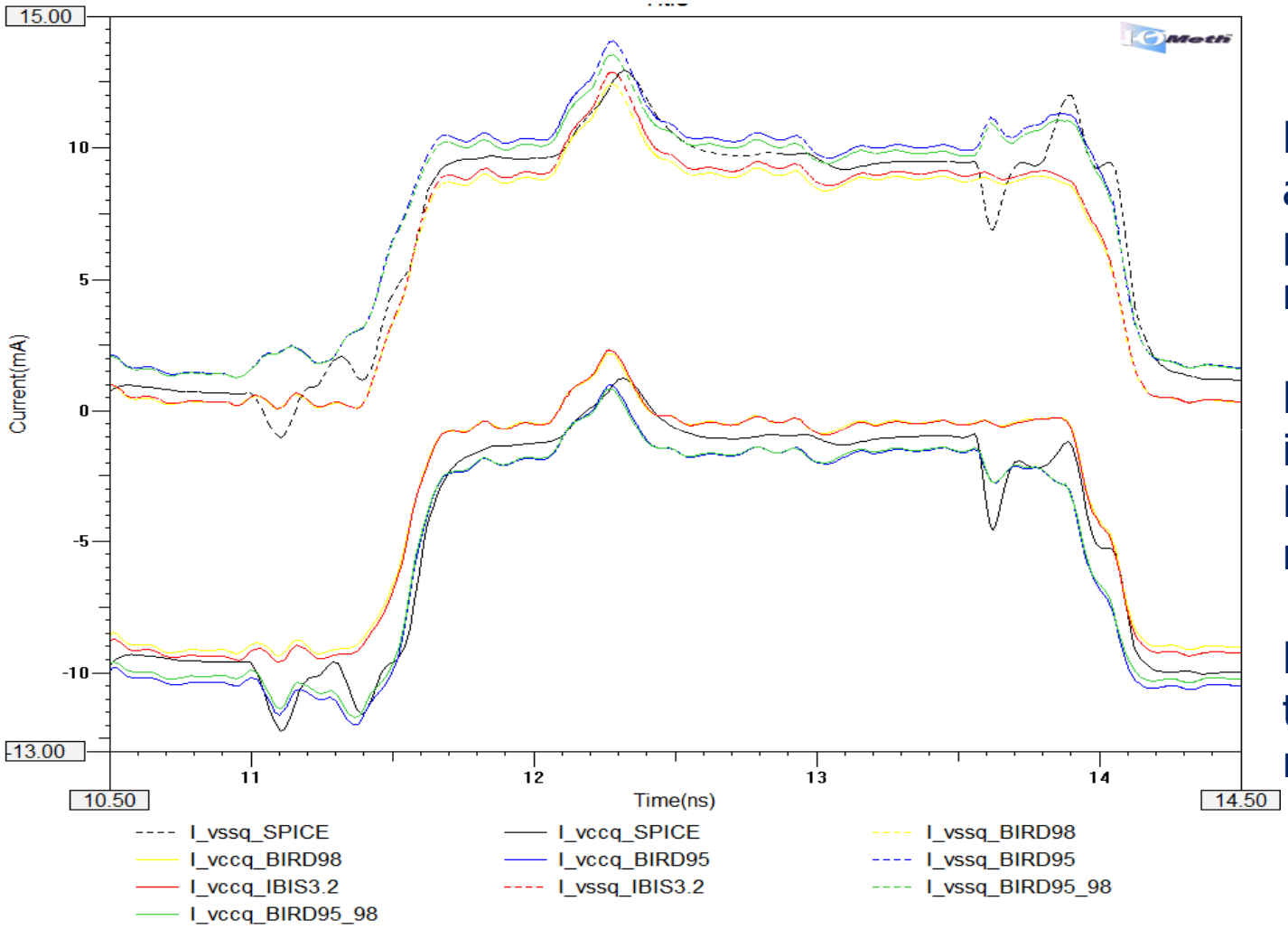


BIRD98 alone is a poor match.

BIRD98 improves BIRD95 results.

Matching to SPICE results ok.

Sim 2, Tool C

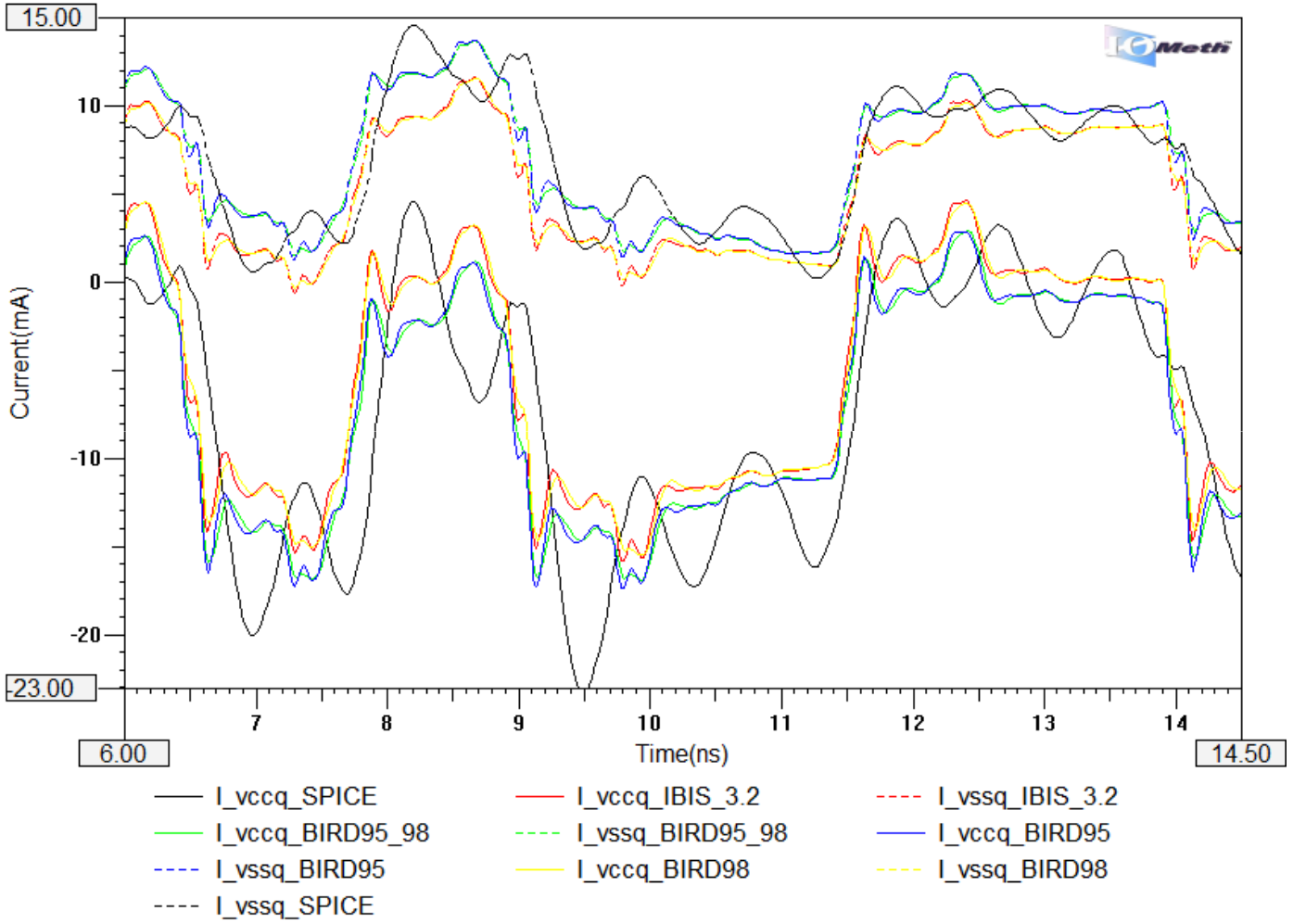


BIRD98 alone is a poor match.

BIRD98 improves BIRD95 results.

Matching to SPICE results ok.

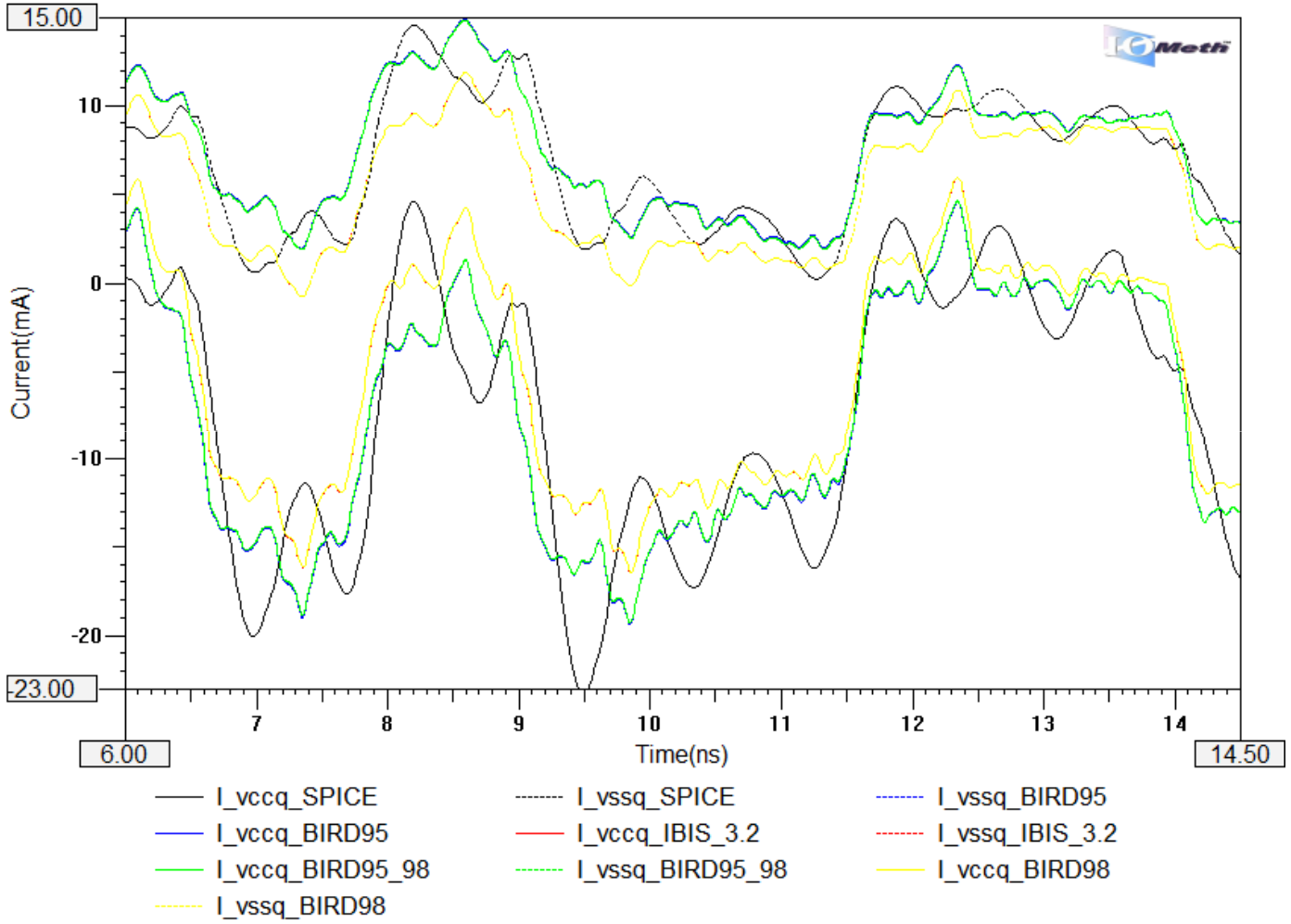
Sim 3, Tool A



BIRD95 and BIRD95 + 98 results are a better match to SPICE.

SPICE shows delay not seen with IBIS.

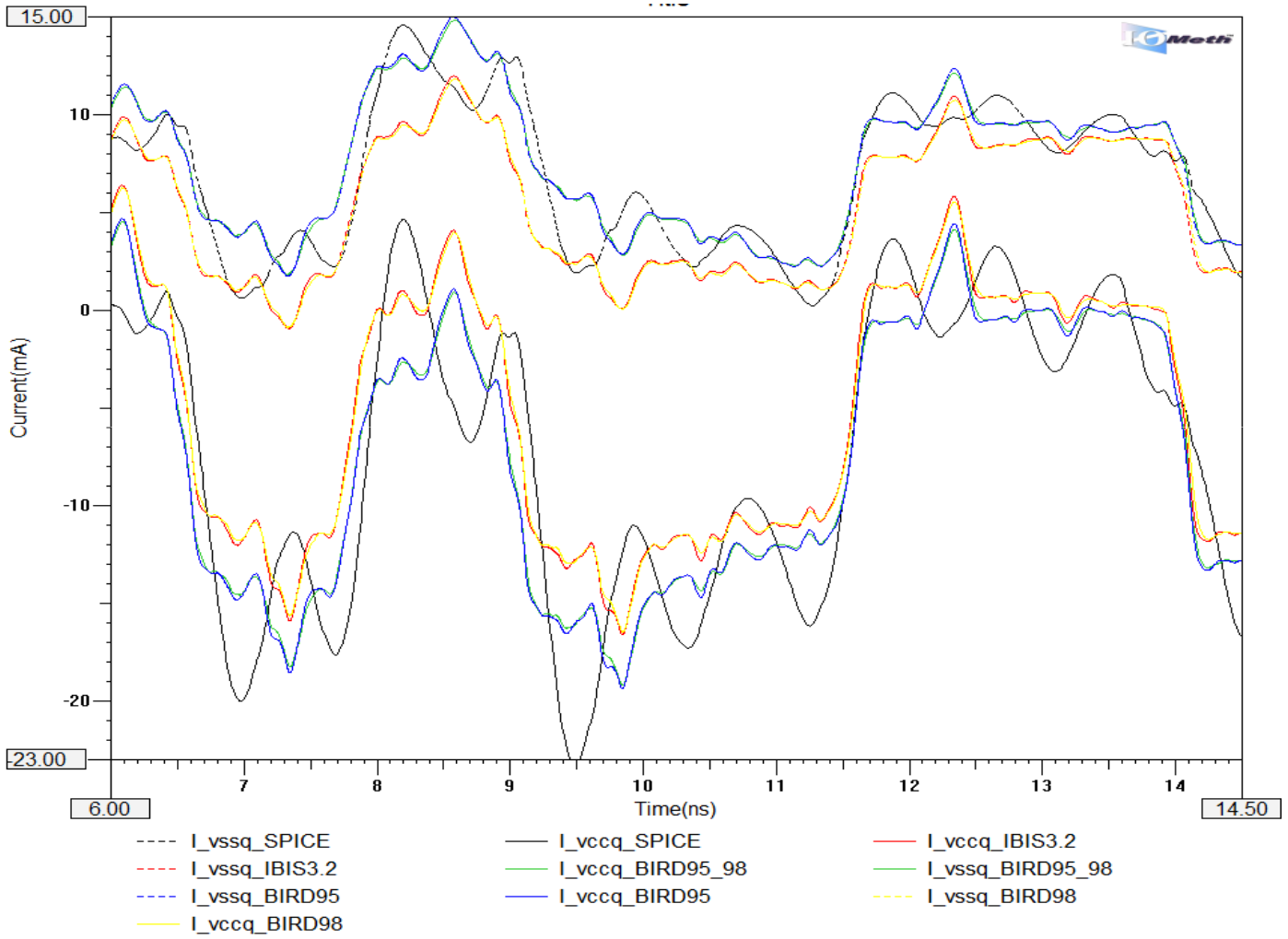
Sim 3, Tool B



BIRD95 and BIRD95 + 98 results are a better match to SPICE.

SPICE shows some delay not seen with IBIS.

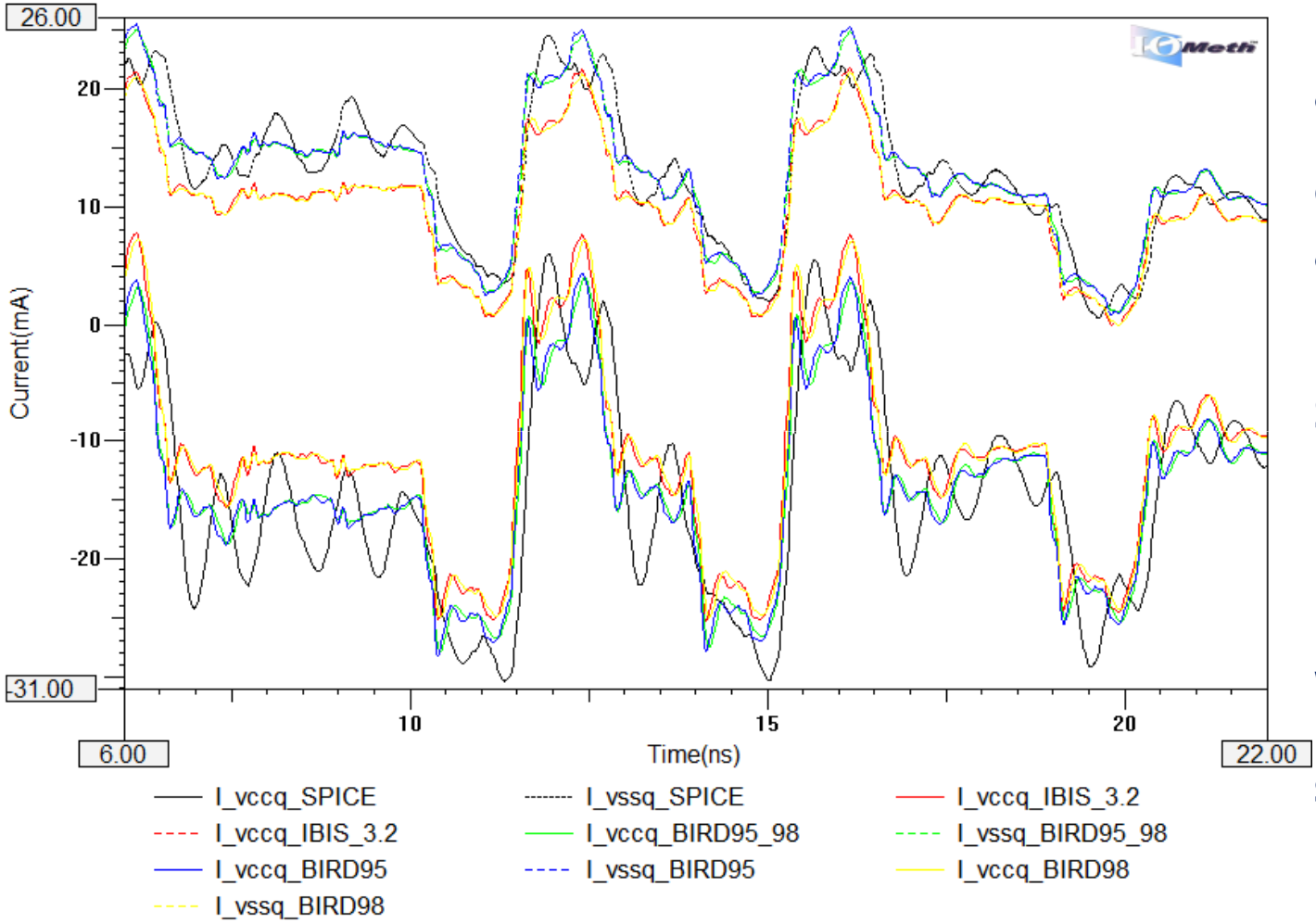
Sim 3, Tool C



BIRD95 and BIRD95 + 98 results are a better match to SPICE.

SPICE shows some delay not seen with IBIS.

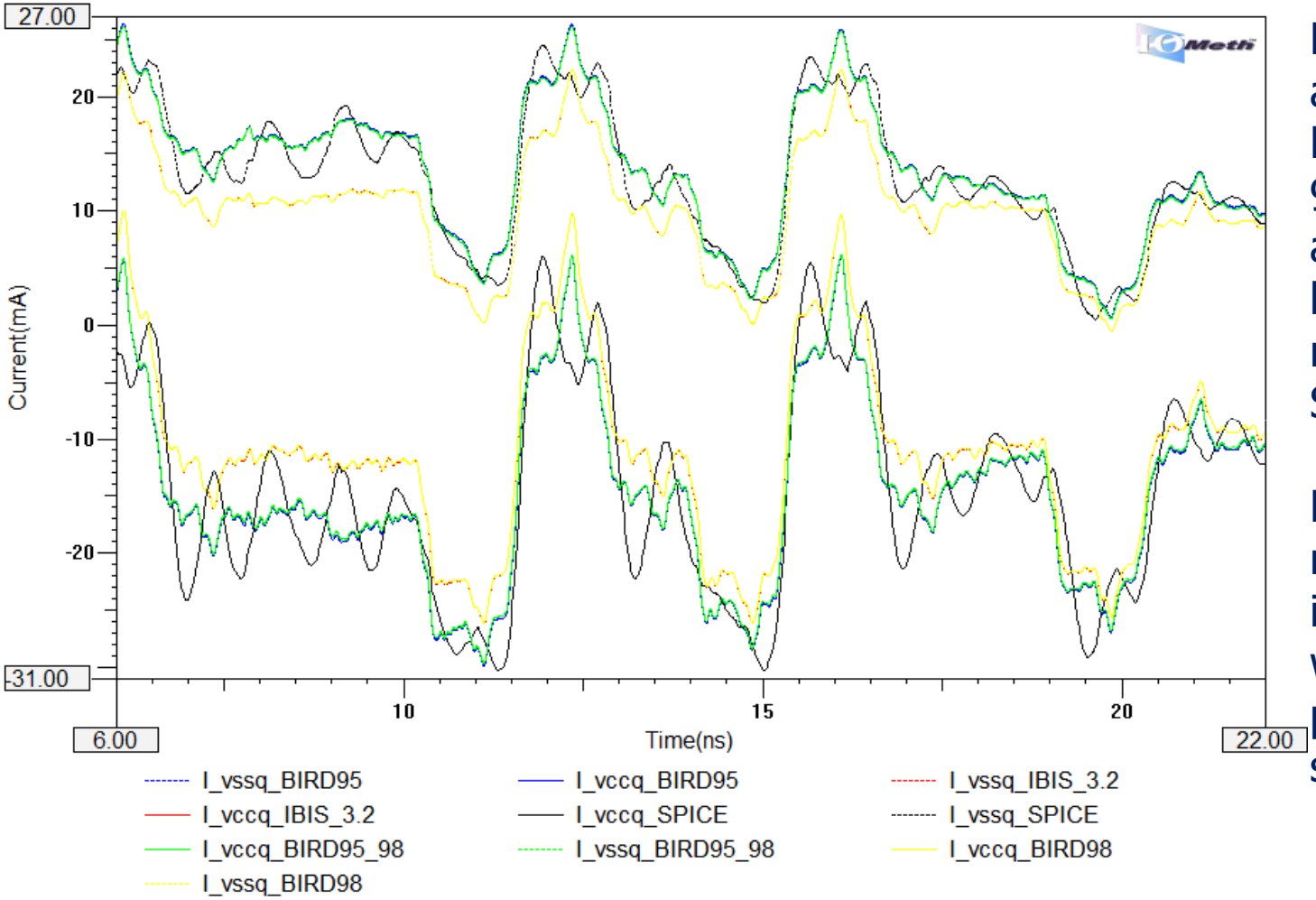
Sim 4, Tool A



BIRD95 and BIRD95 + 98 results are a better match to SPICE.

Results not improving with com-plexity of sim.

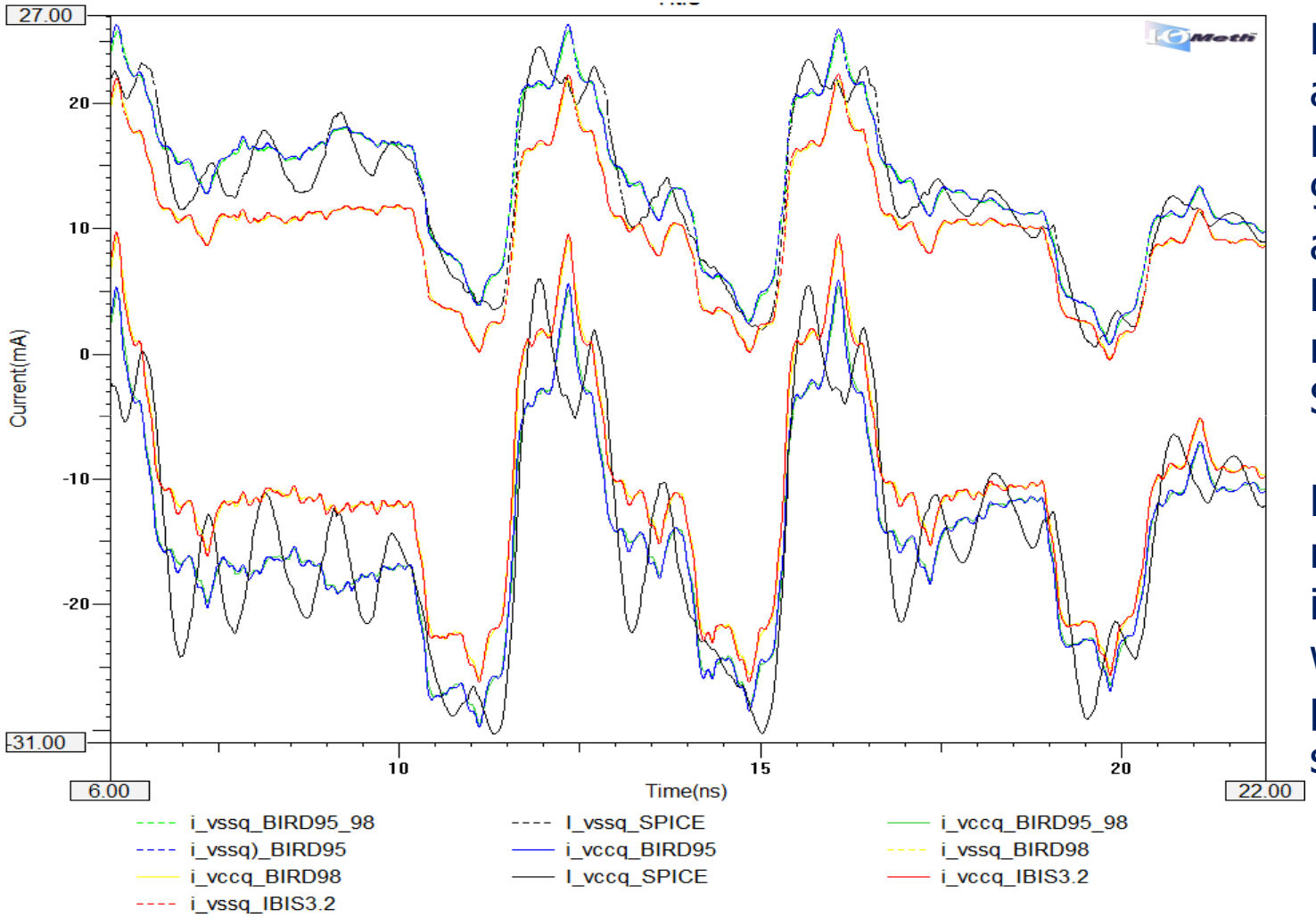
Sim 4, Tool B



BIRD95 and BIRD95 + 98 results are a better match to SPICE.

Results not improving with com-plexity of sim.

Sim 4, Tool C



BIRD95 and BIRD95 + 98 results are a better match to SPICE.

Results not improving with com-plexity of sim.

Conclusions

- Implementations of BIRD95 significantly improve power supply current simulation accuracy.
- Implementations of BIRD98 improve upon accuracy of BIRD95 alone.
- BIRD98 without BIRD95 does not improve results for these test cases.
- Algorithms could use further improvement to better match SPICE simulations that include package parasitics.
- IBISCHK5 may be too ‘sensitive’ for BIRD98 checks.
- Further studies are needed to find out if adding Ivssq info will improve overall accuracy for IBIS PDN simulations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