IBIS in Academia

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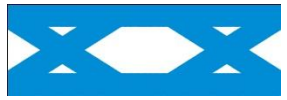
Design Automation Conference
IBIS Summit
San Diego, California
June 7, 2011



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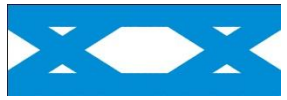
Introduction

- IBIS in academia, technical literature, and academic conferences
- IBIS, a base-line for expanded research on I/O buffer algorithms and extensions
- Many national and international papers, several thesis, several tools
  - About 80-100 "IBIS" references from 139 IEEE Xplore hits
  - Google search, technical library electronic access
  - http://www.ece.ncsu.edu/erl/publications/
  - http://www.emc.polito.it/publications/all_pub.asp
  - http://www.teraspeed.com/ibis_resources.htm
- Sampling of interesting papers and tools here
- Purpose – highlight and make visible academic impact

Review of Academic Involvement

- Basic algorithms
- S2ibis
- New algorithms
- Power delivery systems and EMC
- Other work
- Conference references here
  - SPI = IEEE Workshop on Signal Propagation on Interconnects (Europe)
  - EPEP(S) = Electrical Performance of Electronic Packaging (and Systems)
  - EMC Compo – International Workshop on Electromagnetic Compatibility of Integrated Circuits (Europe)



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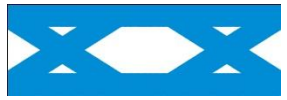
Basic Algorithms from IBIS

- Early modeling algorithms were just ramp or waveforms & non-linear I-V transitions yielding curved results different from extractions
- IBIS Buffer Algorithms – solving two waveform from low and high-state I-V tables
- Many Summit presentations addressed this issue by Ross, Muranyi, Chen, Mirmak, Unger, etc.
  - Basic 2-waveform algorithm and development
  - AMS extensions
  - Many V-T tables
  - ECL
  - Add L_fixture, C_fixture
  - C_comp extensions
  - Additional (blocks) to IBIS for Driver Schedule, Submodels, etc.



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Some Early Algorithm References

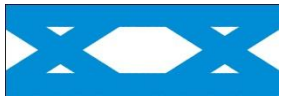
- P.F.Tehrani, Y. Chen, J. Fang, "Extraction of transient behavioral model of digital I/O buffers from IBIS," Proc. 46th Elect. Comp. and Tech. Conf. May 1996 (State Univ. of New York) – 1, 2 waveform algorithm
- Y. Wang, H.N. Tan, "The development of analog SPICE behavioral model based on IBIS model," Proc. Ninth Great Lakes Symp. On VLSI, 1999 (Nanyang Technology Instit. - Singapore) – 2-waveform algorithm
- B. Ross, "IBIS Present and Future," Proc. SPI 2003, May 2003 (Teraspeed Consulting Group) – waveform algorithm research

Spice to IBIS and IBIS Algorithms

- NCSU – Paul Franzon, Michael Steer (also an IBIS Librarian) since about 1995 and students Steve Lipa, Alan Glaser, Ambrish Varma
  - http://www.ece.ncsu.edu/erl/software/ibis_general/
  - http://www.ece.ncsu.edu/erl/publications/
- (Supported by ARPA and DARPA funding)
- Later, Paul Fernando on AMS macro-modeling and Ting Zhu on IBIS algorithms)
- Spice 2 IBIS development: s2ibis, s2ibis3, s2ibis3, s2iplt
  - Now handled by IO Methodology
- Paul Fernando, MS, Ambrish Varma Ph.D. thesis on IBIS topics
- S2IBIS – a major contributor to IBIS success!!

Newer Research and Tools

- Universities
  - Politecnico di Torino – Igor Stievano, Flavio Canavero, etc. (Italy)
  - Univ. de Bretagne Occidentale (France)
  - Georgia Tech (Madhaven Swaminathan, Bhyrav Mutnury, etc.)
  - North Carolina State University (Ting Zhu)
- I/O buffer modeling and model extraction generalization for power intergrity, packages, spline fitting, pre-emphasis, equation based, etc.
  - Radial based functions, and other orthogonal functions as basis
  - M(pi)log tool – includes VHDL-AMS, Spice link
    - http://www.emc.polito.it/software/Mpilog/mpilog_home.asp
  - Volteria, Volteria-Laguerre model
  - Recurrent neural network
  - Surrogate modeling



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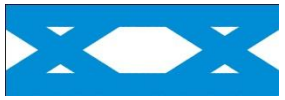
New Academic References

- B. Mutnury, M. Swaninathan, J.P. Libous, "Macromodeling of nonlinear digitial I/O Buffers," IEEE Trans. Adv. Packag. Feb. 2006 (Georgia Tech)
- B. Mutnury, M. Swaminathan, Nam Pham, D. de Araujo, E. Matoglu, "Macromodeling of nonlinear transistor-level receiver circuits," IEEE Trans. Adv. Packag. Feb.2006, (Georgia Tech)
- I.S. Stievano, I.A Maio, F.G. Canavero, "Parametric macromodels of digital I/O drivers," IEEE Trans. Adv. Packag, May 2002, (Politecnico di Torino - Italy)
- A. Varma, A. Glaser, S. Lipa, M. Steer, P. G. Franzon, "The development of a macro-modeling tool to develop IBIS models," EPEP 2003, Oct. 2003 (NCSU)
- I.S. Stievano, I.A Maio, F.G. Canavero, "Mpilog, macromodeling via parametric identification of logic gates," IEEE Trans. Adv. Packag, Feb. 2004, (Politecnico di Torino - Italy)

New References Continued

- A.K. Varma, M. Steer, P.D. Franzon, "Improving Behavioral IO Buffer Modeling Based on IBIS," IEEE Trans. Adv. Packag., Nov. 2008 (NCSU)
- T. Zhu, P.D. Franzon, "Application of surrogate modeling to generate compact and PVT-sensitive IBIS models," EPEPS 2009, Oct. 2009 (NCSU)
- M.G. Telescu,,I.S. Stievano, F.G. Canavero,, N. Tanguy, "An Application of Volterra series to IC buffer models," SPI 2010, May 2010 (Univ. de Bretagne Occidentale. Politecnico di Torino - Italy)
- C. Diouf, M. Telescu, N. Tanguy, P. Cloastre, I.S. Stievano, F.G. Canavero, "Statistically constrained non-linear models with applications to IC buffers," SPI 2011, May 2011 (Univ. de Bretagne Occidentale - France, Politecnico di Torino - Italy)



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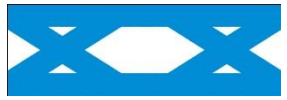
Power Delivery Systems Project

- Mocha: MOdelling and CHAracterization of SiP Signal and Power Integrity Analysis:
  - http://www.mocha.polito.it/WP2.htm
  - European community funded program
- Academic Involvment
  - Politecnico di Torino (Italy)
  - Instituto de Telecomunicacoes (Portual)
- Industrial partners – Micron Technology, Cadence, Agilent, Microwave Characterization Center
- (A STREP project funded by European Community)
- I/O buffers may be extensions of IBIS

More Power Integrity

- Z. Yang, S. Huq, V. Arumugham, I. Park, "Enhancement of IBIS modeling capability in simultanous switching noise (SSN) and other power integrity related simulations-proposal implementation and validation," Int. Symp. Electromagn. Compatibil., Aug, 2005 (Cisco Systems)
- P. Pulici, A. Girardi, G.P. Vanalli, R. Issi, G. Bernardi, G. Ripamonti, A. Strollio, G. Campardo, "A modified IBIS model aimed at signal integrity analysis of systems in package," IEEE Trans. Circuits Syst. I., Aug. 2008 (Univ. Of Naples Federico II, Numonyx, ST Microelectronics – Italy)



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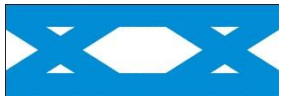
EMC/EMI – Academic Involvment

- UTE (Union Technique de L'Electricite) – French standardization group involved with IBIS in 1998
- Industry and the following French universities
  - Institut National des Sciences Appliquees de Toulouse (INSA) - E. Sicard
  - ESEO Institute of Science and Technology - M. Ramdani
  - Institut Europeen de Recherche Sur Les Systemes Electroniques Pour Les TransPorts (IERSET) - M. Lubineau
- ICEM (Integrated Circuits Electromagnetic Model) now IEC 62014-3
- IC-EMC tool from INSA tool references IBIS Package model and has comment lines for IBIS. It also has a BGA display utility (A. Boyer, E. Sicard, INSA – France
  - http://www.ic-emc.org/



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Other Contributions

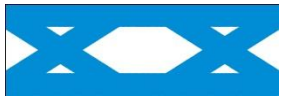
- Non-linear C_comp (BIRD79)
  - Luca Giacotto (Alstrom Transport – France) Ph. D. thesis (Alstom Transport and Laboratoire IMEP Ecole Doctorale EEATS – France) – C_comp pole/zeros as function of voltage, state
  - L. Giacotto, B. Meyniel, J. Chilo, "IBIS models: quality: the benefits of frequency-domain analysis," EMC Comp 2002, Nov. 2002 (Alstrom Transport, France)
- IBIS Healing Tool free utility
  - Francesco de Paulis, Dinilo Di Febo, Antonio Orlandi, University of L'Aquila, Italy
  - European IBIS Summit, May 11, 2011
  - http://orlandi.in.univaq.it/uaq_laboratory/

International IBIS Sampling

- G.N, Nardakumar, N. Patel, R. Reddy, M, Kothandaraman, "Application of the Douglas-Peucker algorithm to generate compact but accurate IBIS models," 18th Int. Conf. VLSI Design, Jan. 2005 (Agere Syst. – India) – I-V table interpolation algorithm
- L. C. Leong, S. H. Ying, C. S. Fong, W. W. Lo, "An improved I/O buffer correlation methodology between silicon and SPICE model," IEEE Asian Pacif. Conf. on Circ. Sys. (ACCAS) Dec. 2010 (Altera - Malaysia) – Correlation with Spice for IBIS model development
- H. Shen, Z. Wang, W. Zheng, "PCB level SI simulation based on IBIS model for high-speed FPGA system," 9th Int. Conf. Electr. Meas. & Instr., Aug. 2009 (Chinese Acad. of Sci. - China) - IBIS and vendor tool
- W-T. Huang, C-T. Chou, I-S. Lin, C-H. Chen, "Studying an approach of I/O buffer information Specification (IBIS) model," J. Chinese Instut Engrg, Feb. 2007 (National Taipei Univ. of Technology, Taiwan) – Basic IBIS and vendor tool

IBIS and Academic Events

- Co-located Summits
  - DAC - Design Automation Conferance (1993 – present)
  - DATE - Design Automation and Test in Europe (1998 – 2009)
  - SPI (2010 – present in Europe)
- Other conferences with IBIS content and potential involvement
  - EPEP(S)
  - EMC Compo (in Europe)



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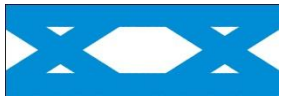
Conclusion

- Academia and IBIS historically connected
  - Literature, conferences, tools, thesis
  - Co-located summits with academic events
    - Presentations from academia
  - Student involvement with IBIS
  - IBIS and I/O buffer research continues (weighted two state functions often the basis for buffer algorithms)
- Cooperative collaboration beneficial



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