Power Integrity for Single Ended Systems

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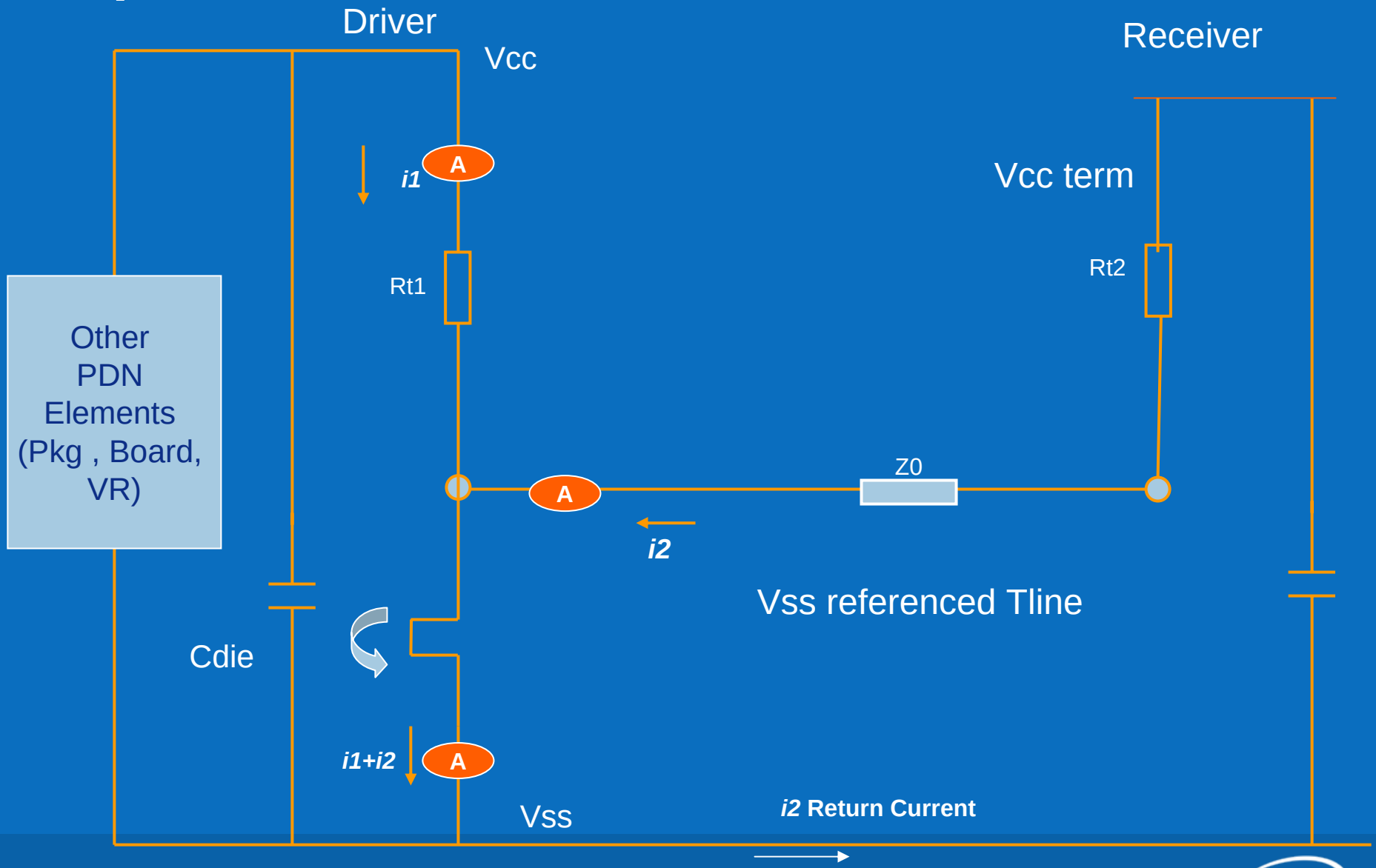
Outline

- Objective: To demonstrate the Power Integrity (PI) methodology for Single ended systems with the emphasis on the buffer models.
- Single Ended systems
  - Driver Types
    - Open drain, Open source, Push-pull
  - Termination schemes for push-pull
    - Vss, Center-tap, Vcc termination
- PI only analysis:
  - Icc(t) generation and usage
- PI/SI analysis
  - PD noise impact on the jitter and voltage margin
- IBIS* involvement

Open Sink Driver

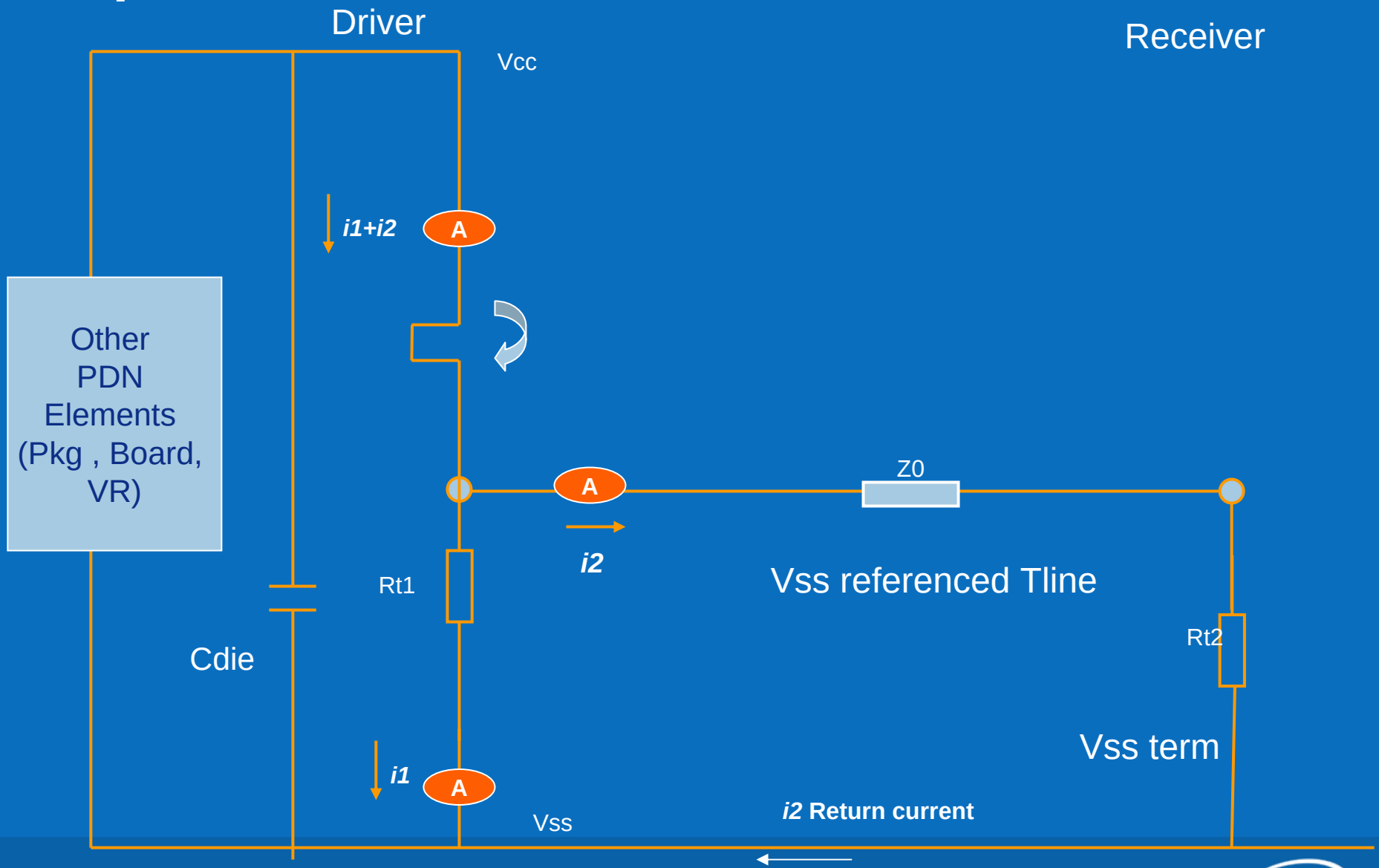


*Other names and brands may be claimed as the property of others

A Ammeter

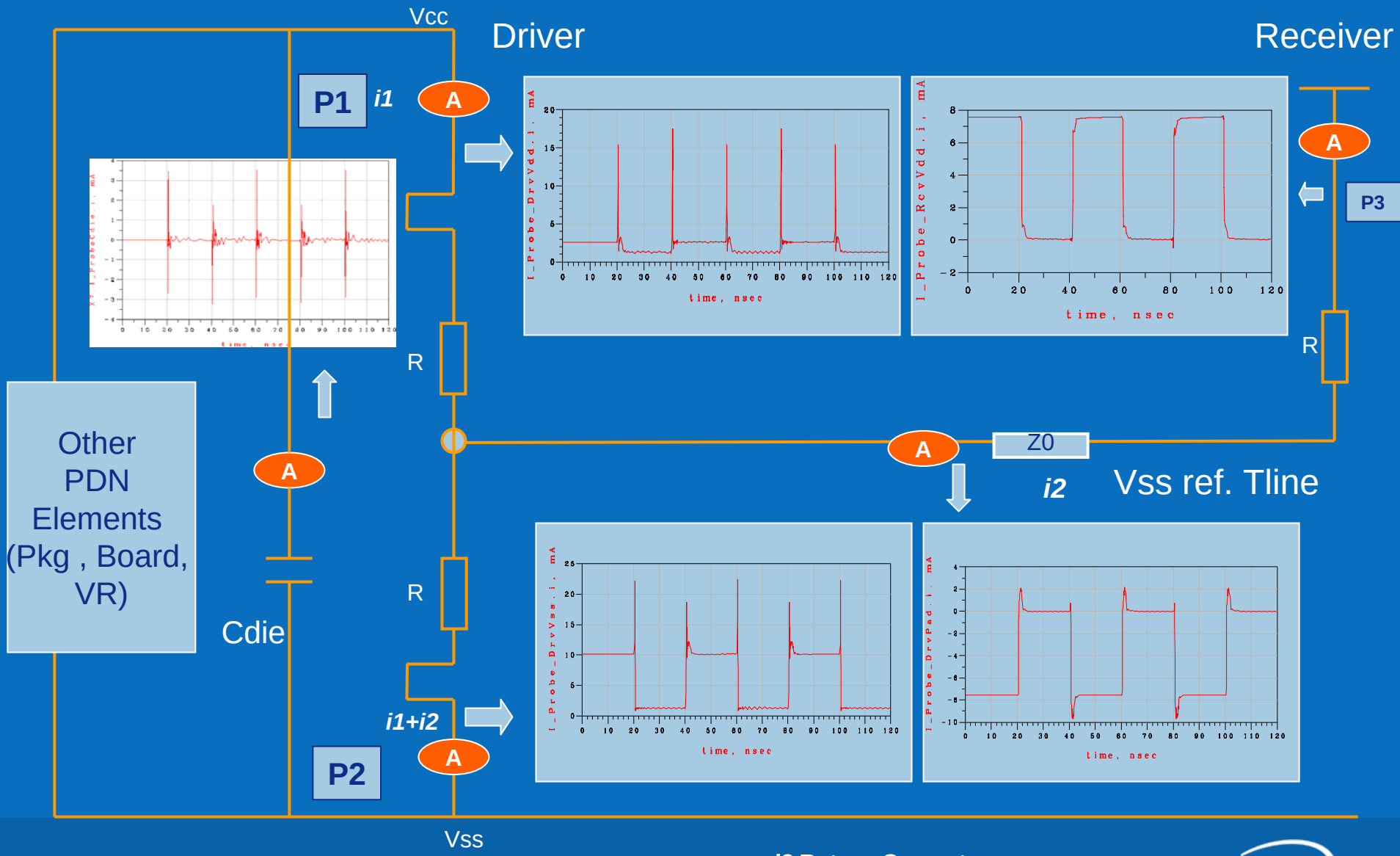
PDN: Power Distribution Network

Open Source Driver



A Ammeter

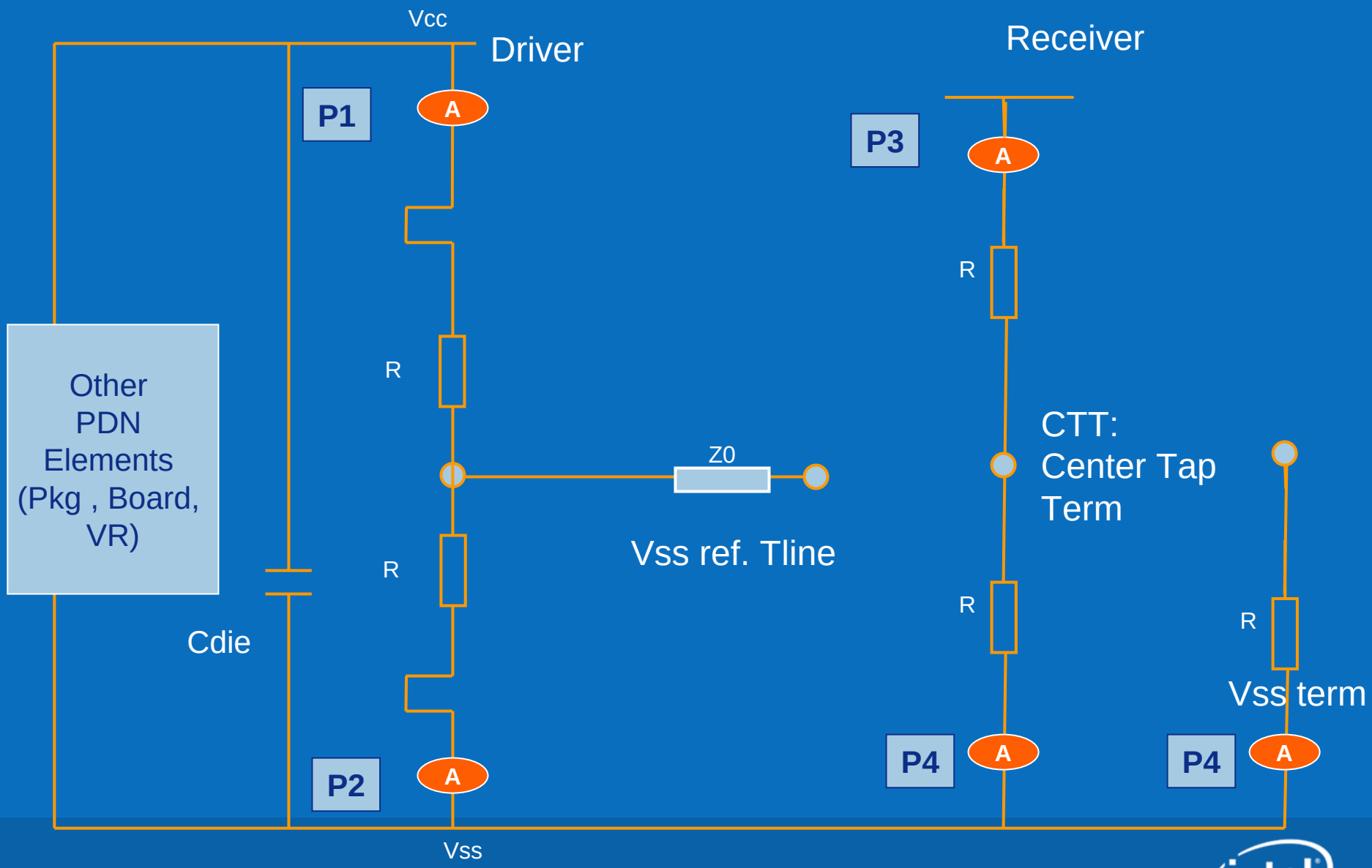
Push-pull Driver, Vcc Termination



i2 **Return Current**

A Ammeter

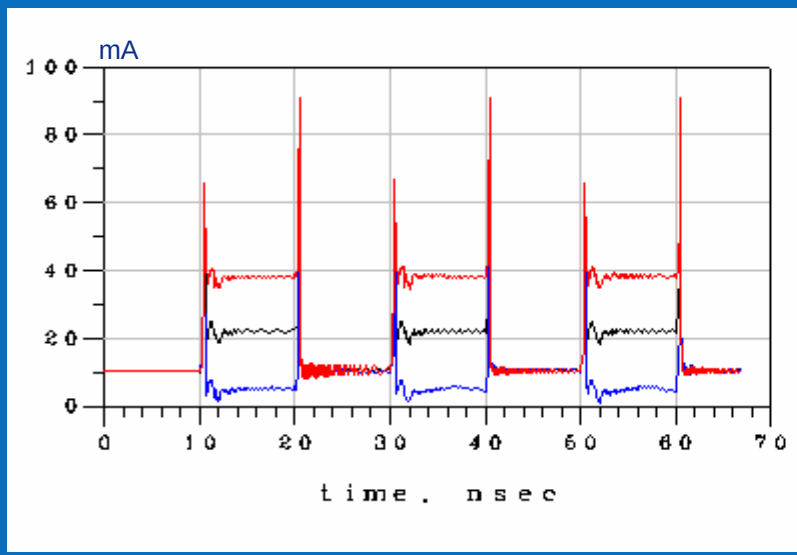
Push-pull: Other terminations



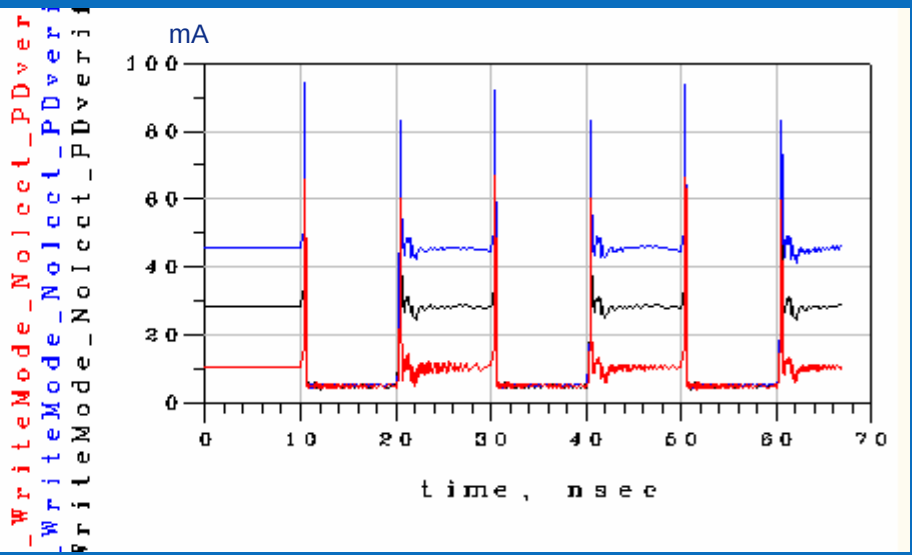
Push-pull Driver

- Four push-pull devices are used with SI/PD† model
- Currents are probed at the Vcc and Vss of the Driver node

Currents at P1 node (Vcc)



Currents at P2 node (Vss)



Vcc Term CTT Vss Term

- Current Profiles at the Driver power domains vary significantly based on the termination schemes at the Receiver
  - Need to consider realistic termination schemes and not just capacitive loading

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† PD: Power Delivery

PDN Currents at Driver

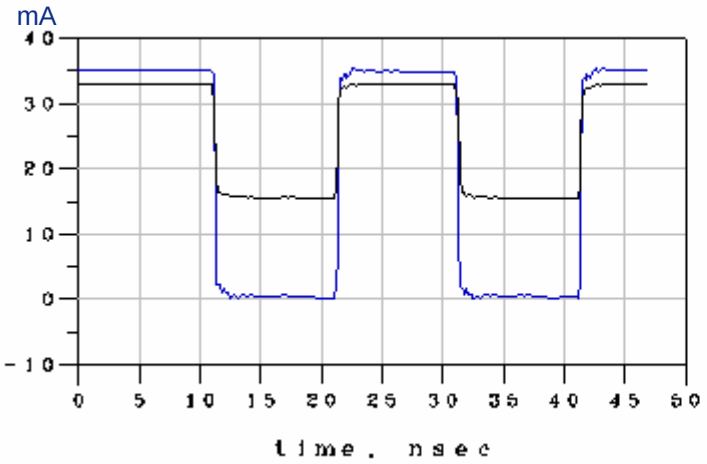
Receiver Term ⇨ Vcc Term Driver currents	Vcc Term	Vss Term	CTT
Vcc Currents **Ivcc**	Crowbar current	DC Step + Crowbar current	½ DC step + Crowbar current
Vss Currents **Ivss**	DC Step + Crowbar current	Crowbar current	½ DC step + Crowbar current

- Driver PDN currents are dependent on termination schemes at the Receiver
  - DC step due to termination scheme
  - IBIS* application: Does BIRD 95 enable to include Ivcc and Ivss based on termination schemes?
- Crowbar currents for all configurations: Behavioral models need to include accurate Crowbar currents

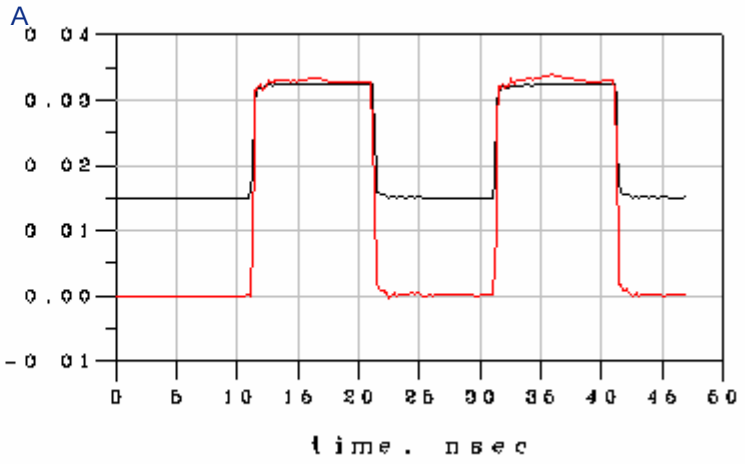
Push-pull Driver

- Four push-pull transistors are used with SI/PD model
- Currents are probed at the Vcc and Vss of the Receiver node

Currents at P3 node (Vcc)



Current at P4 node (Vss)



Vcc Term CTT Vss Term

- Vcc (P3) currents: di/dt for Vcc Term is higher than that for CTT.
- System level model need to be considered with Driver and Receiver PDN

PDN currents at Receiver

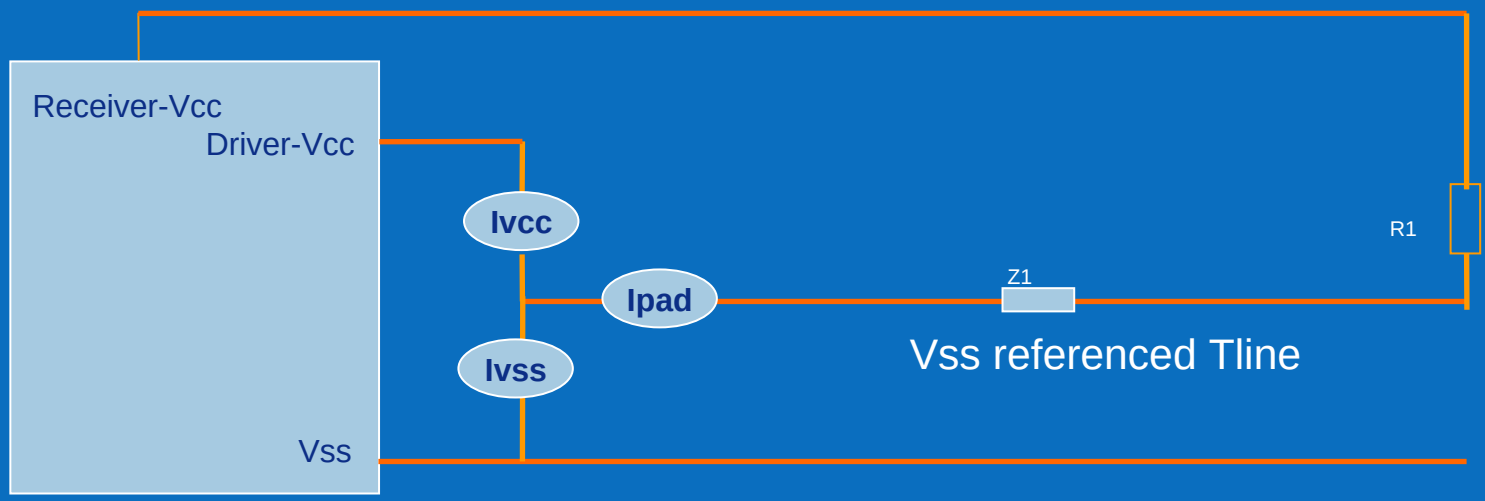
Receiver Term → / Receiver currents	Vcc Term	Vss Term	CTT
Vcc Currents	DC Step	N/A	½ DC step
Vss Currents	N/A	DC Step	½ DC step

- CTT produces smaller step than other two
  - Due to the resistor divider the DC step is half of that for the other cases
- Smaller the step, smaller is the di/dt.

Icc(t) Generation

- Icc(t) is Ivcc and Ivss at the Driver PD node w.r.t. time
  - It provides a means to estimate the noise on the PDN as a function of SSO
    - Advantages: It gives first pass noise information
    - Disadvantages: It cannot model the buffer/ PDN dynamic interaction.
- Icc(t) for a single Driver is expanded to the interface
  - It can be scaled by total number of Drivers switching at the same time.
- Then, generate a PDN network and test different patterns, as PDN has some resonance.
  - Maximum data rate
  - Data rate at PDN resonance frequency
  - Interconnect resonance frequency

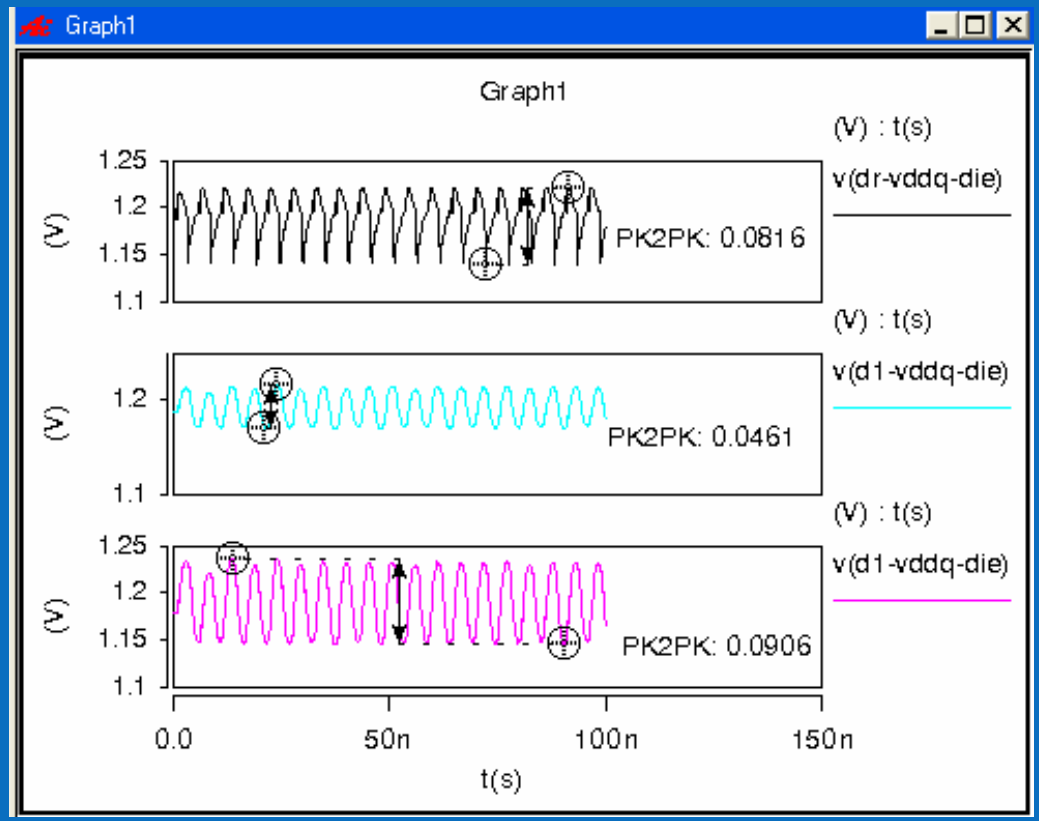
Icc(t) Usage Models



- For calculating the PDN noise
  - Different currents in Vcc and Vss need to be accounted for.
  - Need two out of three currents for modeling: Ivcc, Ivss and Ipad
  - IBIS* application: BIRD 95 can include these currents
- Transmission lines
  - For PDN-noise only analysis, Use individual transmission lines OR use a scaled model of multiple transmission line. Terminate the line/ lines at the far end

Example: Noise Profiles

Noise at the Driver and Receiver End for two termination schemes



Driver-noise

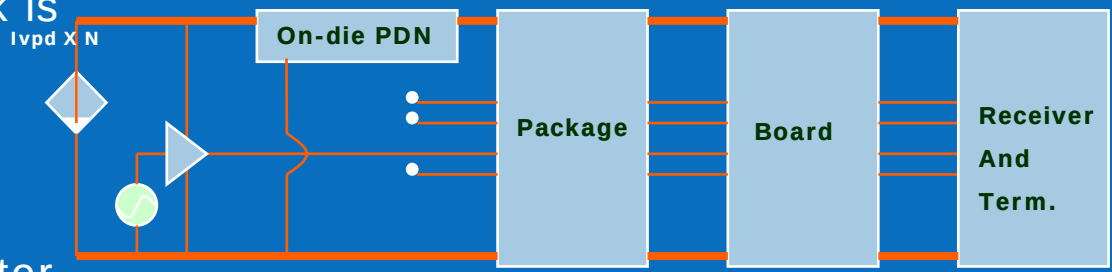
Receiver side noise for CTT

Receiver side noise for Vcc term

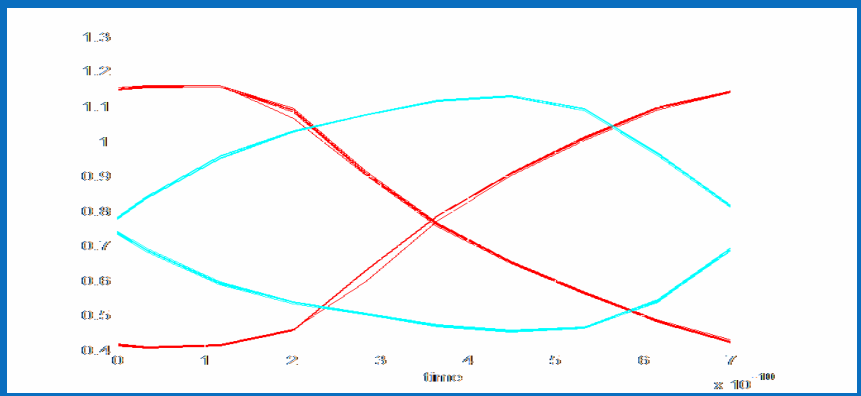
- Driver side noise is very similar for CTT and Vcc terminations
- Receiver side noise is different based on the termination schemes.

PDN Noise impact on timing

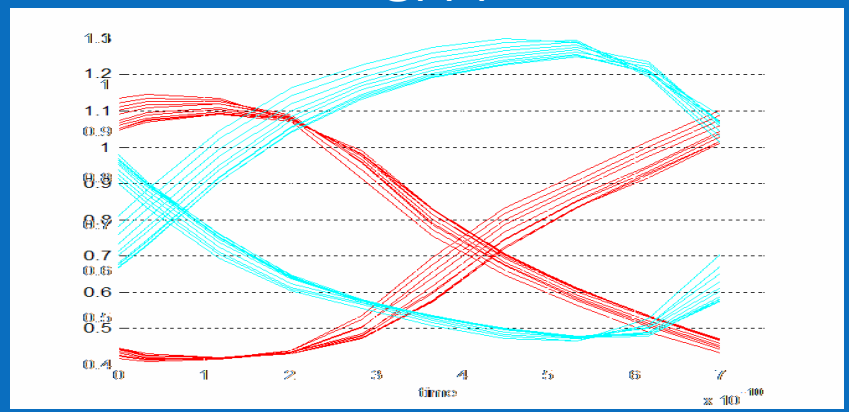
- SI-PI comprehensive deck is generated
- 10 Buffers switching simultaneously 1010
- Cycle to cycle DQ-DQS jitter is measured.



SI only



SI-PI

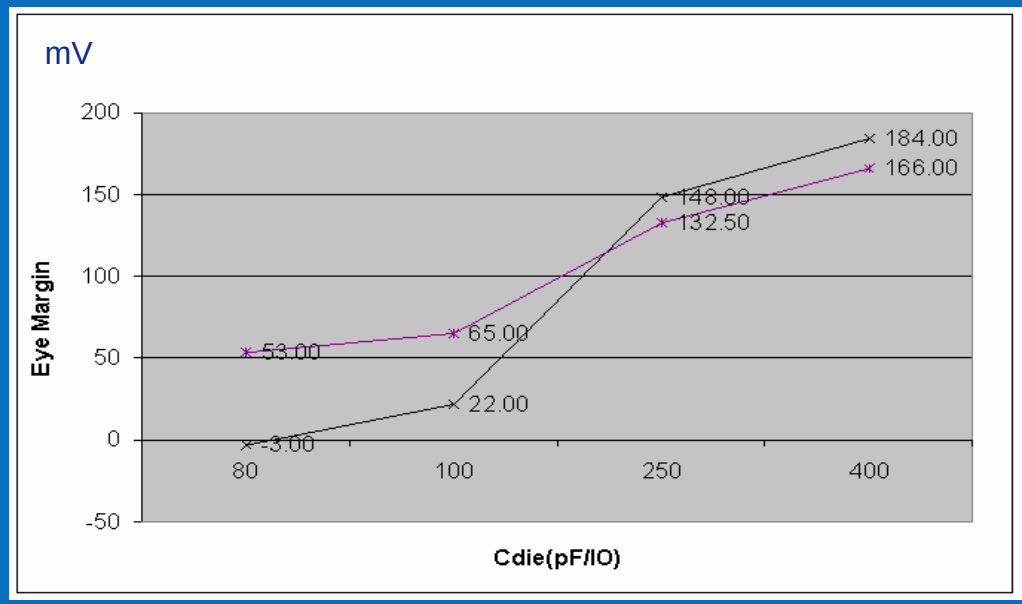


- Inclusion of Icc(t) from different no. of buffers on power node, produces the jitter in SI-PI simulations.

PDN Optimization

- System Level PI-SI models are generated
- Icc(t) is created for 66 buffers
- Two cases are studied: 1333MTPS, 267MTPS

EYE margin vs. Cdie



267MTPS 1333 MTPS

- EYE diagram includes effects due to ISI, crosstalk and SSO
- Cdie/ IO is varied and EYE margin is plotted.
- Higher the Cdie, lower is the SSO noise, hence higher is the EYE margin

Conclusions

- Power Integrity for the single ended systems
  - SSO Noise on the PDN
    - Icc(t) computation comprise of
      - Termination schemes, Driver type, Data Pattern
  - Jitter due to PDN
    - Driver side PD to signal coupling (primary source)
    - Channel PD to signal coupling
  - EYE margin impact due to PDN
    - Cdie optimization
- Behavioral Buffer Model needs to have
  - Ivcc, Ivss, Ipad
  - Dependency on the termination schemes
  - Ability to have noisy voltage source
- Can IBIS* BIRD95/98 address all that?