Case Study of Scheduled Single-Ended Driver Featuring [Test Data]

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Agenda

- Introducing an Unusual Design
  - "Buffer X" on "Interface X"
- Describing the Design with IBIS
  - [Driver Schedule]
- Hurdles to Cross-tool Operation
  - [Driver Schedule] Implementation
- Applying [Test Data] to Aid Correlation
- Tool Correlation
- Comments and Recommendations
- Q & A

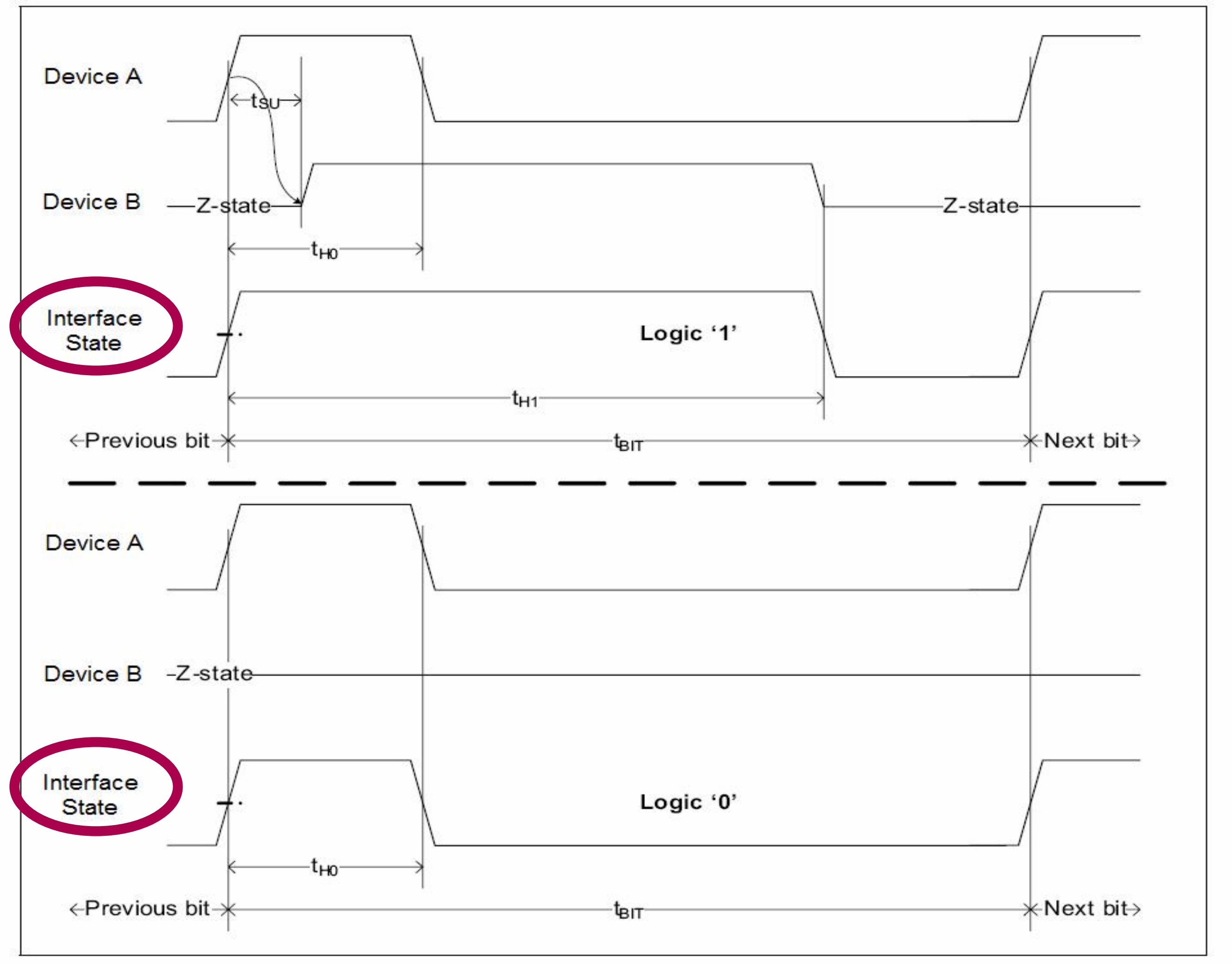
An Unusual Design

“Buffer X” for “Interface X”

- A real interface, in use on real systems
- Many familiar aspects, making IBIS a good modeling approach
  - Interface is single-ended and multi-drop
  - Buffers are complementary (pullup/pulldown) or open-source
  - Edge rates in (low) nanoseconds, with MHz switching rates
- But… several bizarre features confound simple model-making
  - Device contention: multiple components drive simultaneously
  - Logic is both time-and voltage-based
    - *“1” and “0” defined by percent duty cycle at high or low voltages*
  - At least one device uses staged buffer turn-on/turn-off

Example of Timings and Logic

Device B has staged turn-on/ turn-off in this case study



Describing Buffer X with Traditional IBIS

- Contention poses no issue for IBIS per-se
  - Buffer description does not "care" about other buffer states
  - Most tools support multiple-driver topologies
- Unusual logic is a minor hurdle
  - Device A duty cycle for logic "1" or "0" is 25% high V /75% low V
  - Device B is in high-impedance (high-Z) state for logic "0"
  - Device B duty cycle for logic "1" is ~ 75% high V /25% high-Z
  - Contention (and buffer impedances) creates final interface states
  - Can handle logic at tool level, without special IBIS considerations
- Describing Device B requires only a few IBIS features
  - Open-source, using traditional I-V and V-t tables, plus C_comp
  - Buffer uses stages of different impedances
  - Stages are driven by a fixed internal clock, unrelated to interface switching speed

Need [Driver Schedule]!

[Driver Schedule] Refresher (IBIS Cookbook)

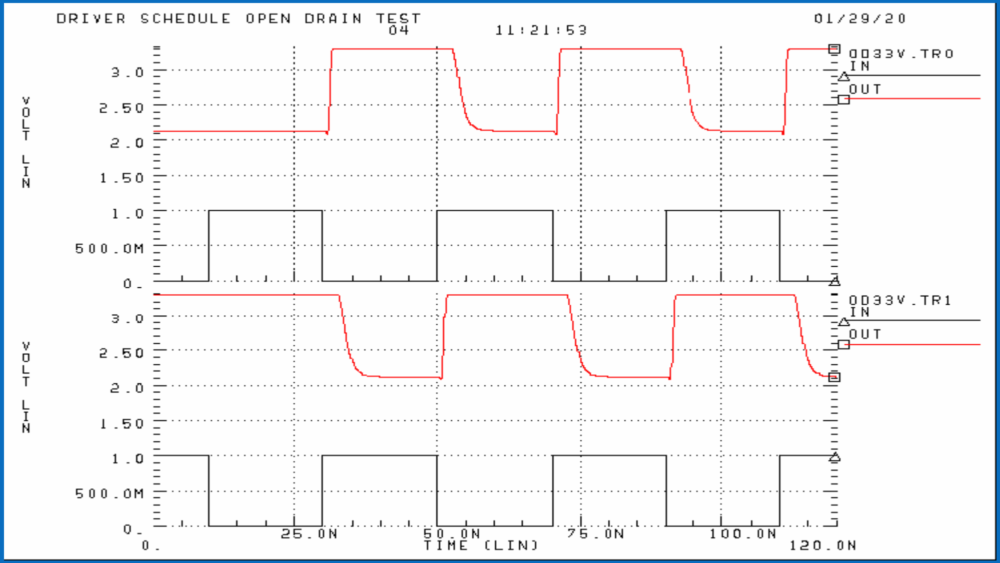
- [Driver Schedule] describes buffer behavior using individual [Model]s controlled by timings given relative to the input stimulus

"Some applications require that a buffer change its strength or transition speed characteristics at fixed times after input stimulus changes."

```
[Driver Schedule]
|
| Model_Name Rise_on_dly Rise_off_dly Fall_on_dly Fall_off_dly
|
P0_stage     0.0000ns    5.0000ns     NA          NA
N0_stage     0.0000ns    NA           0.0000ns    NA
N1_stage     0.3006ns    NA           0.0549ns    NA
N2_stage     0.5481ns    NA           0.1163ns    NA
```

P0 on for 5 ns at/after rising *input* edge

N0, N1 and N2 staggered after any input edge



<u>Inverter [Driver Schedule]</u>
Rise_on_dly = NA
Rise_off_dly = 0 ns
Fall_on_dly = NA
Fall_off_dly = 0 ns

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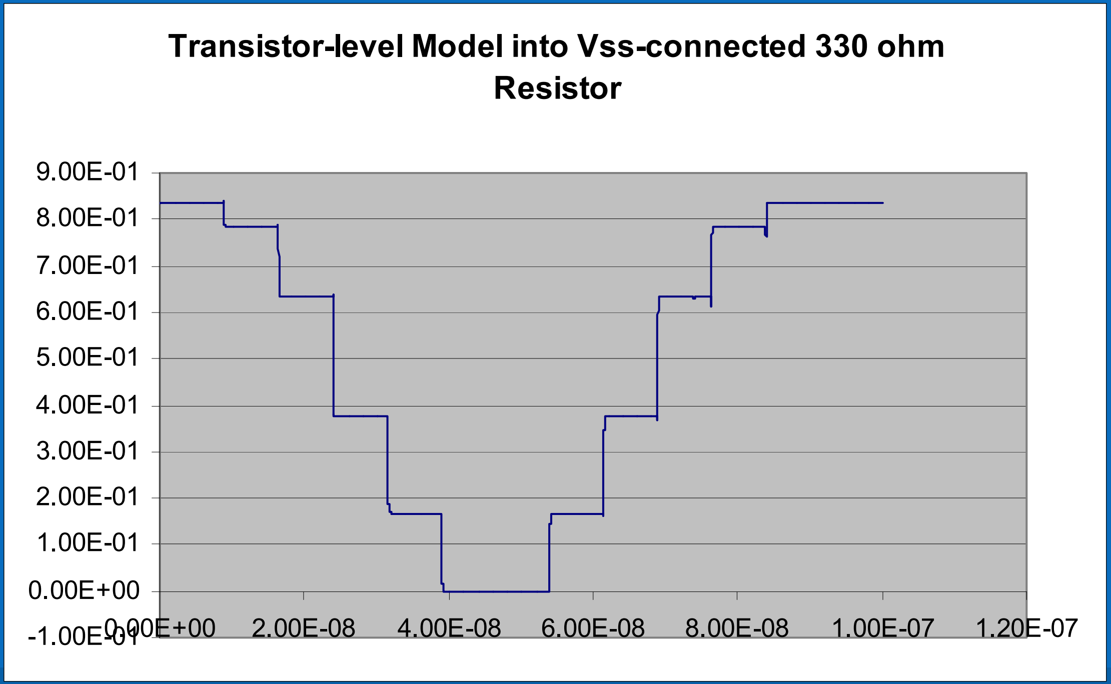
Specific Implementation

- Device B IBIS Implementation
  - Five "legs" or stages, [Pullup] only
  - First stage turns on immediately
  - Following stages turn on at regular periods
  - Only Rise_on_dly and Fall_on_dly used
  - Stage impedances range from ~1500 ohms to ~100 ohms
  - "Top-level" buffer [Model] is a duplicate of leg 1, plus clamp data



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Hurdles to Cross-Tool Operation

- [Driver Schedule] has not been consistently supported in the past
  - Behavior under different tools varied widely (and may still)
  - BIRD88.3 written to ensure better signal initialization of [Driver Schedule]

- To build confidence, we need a way to verify tool output vs. transistor-level design performance and intent
  - Traditional IBIS models are created from transistor-level data
  - Correlation using same conditions produces the same IBIS I-V, V-t data
  - [Driver Schedule] combines several buffers, making correlation of *tool interpretation of IBIS data* critical

IBIS has such a feature:
[Test Data], in Version 4.0

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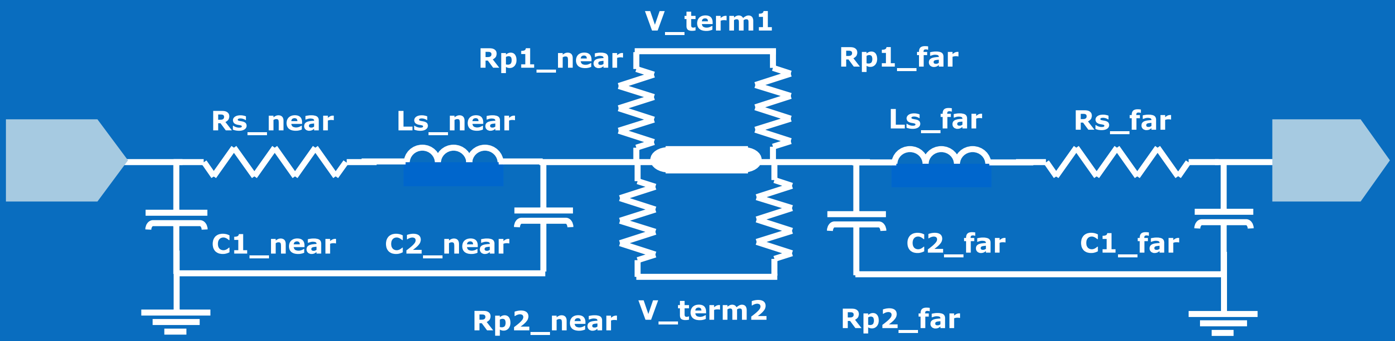
[Test Data] and [Test Load]

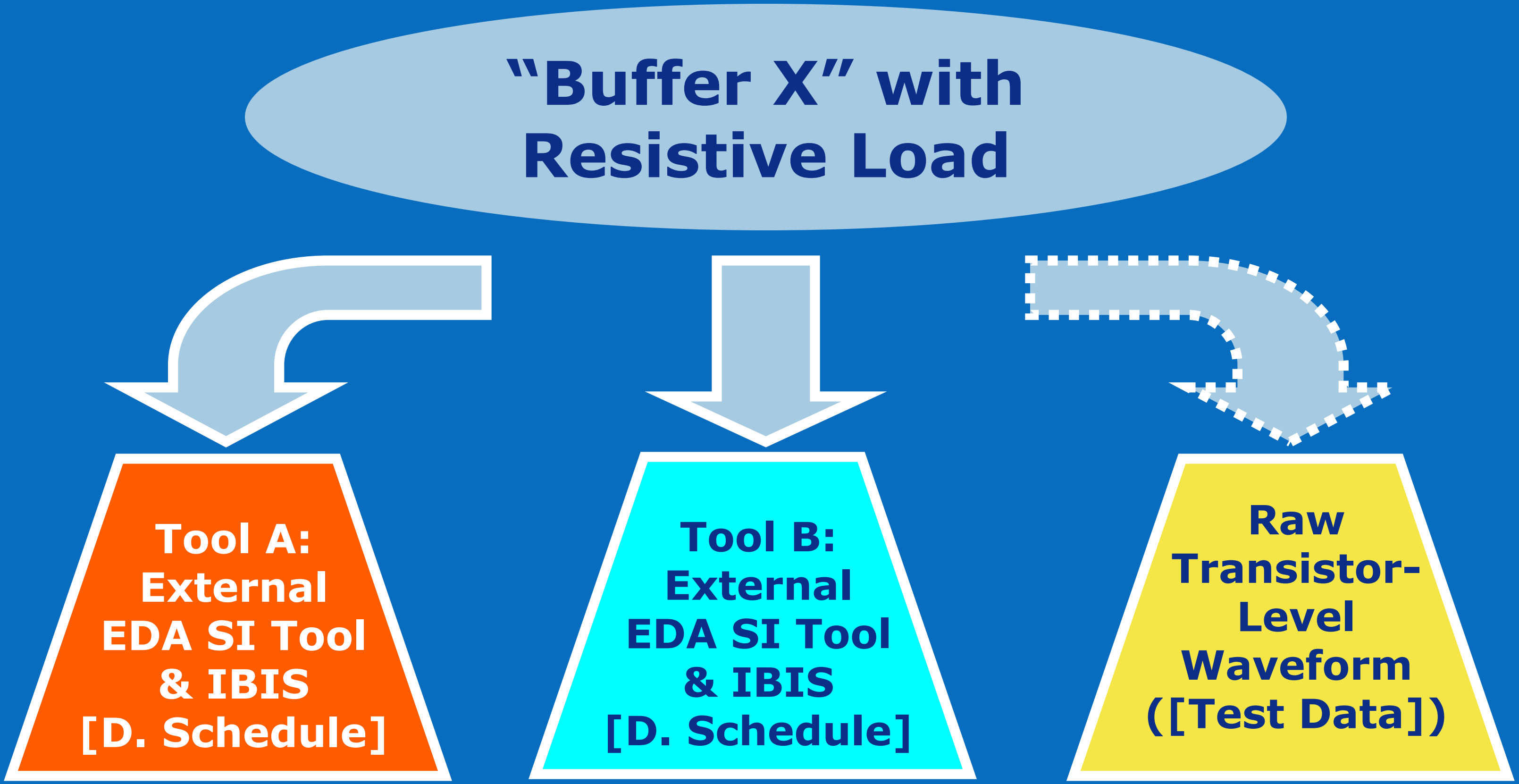
- [Test Data]
  - Contains simple rising and/or falling V-t tables (typical, minimum and maximum)
  - Supports single-ended and differential buffers
  - Links to a particular model by [Model] name
  - Links to a particular load by [Test Load] name
  - Not actually for use in simulations of the associated buffer – correlation only!

- [Test Load]
  - Describes the loading used for the [Test Data] waveform
  - Supports parallel and serial elements, plus at-driver and receiver measurement points



- Procedure for "Buffer X" Device B and [Test Data]/[Test Load]
  - Simply imported the transistor V-t data for a resistive at-pad load from a spreadsheet
    - *1 Rising Waveform and 1 Falling Waveform, "Near End", single-ended*
  - Specified [Test Load] as 330 ohms, 0 V, "Near End"

Testing “Buffer X”



“Buffer X” with Resistive Load

Tool A: External EDA SI Tool & IBIS [D. Schedule]

Tool B: External EDA SI Tool & IBIS [D. Schedule]

Raw Transistor-Level Waveform ([Test Data])

How do the tools “measure up?”

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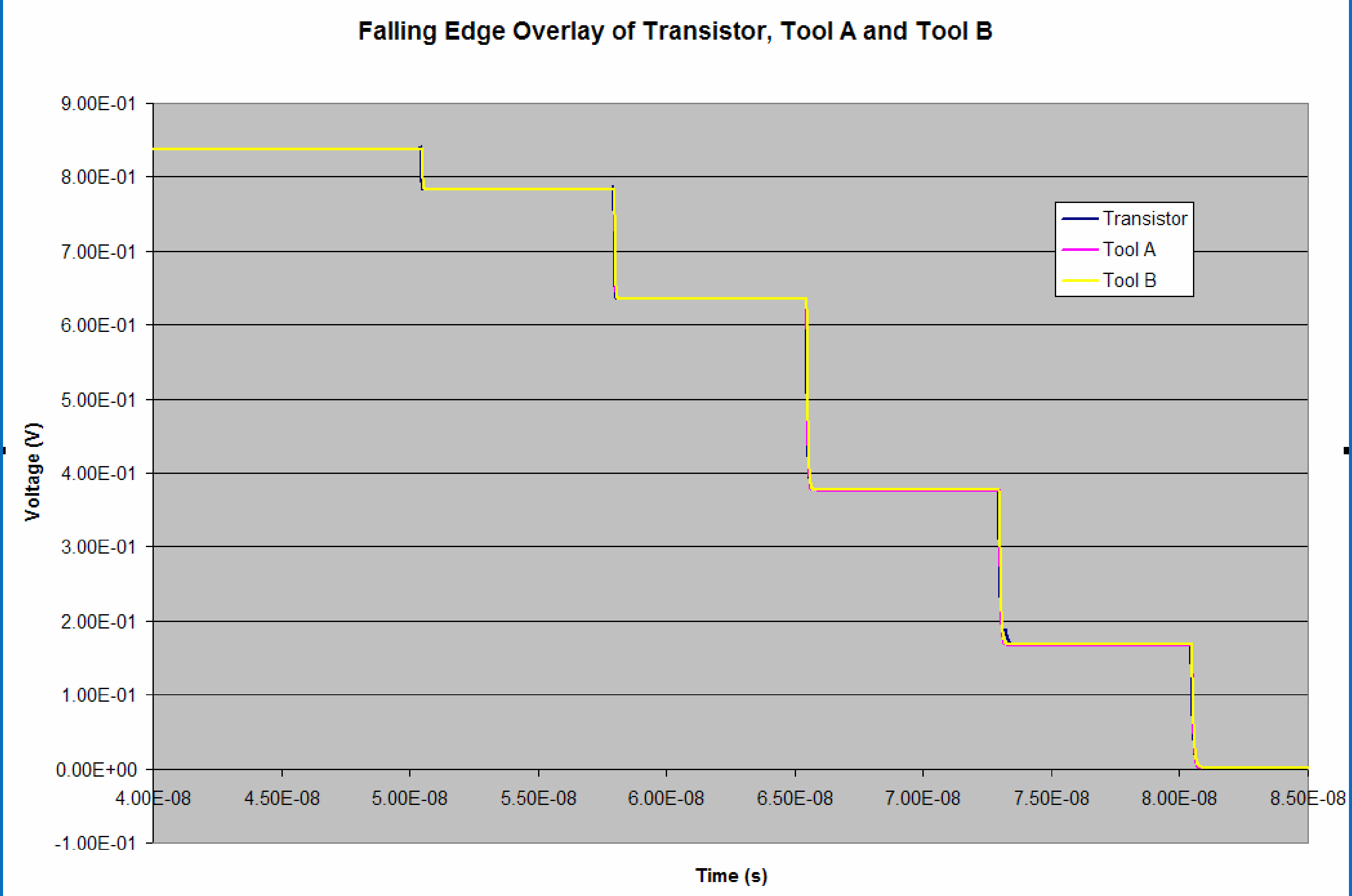
Correlation Overlays – Falling Edge

- Min corner, 330 ohm load to ground at pad



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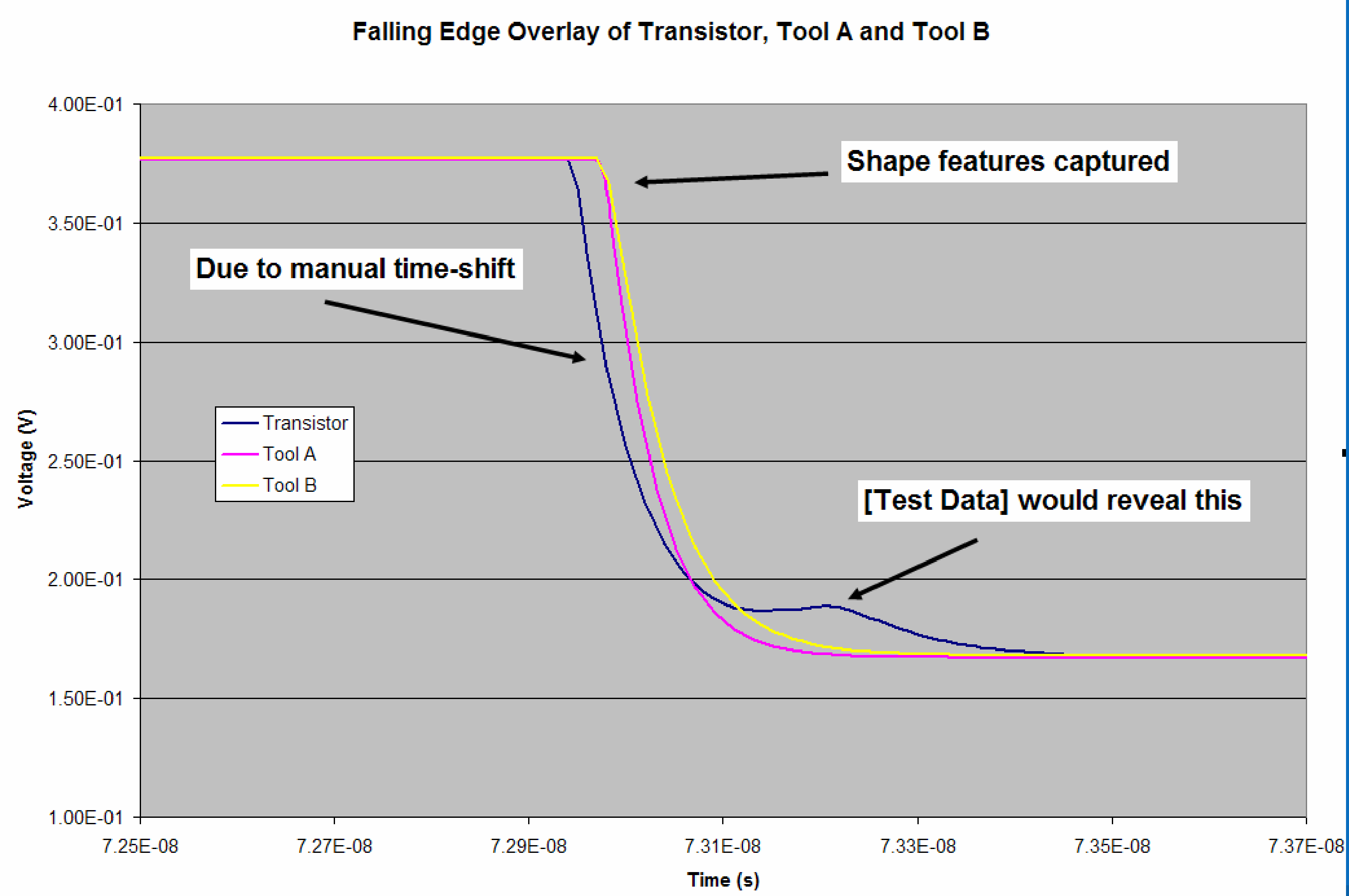
Correlation Overlays – Falling Edge Zoom

- Zoom reveals potential value of [Test Data]



Shape features captured

Due to manual time-shift

[Test Data] would reveal this

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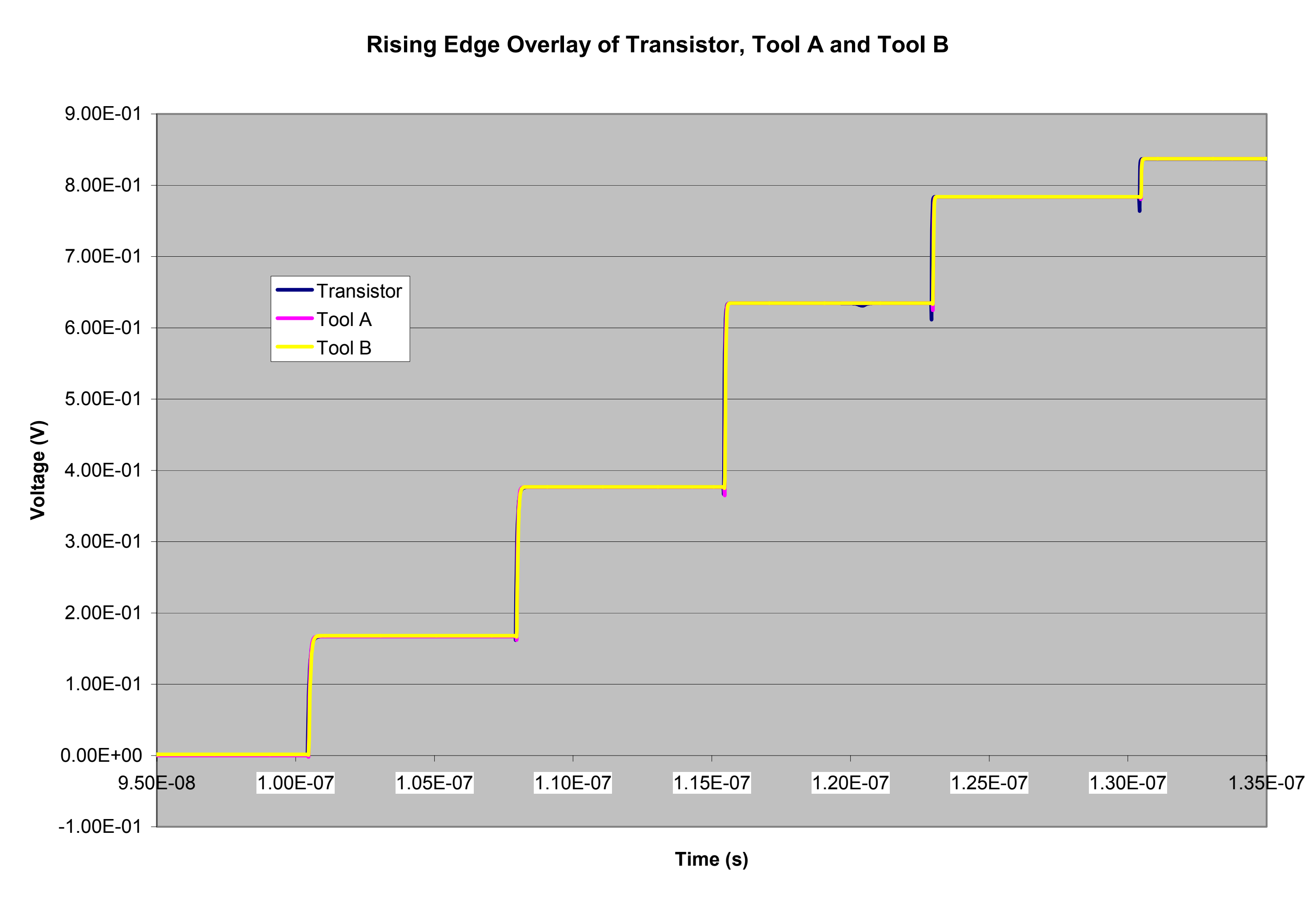
Correlation Overlays – Rising Edge

- Min corner, 330 ohm load to ground at pad



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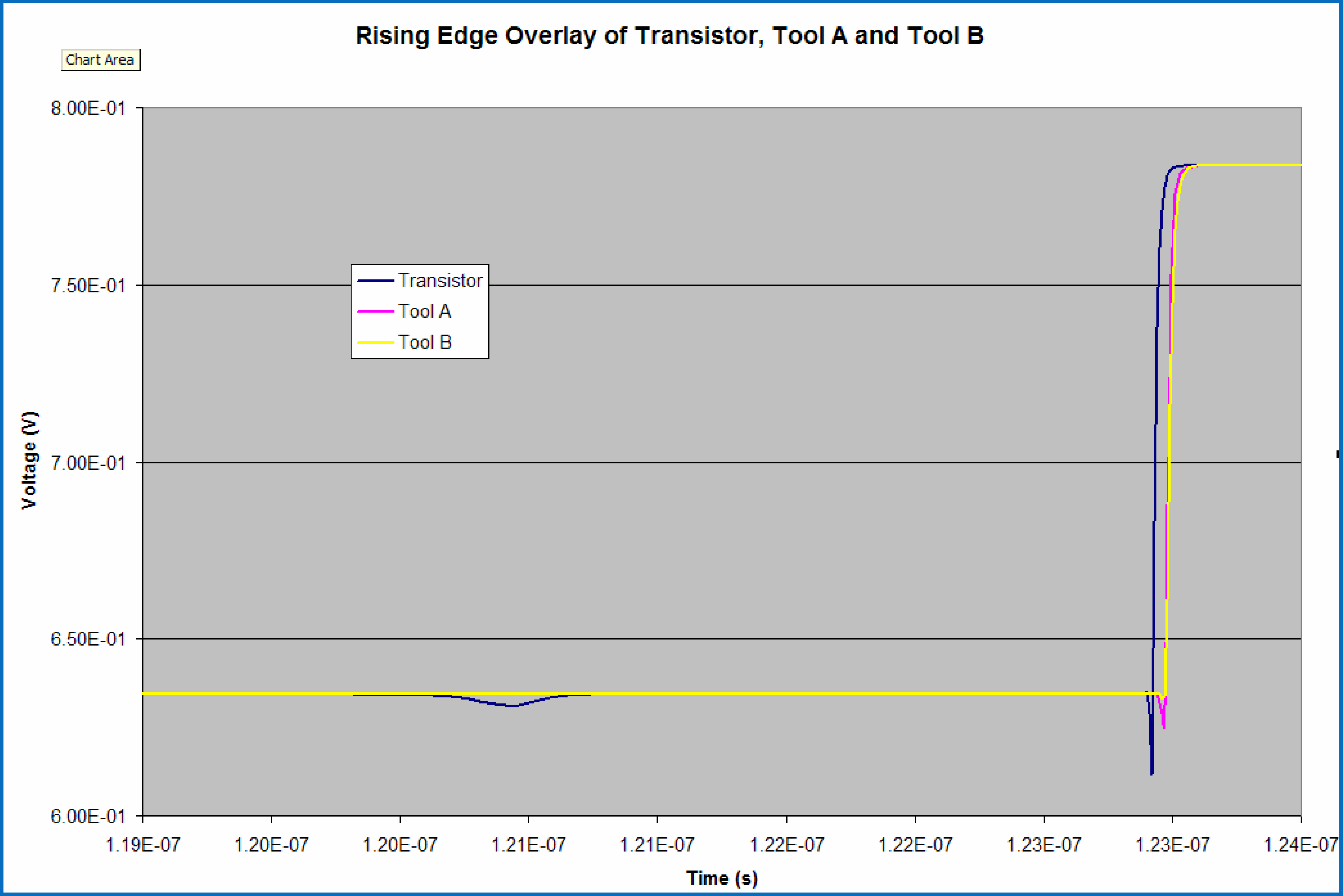
Correlation Overlays – Rising Edge Zoom

- Zoom reveals potential value of [Test Data]



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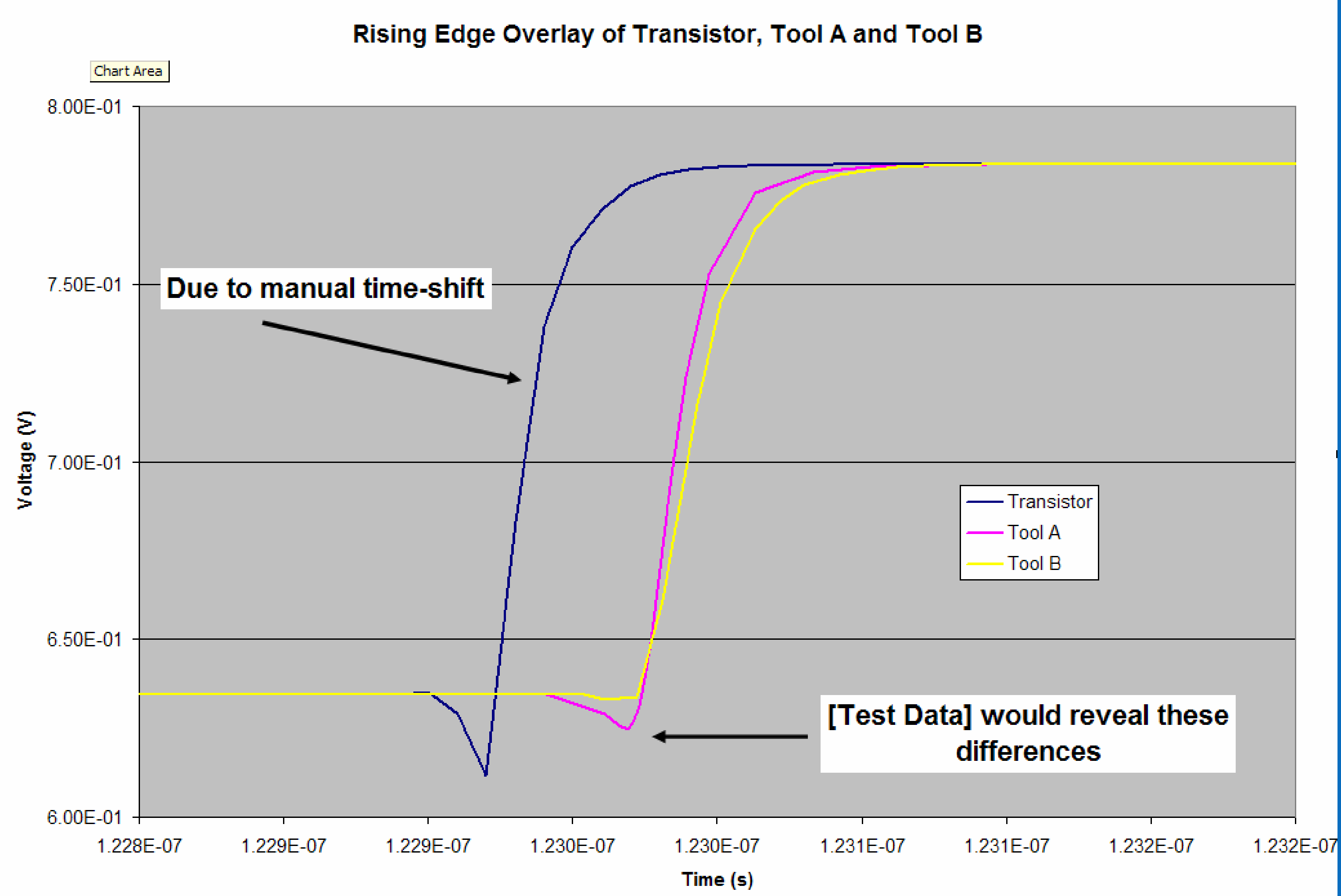
Correlation Overlays – Rising Edge Zoom (2)

- Again, zoom reveals potential value of [Test Data]



Due to manual time-shift

[Test Data] would reveal these differences

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Findings from [Driver Schedule] and [Test Data]

- First, the bad news…
  - Neither of the tools tested supported [Test Data]/[Test Load]
  - The keywords did not cause errors per se, but were simply ignored
  - Therefore, no automated means was available for comparing tool output to [Test Data] information
- Now the good news…
  - Manual comparison of tool to transistor-level data showed good correlation
  - Tools are therefore processing [Driver Schedule] (in this case) correctly
  - Comparisons using [Test Data] transistor-level waveforms vs. tool outputs can reveal tool usage and user setup issues
  - User must decide which differences are relevant to design targets

[Test Data] has value in correlation,
particularly if comparisons could be automated

Extracting [Test Data] places no significant burden
on design/simulation engineer

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Comments

- [Test Data] can add value!
  - For tool vs. transistor or lab correlation, [Test Data] is a clear advantage
  - The keyword is very easy to implement, for simple loads
- Creating [Driver Schedule] models poses problems for model makers
  - Syntax is difficult to understand, even with examples
  - Data almost impossible to gather without:
    - *Applying math to extracted tables*
      - *Buffer ends cycle with apparent impedance of leg 1 || leg 2 || leg 3…*
      - *We want each leg in its own [Model] section*
      - *Design may not enable single-leg transient V-t extraction*
    - *"Cutting" the schematic into pieces*
    - *Relying on design test modes (not always available)*
- Annoyance: Vref, Cref, Rref, Vmeas required for individual leg [Model]s
  - Clearly Vref, etc. are only really are needed at the top-level
  - Individual legs may not even pass through Vmeas level

Recommendations

- [Test Load]
  - Support loss descriptions for transmission lines
  - Clarify whether load is at-pad or at-pin (intent seems to be at-pad)
- [Test Data]
  - Permit custom, defined data patterns (e.g., PRBS)
  - Clarify support of series devices
  - Clarify distinction between simulated and lab-captured data
  - Add Cookbook entries for both [Test Data] and [Test Load]
- [Driver Schedule]
  - Remove requirement for Vmeas, etc. in scheduled models (below top-level)
  - Add additional examples to Cookbook and specification
  - Permit “Combination [Model]” or additive model data, rather than require data for isolated legs individually
    - *Pushes math manipulation of driver data to tool rather than to maker*
    - *Would probably drive tool-to-tool divergence of results*

Thanks to the IBIS Quality Task Group for several of the suggestions above and their continuing [Test Data] analysis!

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Q & A

Leap ahead™