EIA IBIS Open Forum Minutes

Meeting Date: **June 10, 2008**

GEIA STANDARDS BALLOT VOTING STATUS
See last page of the minutes for the voting status of all member companies.

VOTING MEMBERS AND 2008 PARTICIPANTS

Agilent	Sanjeev Gupta, Radek Biernacki, Amolak Badesha Fangyi Rao, [Ian Dodd], Yutao Hu, Vuk Borich Nobutaka Arai, Ludwig Eichingner
AMD	Nam Nguyen
Ansoft Corporation	Steve Pytel, Ricardo Teliuteuesh*, Dan Dvorscak*
Apple Computer	(Bill Cornelius)
Applied Simulation Technology	(Fred Balistreri)
ARM	(Nirav Patel)
Cadence Design Systems	Terry Jernberg, Hemant Shah, Ambrish Varma [C. Kumar], Brad Griffin, Zhen Mu
Cisco Systems	Syed Huq*, Mike LaBonte, AbdulRahman (Abbey) Rafiq Huyen Pham, Emily Yao, Susmita Mutsuddy John Fisher, Paul Ruddy, Jun Li, Jianmin Zhang Luis Boluna, Kelvin Qiu, Jane Lim, Ilyoung Park Rick Brooks, Chris Padilla, Ehsan Kabir
Ericsson	Anders Ekholm
Green Streak Programs	Lynne Green*
Hitachi ULSI Systems	Kazuyoshi Shoji*
Huawei Technologies	Tao Guan, Xiaoqing Dong
IBM	Adge Hawes
Infineon Technologies AG	Christian Sporrer
Intel Corporation	Michael Mirmak*, Rich Mellitz, Wei-hsing Huang* Vishram Pandit*
LSI	[Frank Gasparik], Brian Burdick, [Kim Helliwell]
Marvell Semiconductor	(Itzik Peleg)
Mentor Graphics	Arpad Muranyi*, John Angulo
Micron Technology	Randy Wolff
Nokia Siemens Networks GmbH	Eckhard Lenski, Klaus Huebner, Katja Koller
Samtec	Jim Nadolny, Justin McCalister
Signal Integrity Software	Mike Steinberger, Walter Katz*, Todd Westerhoff* Doug Burns, Mike Mayer, Barry Katz
Sigrity	Sam Chitwood*, Brad Brim*, Ben Franklin Kristopher Stytte, Raymond Chen*
Synopsys	Ted Mido
Teraspeed Consulting Group	Bob Ross*, Tom Dagostino, Al Neves
Texas Instruments	Richard Ward*

Toshiba	Yasumasa Kondo*, Noriyasu Yoshikawa*
Xilinx	David Banas*, Ajay Shah, Suzanne Yiu Mustansir Fanaswalla
ZTE	(Ying Xiong)

OTHER PARTICIPANTS IN 2008

Aeroflex Metelics	David Nguyen
Aica Kogyo	Akihiro Tanaka
Altera	Ravindra Gali, Jing Wu, John Oh, Hui Fu
Avago Technologies	Minh Quach, Sari Tocco
Bayside Design	Elliot Nahas, Kevin Roselle
Celestica	Ihsan Erdin
ECL Advantage	Thomas Iddings
EFM	Ekkehard Miersch
Elma Bustronic	Michael Munroe
Exar	Helen Nguyen
Flextronics	Hasnain Syed
Freescale	Jon Burnett
GEIA	(Chris Denham)
Golden Bridge Networks	Saman Sadigh
ICT Solutions	Steven Wong
Interface Technologies	Dan Waterloo*
IO Methodology	Lance Wang*, Zhi (Benny) Yan, Li (Kathy) Chen
JEITA	Atsushi Ishikawa*
Magma DA	Anand Ramalingam*
NEC	Takeshi Watanabe*
NetLogic Microsystems	Eric Hsu
North Carolina State University	Paul Franzon*
Nokia	Ali Arsian
Nuova Systems	Zhiping Yang
Prentice Hall	Bernard Goodwin*
Physware	Marc Kowalski
Politecnio di Torino	Igor Stievano
Qimonda AG	Md Morshed Alam Heial, Suhas Jawale
Siemens AG	Manfred Maurer, Annika Woehner
Simberian	Yuriy Shlepnev
SimLab Software GmbH	Heiko Grubrich
Tektronix	Steve Corey
TietoEnator GmbH	Heinz-Hartmut Ibowski
Tyco Electronics	Chad Morgan
Vertical Circuits	Mark Egbers
Xsigo Systems	Robert Bada
Zuken	Michael Schaeder, Ralf Bruening
Independent	Guy de Burgh, Ardy Forouhar, Dave Galloi

Kazuhiko Kusunoki

In the list above, attendees at the meeting are indicated by *. Principal members or other active members who have not attended are in parentheses. Participants who no longer are in the organization are in square brackets.

UPCOMING MEETINGS

The bridge numbers for future IBIS teleconferences are as follows:

Date	Telephone Number	Meeting ID
June 27, 2008	1-866-432-9903	121587005

All meetings are 8:00 AM to 9:55 AM US Pacific Time. Meeting agendas are typically distributed seven days before each Open Forum. Minutes are typically distributed within seven days of the corresponding meeting. When calling into the meeting, press 1 to attend the meeting, then follow the prompts to enter the meeting ID. For new, local international dial-in numbers, please reference the bridge numbers provided by Cisco Systems at the following link:

http://www.cisco.com/web/about/doing_business/conferencing/index.html

NOTE: "AR" = Action Required.

INTRODUCTIONS AND MEETING QUORUM

The IBIS Open Forum Summit was held in Anaheim, California at the Marriott Hotel during the 2008 Design Automation Conference (DAC). 26 people from 19 organizations attended. The attendees were approximately evenly split between EDA tool vendors, model users and model makers.

The notes below capture some of the content and discussions. The meeting presentations and other documents are available at:

http://www.ibis-information.org/summits/jun08/

Michael Mirmak opened the meeting by thanking event sponsors Mentor Graphics and the IBIS Open Forum for their financial and logistical support. Michael also thanked the presenters and participants for attending. Each attendee was asked to introduce him or herself.

Michael asked if there were any new issues or discussion items to add to the agenda. No issues were raised.

PRESENTATIONS AND DISCUSSION TOPICS

The rest of the meeting consisted of presentations and discussions. These notes capture some of the content and discussion. More details are available in the documents uploaded to the location noted above.

IBIS CHAIR'S REPORT

Michael Mirmak, Intel Corporation

Michael Mirmak summarized the current state of the IBIS Open Forum and its activities. IBIS membership in 2007 was 34 [corrected later to 32], with member renewals continuing. Successful summits were held in San Jose, California and Munich, Germany, with events in Japan and China planned for November. A summit in Taiwan is under active consideration. He added that the merger of the GEIA and ITAA has not resulted in significant changes to day-to-day IBIS operations.

The current BIRD listing was summarized. Eight changes to the IBIS specification have been approved and are expected to be included in the IBIS 5.0 release scheduled for later this year. Michael continued by thanking the members and current officers -- Syed Huq, Randy Wolff, Lance Wang and Bob Ross -- for their help in continuing to support IBIS activities over the past year.

He completed his talk with a call to action, proposing that IBIS members get more involved in development of advanced specifications like PCI Express* 3.0 and USB 3.0. The industry-wide reach, increased speeds and need for eye diagram-based measurements in these specifications present a challenge for IBIS, while also providing an opportunity to demonstrate IBIS features like AMI and multi-lingual support. Michael concluded with specific recommendations to the three major sectors involved with IBIS, suggesting that development of IBIS support for these specifications while they're still being written would help IBIS avoid being seen as technologically "behind."

Richard Ward commented that PCI Express* and USB are not the only high-speed specifications now in development. Two 10 Gb/s fiber-based specifications are now in development that might benefit from IBIS support: SFF8431 and SFF8461. David Banas and Arpad Muranyi noted that support of upcoming optical specifications has been raised to IBIS members before and would be of benefit in the long term.

COMMON ISSUES IN MODELS SUBMITTED TO THE IBIS MODEL REVIEW COMMITTEE

Lynne Green, Green Streak Programs

Lynne provided an overview of the most prevalent problems seen in models provided to the IBIS Model Review Committee. She explained the role of the committee chair in accepting models, providing initial comments and then distributing them to the committee members for their individual review.

Most commonly, less than half of the received models do not pass the IBISCHK parser, because the maker or user simply had not run the parser checks on the file. Non-monotonicity errors also abound, though these may sometimes be the result of clamp subtraction changing the appearance of otherwise monotonic waveforms. Other issues include models with clamps that do not pass through the I-V origin when on-die terminations are not present (and leakage is not anticipated to be significant), plus mismatches between I-V and V-t data. She observed that many modeling issues could be detected by graphical analysis rather than parser checks.

Lynne concluded by recommending that the Cookbook and parser be more prominently featured on the IBIS website. Further, example models, both good and bad, could be shown on-line to educate model makers on effective and ineffective techniques. Finally, Lynne recommended that a greater focus be taken by the IBIS Open Forum on "newbies" or new IBIS model makers and users, to ensure that good practices are understood and adopted by those just entering the industry.

CASE STUDY OF SCHEDULED SINGLE-ENDED DRIVER FEATURING [TEST DATA]

Michael Mirmak, Priya Vartak, Ted Ballou, Intel Corporation

Michael presented a summary of work related to an unusual buffer and interface design at Intel. Called "Buffer X" and "Interface X" for this presentation, the electrical behavior of this system involves time-based as well as voltage-based logic levels, similar to pulse-width modulation. Because of the timed turn-on and turn-off of a particular implementation of Buffer X, [Driver Schedule] was used to model the buffer design in IBIS, and [Test Data]/[Test Load] used to show correlation quality of the IBIS buffer behavior under user tools versus transistor-level data.

Michael also showed actual [Driver Schedule] performance of two industry simulation tools, showing the waveform quality against the transistor-level data in [Test Data]. He concluded by noting that, while tools seem to be doing better at supporting [Driver Schedule], the keyword is difficult to use in models. Fortunately, [Test Data] and [Test Load], while not automatically supported by any known tools, permit model makers to correlate tool behavior against design behavior.

Todd Westerhoff noted that many of the differences shown between transistor-level and IBIS-based results for [Driver Schedule] may quite simply not have any impact on the operation of the bus. Arpad Muranyi suggested that some of the differences may be attributed to the section-by-section approach needed to model [Driver Schedule] as separate buffers. Separating the buffer into parts may eliminate coupling or other effects that could show up in the actual design as a result of one section influencing the others' behavior.

Walter Katz suggested that [Test Data] might be made more useful if it were provided at different frequencies, perhaps in separate files, with strong separation of typical, minimum and maximum corners.

SERDES MODELING: IBIS-AMI CORRELATION

Todd Westerhoff, Signal Integrity Software (SiSoft)

Todd summarized recent activity in correlating IBIS-AMI models of XAUI and PCI Express* Generation 1 and 2 to bitstream simulations. Correlation involved both direct SPICE waveforms and IBIS-AMI outputs using bit patterns and step/pulse response processing through IBIS-AMI. The number of bits ranged from 10,000 to over 1 million.

Todd also showed comparisons between waveform processing done by the two existing versions of the IBIS-AMI toolkit, plus IBIS-AMI processing versus direct analysis under IBM's HSSCDR using HSS6G technology. Matching across all comparisons was extremely close, even when five to seven S-parameter segments were cascaded to represent the system behavior.

Syed Huq inquired about silicon correlation being a critical measure of success. Todd agreed that this would be critical, but was not part of this study.

David Banas requested clarification on the meaning of "TX_Init" and how it is used in this analysis. The naming and diagrams imply that TX_Init only involves the transmitter's output waveforms but suggests the rest of the system is not involved. Todd clarified that TX_Init's waveforms do indeed include unequalized transmitter and full system effects, in order to show how the driver stimulus affects the system as well as how the system reflections, discontinuities, etc. change the step/impulse response.

CURRENT IBIS-AMI SUPPORT

Arpad Muranyi, Mentor Graphics Corporation

Arpad began his presentation by revisiting benchmarks for VHDL-AMS, IBIS-AMI and The MathWorks' MATLAB* processing the same algorithmic buffer representation. He noted that processing waveforms in a single call rather than splitting the waveforms into multiple calls to a "GetWave" function can result in significantly longer processing times. Simply put, calling the GetWave function several times can decrease overall algorithmic processing times, more closely aligning VHDL-AMS and ANSI C implementations in terms of performance.

He continued by noting that VHDL-AMS can be used to process IBIS-AMI code directly, though the implementation was specific/proprietary to Mentor Graphics. Relevant sections of the code for the VHDL-AMS/C-wrapper implementation of the IBIS-AMI interface were shown and discussed in the presentation.

ELECTION OF OFFICERS

Michael Mirmak announced the available positions and responsibilities. He also noted that the existing officeholders were willing to continue as nominees. Mr. Chungxing Huang of Huawei Technologies was nominated by e-mail for the position of webmaster. No other nominations were received. The following candidates were elected by the voting membership present at the Summit as officers for 2008-2009:

Chair:	Michael Mirmak, Intel Corp.
Vice-Chair:	Syed Huq, Cisco Systems
Secretary:	Randy Wolff, Micron Technology
Postmaster:	Bob Ross, Teraspeed Consulting Group
Webmaster:	Syed Huq, Cisco Systems
Librarian:	Lance Wang, IO Methodology, Inc.

Michael thanked the outgoing officers and congratulated the new officers. Arpad Muranyi noted that perhaps elections would be better held at DesignCon rather than DAC, as the attendance at the DesignCon event appears to be higher.

Later during the meeting, Michael presented some commemorative items to the outgoing board members, and Bob Ross presented one to Michael.

POWER INTEGRITY FOR SINGLE ENDED SYSTEMS

Vishram Pandit and Myoung Joon Choi, Intel Corporation

Vishram summarized various types of system single-ended interface terminations, including Vcc-terminated, Vss-terminated and center-tap terminated arrangements, to compare the relative supply current changes. As minimizing the change in supply current with time (dI/dt) is critical for good power integrity design, analyzing the whole system, rather than just the driver or just the receiver, is required.

Vishram also reviewed Icc(t) as a means of characterizing the noise on the buffer's power delivery network as SSO effects take hold. This effect can be scaled to address SSO effects on groups of buffers. Studies of the same termination options as used in the dI/dt analysis show that Icc(t), and therefore SSO, changes with different termination schemes.

Vishram noted that, in collecting Icc(t), current in power and current in ground rails at the buffer side are not necessarily equal, due to currents in or out of the pad. Vishram concluded by asking whether BIRD95 and BIRD98 can handle these situations. The overall response from the audience was affirmative, though Vishram and David Banas noted that pre-driver effects were increasingly important. Only final stages of the pre-driver were included in the study. Some logic and other stages of the pre-driver were not included. Vishram emphasized that the currents in power and ground were coming not only from the pre-driver but also from the type of termination scheme.

Bob Ross observed that BIRD95 can represent the distribution of currents involving Vcc, Vss and the I/O pad into account. However, he added that the V-t tables in an IBIS model imply a certain pad current, particularly if a resistive load is used. Therefore, BIRD95 only needs to include Vcc and Vss currents to provide a complete power delivery representation.

ELECTRICAL MODELING AND MODEL REPRESENTATIONS FOR PACKAGE INTERCONNECTS AND POWER DELIVERY NETWORKS

Brad Brim and Sam Chitwood, Sigrity

Brad summarized various types of industry package designs and analysis types to suggest that, with combined SI and PI (power integrity) analysis becoming a requirement for today's more complex systems, the model formats available for interconnects are inadequate. Signal integrity behavior is influenced by return path and rail variations, making accurate modeling of references and planes imperative. Most package interconnect modeling formats, including those available under IBIS, use only static extraction of L and C values and ignore return paths. Alternatives include S-parameters, ICM, arbitrary circuit descriptions and transmission line models like the W-element. However, some of these formats don't include return path effects either, or in the case of ICM, only represent line-to-line coupling and not section-to-section coupling (as would be seen in serpentine trace routes, for example). Further, often S-parameter data is converted to a circuit representation through vector-fitting, which may cause causality and/or passivity issues.

Brad called on the industry, specifically the IBIS Open Forum, to help develop a general standard for broadband multi-stage RLCK models (where conductivity G is considered part of "R" in the name but same-line section-to-section coupling K is included). These would be efficient to generate and simulate and are extracted from full-wave S-parameters, but involve

optimization of RLC circuit components into a circuit model that matches the broadband response needed. Standard header information for connectivity could help support chip-package co-design and avoid the connectivity errors to which arbitrary SPICE netlists can contribute. ICM partially solves the problem, but without all the general circuit features and coupling relationships that would make it entirely suitable.

TOUCHSTONE ISSUES

Bob Ross, Teraspeed Consulting Group

Bob provided a summary of current technical issues within the development of Touchstone 2.0. At present, the IBIS Ad Hoc Interconnect Task Group has taken up discussion of support for mixed-mode network parameters, after initially deferring inclusion until Touchstone 3.0. Supporting mixed-mode involves representing interactions between ports in a consistent way, including both differential and common-mode relationships.

A key issue is whether the assignment of positions within a matrix is fixed based on the relationships being described (for example, SDD representing differential stimulus and differential response always appearing in the upper left quadrant of a matrix). A generalized format would follow an order presented elsewhere in the file as a vector, which also determines the off-diagonal data positions. This ordering vector would also contain information on the relationships of interest within the matrix (i.e., single-ended, differential, common-mode), without forcing particular relationships into particular positions in the matrix.

A further issue is specification of impedances. While the original Touchstone and early Touchstone 2.0 drafts defined single-ended reference impedances, the mixed-mode format could permit mixed-mode references, linking two ports sharing a common reference. Unequal references could cause data processing issues. Bob concluded by noting that the format was still under development and that some of the impedance specification issues were still to be settled.

Michael Mirmak noted that one advantage of the new format would be that it could enable both mixed-mode and a reduced file size due to the limited list of port relationships made explicit in the file.

NEXT GENERATION I/O MACROMODELING

Paul Franzon, Ting Zhu, North Carolina State University, Ambrish Varma, Cadence

Paul provided a brief overview of current macromodeling and behavioral buffer modeling work being conducted at North Carolina State University (NCSU). Paul expressed concern that the use of IBIS as a modeling standard could diminish without an “influx of new technology.” Supporting new technology could include templates for VHDL-AMS, Verilog-AMS or other types of macromodeling approaches. Similarly, BIRD95/97 support with “black box” methods, including correction factors for today’s tables and charge conservation improvements to SPICE models, could be part of advanced research to improve IBIS. NCSU is pursuing a US National Science Foundation grant to finance the work of a Ph.D. student for three years in developing these advanced techniques. Paul concluded by requesting letters of support for this effort and distributing a questionnaire to IBIS Summit attendees, to clarify the technical areas in which they were most interested.

Michael Mirmak inquired whether a focus on analog-only buffer modeling was appropriate, given the increasing need for statistical modeling, particularly for SerDes. Paul agreed this was worth investigation.

DISCUSSION

Michael opened the floor for discussion topics. Lynne Green asked about better educating new IBIS users and model makers. Suggestions for improvement from the attendees included

- better support, documentation and examples for S2IBIS3 usage
- web improvements, including more Cookbook prominence and a search engine
- differential model creation support, either in S2IBIS3 or other tools
- better education on SPICE tool usage with IBIS
- better education on signal integrity concepts and modeling methodologies

Attendees noted that signal integrity books mentioning IBIS and general modeling are on the increase. In addition, signal integrity university courses were now available from the University of South Carolina and San Jose State University. Michael noted that the modeling and SerDes SI portions of the USC curriculum, co-sponsored by Intel, are now freely available on-line:

http://www.intel.com/education/highered/signal/index.htm

Lynne Green volunteered to act as a coordinator for IBIS education information. Participants also noted that a panel discussion at DesignCon might be highly beneficial, as would polling non-IBIS SI engineers to find out the needs they have that are not currently served by IBIS.

The discussion turned to what is needed within IBIS to keep it relevant. Todd Westerhoff observed that increasing amounts of detail being demanded by some model makers and users tends to disadvantage IBIS, despite additional detail not necessarily increasing accuracy. Arpad Muranyi added that the current specifications were written by those not necessarily working on the most advanced interfaces or technologies. Suggestions for IBIS improvements included:

- timing models at the buffer level
- tests for correlation plus test data separate from the model data
- data on enable/disable transitions and their effects on outputs
- true differential buffer support
- overclocking support
- advanced packaging support
- Icc(t) support, if not already part of BIRD95
- measurement rules that correspond to industry standards (e.g., DDR, eye masks)
- simplification of IBIS data formatting
- bi-modal and/or frequency-dependent C_comp
- flexible controls (e.g., parameters or nodes that can control buffer behavior separate from requirements for new I-V and/or V-t data)

Participants suggested a DesignCon paper on IBIS technologies (ICM, IBIS 5.0, Touchstone 2.0, etc.) might be useful. However, Todd Westerhoff noted that only about 1 out of every 30 papers submitted is accepted, and the level of technological content is expected to be high.

Lynne Green suggested that more measurement-based IBIS generation tools should be made available, to pull package and I/O information from components, using a test board or platform. Arpad suggested that PCB resonances may make de-embedding these components difficult. David Banas agreed, noting that a recent test effort was halted due to an incorrectly specified impedance on a test board trace.

The discussion moved on to current usage models for IBIS. At present, many IBIS model makers avoid using the built-in package keywords and treat IBIS as a die-only or even buffer-only format, rather than a complete model of an entire component. Michael Mirmak suggested that IC vendors may have a pre-layout-only viewpoint, where models are used to generate layout rules and integration with post-layout analysis isn't needed. Todd Westerhoff responded that post-layout is quite critical, as rules are rarely comprehensive or universally applicable. David Banas added that the utility of post-layout analysis is eroded by excessive guardbanding in models. Testing to specifications is what's ultimately important to designers. He added that most testers have only a 100 ps resolution where simulators and specifications are approaching sub-picosecond precision. He and Todd added that, with increasing speeds and edge rates shortening wavelengths, at-die or at-pad specifications are required but probing is difficult to impossible, making at-pin specifications less useful and simulations critical.

Walter Katz observed that the AMI efforts have worked because of the close collaboration of tool vendors and IC designers. Vishram responded that die models for BIRD95/98 efforts may not be forthcoming as the needs for power delivery analysis increase, due to IP concerns. Sam Chitwood added that pad capacitance and overall die capacitance information is needed for a true analysis, but on-die decoupling information can reveal proprietary die size information. Others suggested that behavioral approaches or even encryption might find an application here. For power delivery, a PCB impedance target over a bandwidth is needed, and this specification must be translatable to a component-level specification or requirement.

CONCLUDING ITEMS AND NEXT MEETING

The discussion concluded at approximately 4:40 PM. Michael Mirmak asked about additional topics, but none were proposed. He repeated his thanks to the co-sponsors and adjourned the meeting.

The next Open Forum teleconference will be held June 27, 2008 from 8:00 AM to 10:00 AM US Pacific Time.

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NOTES

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This meeting was conducted in accordance with the GEIA Legal Guides and GEIA Manual of Organization and Procedure.

The following e-mail addresses are used:

majordomo@eda.org

In the body, for the IBIS Open Forum Reflector:
subscribe ibis <your e-mail address>

In the body, for the IBIS Users' Group Reflector:
subscribe ibis-users <your e-mail address>

Help and other commands:
help

ibis-request@eda.org

To join, change, or drop from either or both:
IBIS Open Forum Reflector (ibis@eda.org)
IBIS Users' Group Reflector (ibis-users@eda.org)
State your request.

ibis-info@eda.org

To obtain general information about IBIS, to ask specific questions for individual response, and to inquire about joining the EIA-IBIS Open Forum as a full Member.

ibis@eda.org

To send a message to the general IBIS Open Forum Reflector. This is used mostly for IBIS Standardization business and future IBIS technical enhancements. Job posting information is not permitted.

ibis-users@eda.org

To send a message to the IBIS Users' Group Reflector. This is used mostly for IBIS clarification, current modeling issues, and general user concerns. Job posting information is not permitted.

ibis-bug@eda.org

To report ibischk parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/bugs/ibischk/
http://www.eda.org/ibis/bugs/ibischk/bugform.txt

icm-bug@eda.org

To report icmchk1 parser BUGs. The BUG Report Form resides along with reported BUGs at:

http://www.eda.org/ibis/icm_bugs/
http://www.eda.org/ibis/icm_bugs/icm_bugform.txt

To report s2ibis, s2ibis2 and s2iplt bugs, use the Bug Report Forms which reside at:

http://www.eda.org/ibis/bugs/s2ibis/bugs2i.txt
http://www.eda.org/ibis/bugs/s2ibis2/bugs2i2.txt
http://www.eda.org/ibis/bugs/s2iplt/bugsplt.txt

Information on IBIS technical contents, IBIS participants and actual IBIS models are available on the IBIS Home page:

http://www.eigroup.org/ibis/ibis.htm

Check the IBIS file directory on eda.org for more information on previous discussions and

results:

http://www.eda.org/ibis/directory.html

All eda.org documents can be accessed using a mirror:

http://www.ibis-information.org

Note that the "/ibis" text should be removed from directory names when this URL mirror is used.

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GEIA STANDARDS BALLOT VOTING STATUS

I/O Buffer Information Specification Committee (IBIS)

Organization	Interest Category	Standards Ballot Voting Status	April 25, 2008	May 16, 2008	June 6, 2008	June 10, 2008
Advanced Micro Devices	Producer	Inactive			√	
Agilent Technologies	User	Inactive				
Ansoft	User	Inactive				
Apple Computer	User	Inactive				
Applied Simulation Technology	User	Inactive				
ARM	Producer	Inactive				
Cadence Design Systems	User	Active	√		√	
Cisco Systems	User	Active	√		√	√
Ericsson	Producer	Active	√	√	√	
Green Streak Programs	General Interest	Inactive				√
Hitachi ULSI Systems	Producer	Inactive				√
Huawei	User	Inactive	√	√		
IBM	Producer	Active	√	√	√	
Infineon Technologies AG	Producer	Inactive				
Intel Corp.	Producer	Active		√	√	√
LSI	Producer	Active	√	√	√	
Marvell Semiconductor	Producer	Inactive				
Mentor Graphics	User	Active		√	√	√
Micron Technology	Producer	Inactive	√	√		
Nokia Siemens Networks	Producer	Active	√		√	
Samtec	Producer	Inactive				
Signal Integrity Software	User	Active	√	√		√
Sigrity	User	Inactive				√
Synopsys	User	Inactive				
Teraspeed Consulting	General Interest	Active	√	√	√	√
Texas Instruments	Producer	Inactive				√
Toshiba	Producer	Inactive				√
Xilinx	Producer	Active			√	√
ZTE	User	Inactive				

CRITERIA FOR MEMBER IN GOOD STANDING:

- MUST ATTEND TWO CONSECUTIVE MEETINGS TO ESTABLISH VOTING MEMBERSHIP
- MEMBERSHIP DUES CURRENT
- MUST NOT MISS TWO CONSECUTIVE MEETINGS

INTEREST CATEGORIES ASSOCIATED WITH GEIA BALLOT VOTING ARE:

- USERS - MEMBERS THAT UTILIZE ELECTRONIC EQUIPMENT TO PROVIDE SERVICES TO AN END USER.
- PRODUCERS - MEMBERS THAT SUPPLY ELECTRONIC EQUIPMENT.
- GENERAL INTEREST - MEMBERS ARE NEITHER PRODUCERS NOR USERS. THIS CATEGORY INCLUDES, BUT IS NOT LIMITED TO, GOVERNMENT, REGULATORY AGENCIES (STATE AND FEDERAL), RESEARCHERS, OTHER ORGANIZATIONS AND ASSOCIATIONS, AND/OR CONSUMERS.