
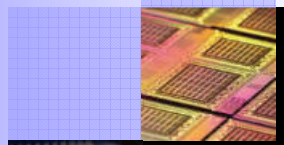

Electrical Modeling and Model Representations for Package Interconnects and Power Delivery Networks

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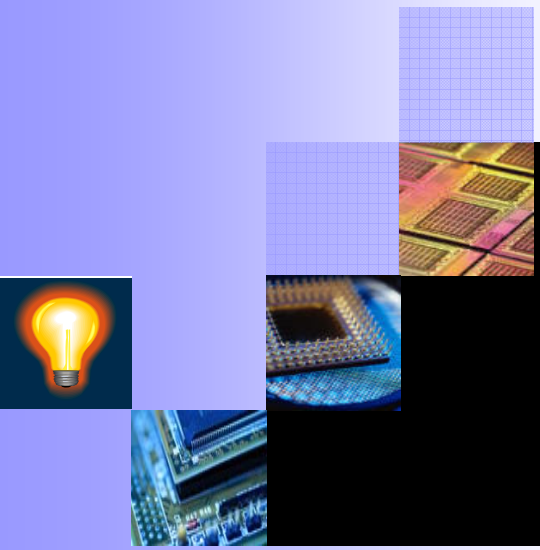
Outline

- Introduction
- SI and PI support by Models
- Package Interconnect Model Hierarchy
- Broadband RLCK Models
- Package Model Representation Requirements
- Present Model Application Issues
- Summary

Introduction

- End-users require ready access to accurate package models with increasingly …
  - complex packages.
    - SiP - arbitrary branching and coupling
  - detailed PI consideration.
  - higher bandwidth.

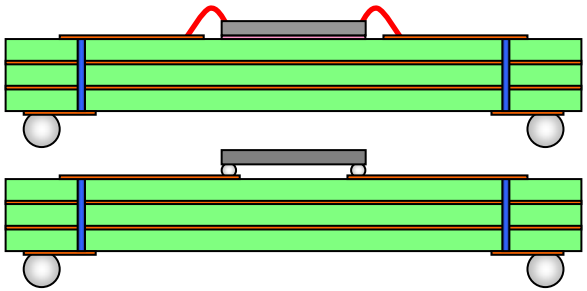
- Present “standard” model formats do not fully support user needs.
  - complexity of model topology must be increased
  - interoperability must be maintained or expanded



Model Requirements for SI and PI of Modern Packages

SI and PI are not separable and PI is not presently well supported by models and model representations.

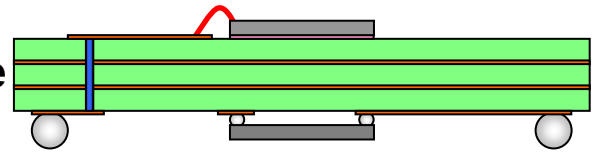
Common package types

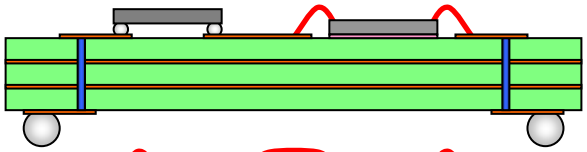


wirebond

flipchip

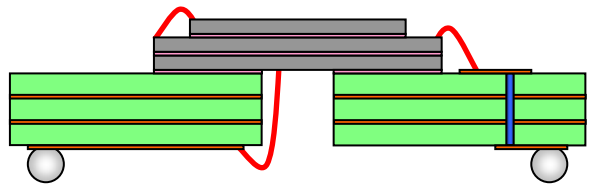
2-sided die

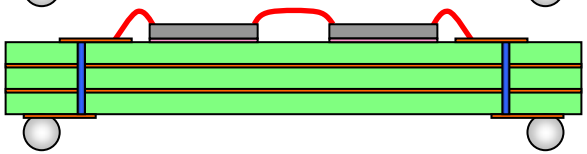




side-by-side die

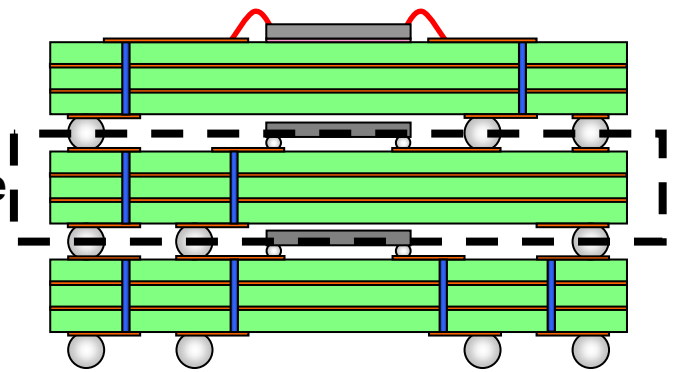
W-BGA

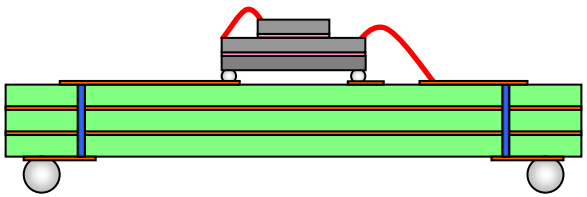




die-to-die bondwires

package-on-package

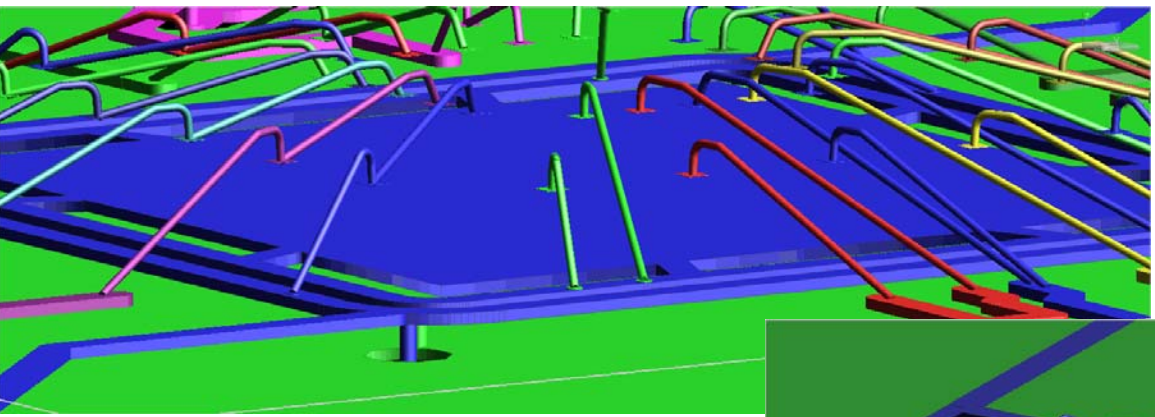




stacked-die

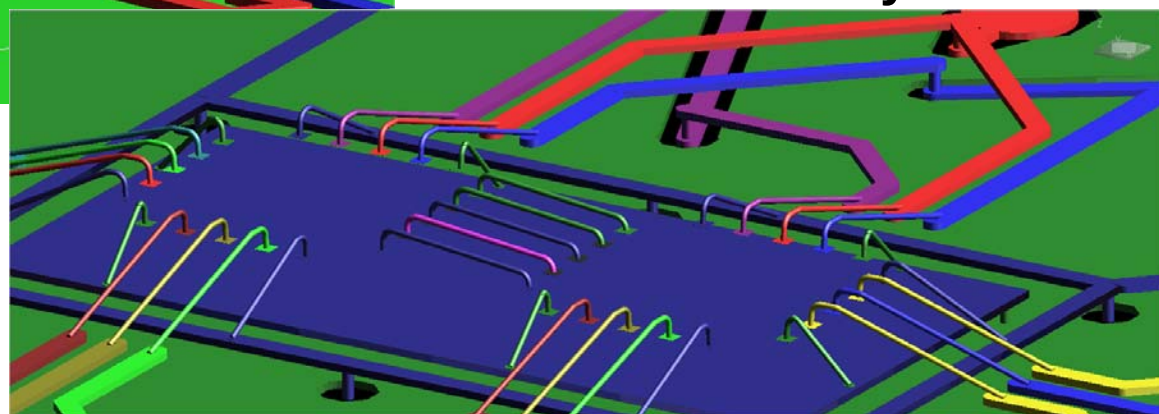
Rapidly increasing package complexity System-in-Package (SiP)

- Increasingly common designs
  - System-in-Package (SiP) applications
- Support required for
  - wirebond, flipchip, combination
  - Net-based and Pin-based models
    - pin grouping for links to chip models



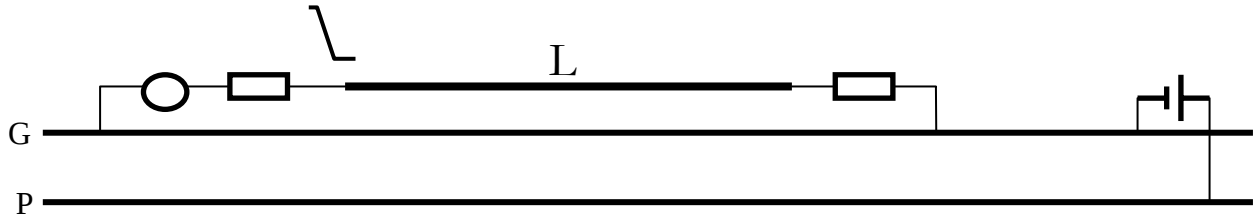
Stacked Die

Side-by-Side Die

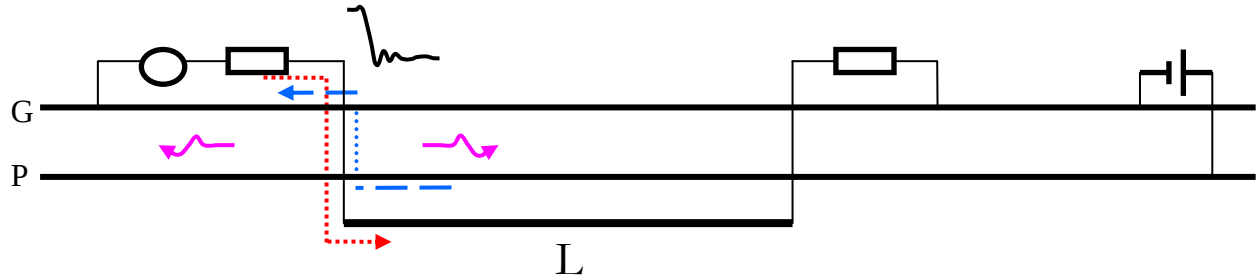


Power integrity *versus* signal integrity ?

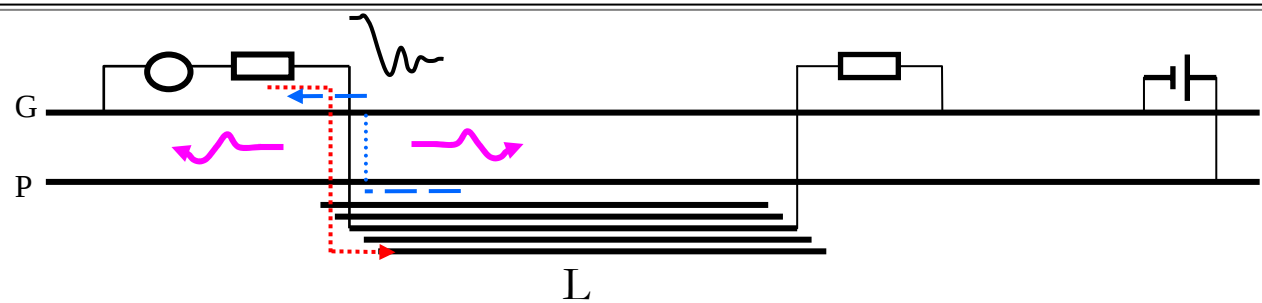
One signal switching without reference plane change



One signal switching with reference plane change

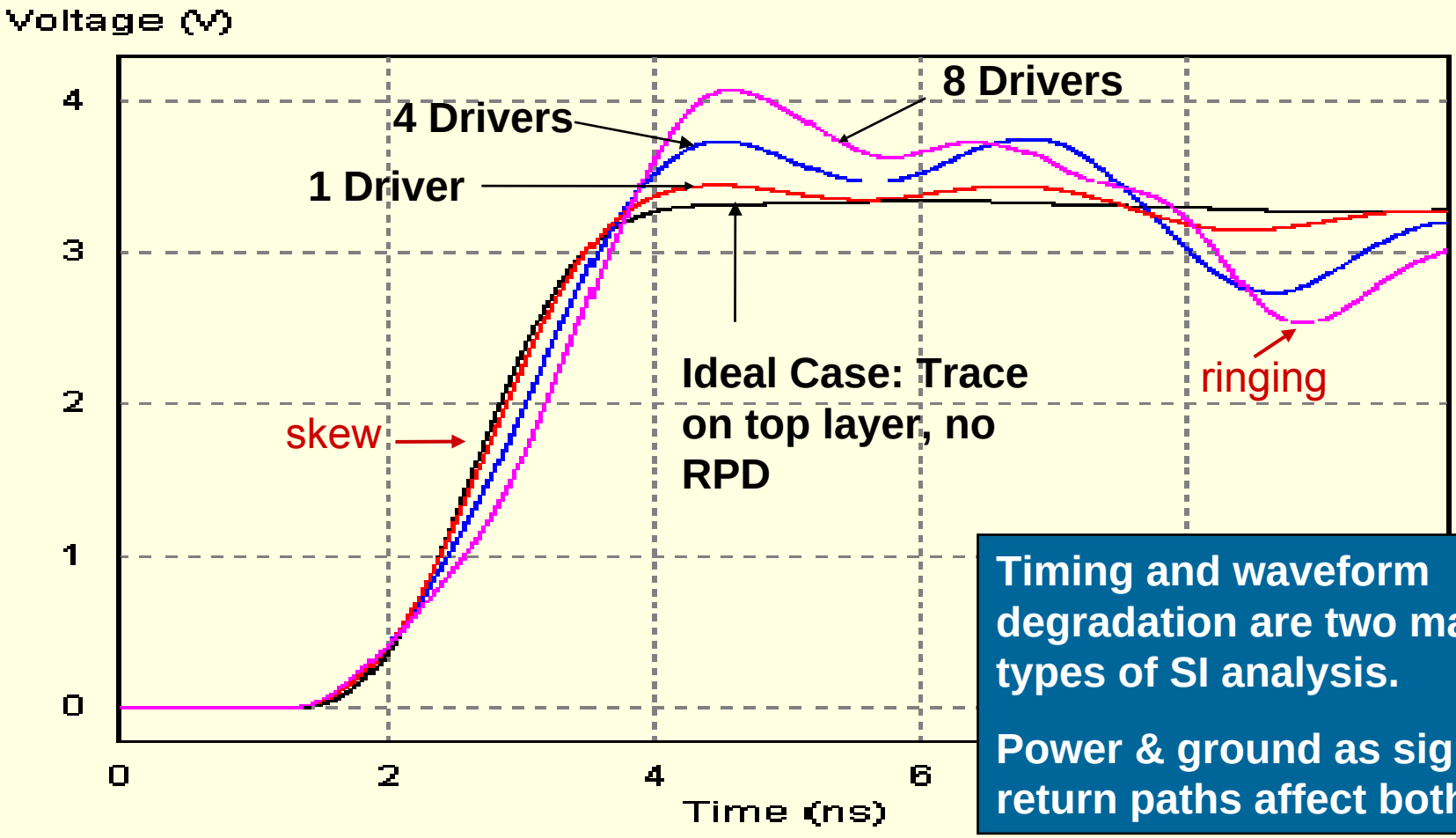


Multiple signals switching with reference plane change



Power integrity *and* signal integrity !

SSN/SSO – Simultaneous Switching Noise/Output

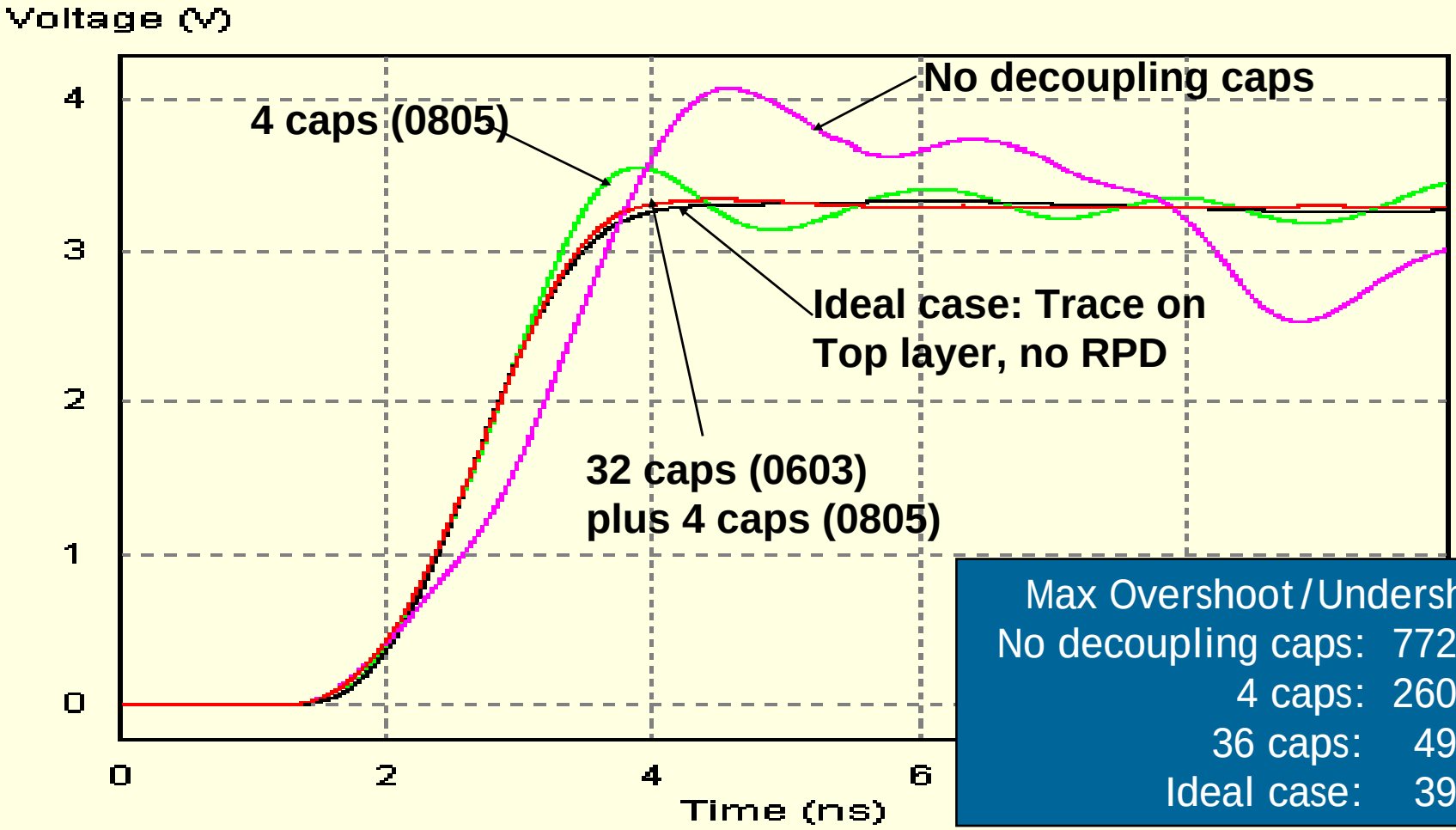


Timing and waveform degradation are two major types of SI analysis.

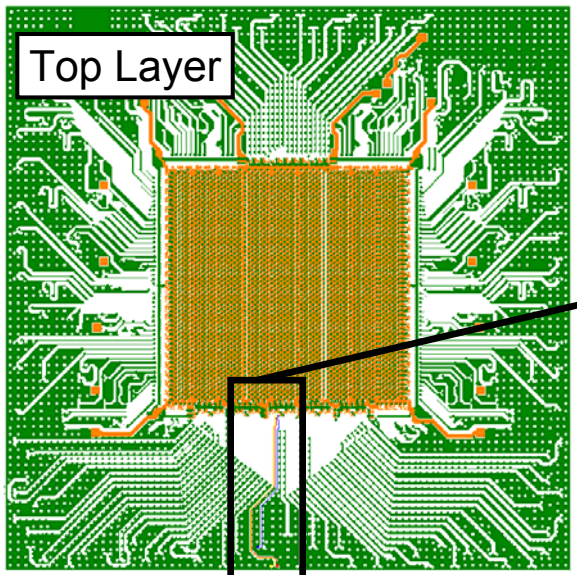
Power & ground as signal return paths affect both.

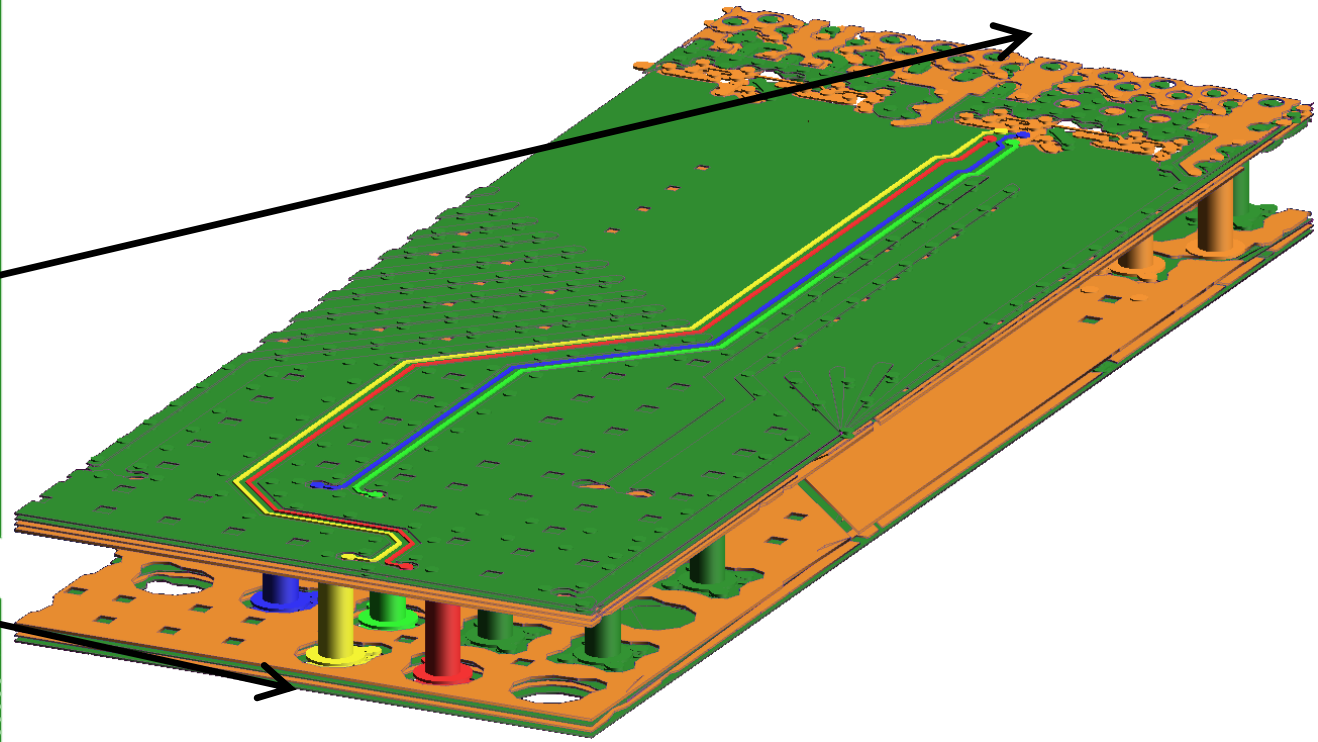
Power integrity *and* signal integrity !

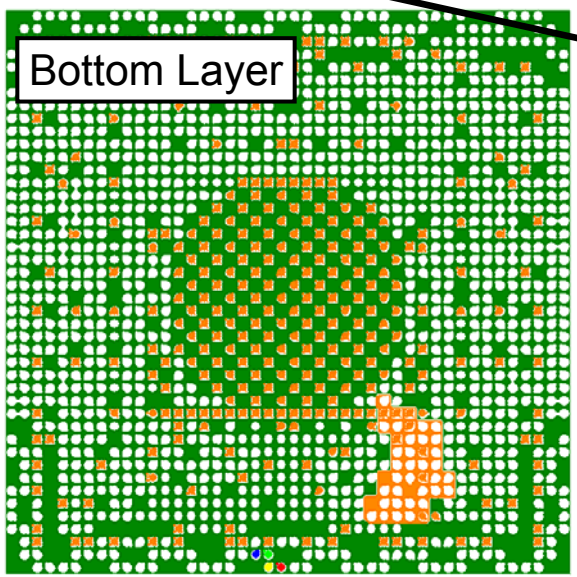
effect of adding decaps

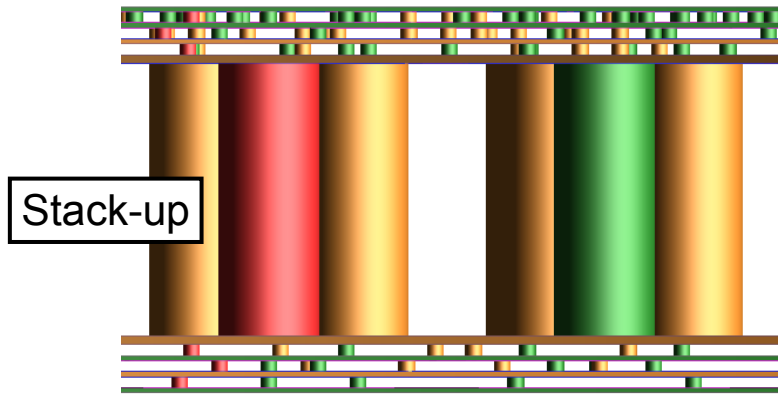


two high speed diff pairs in a package

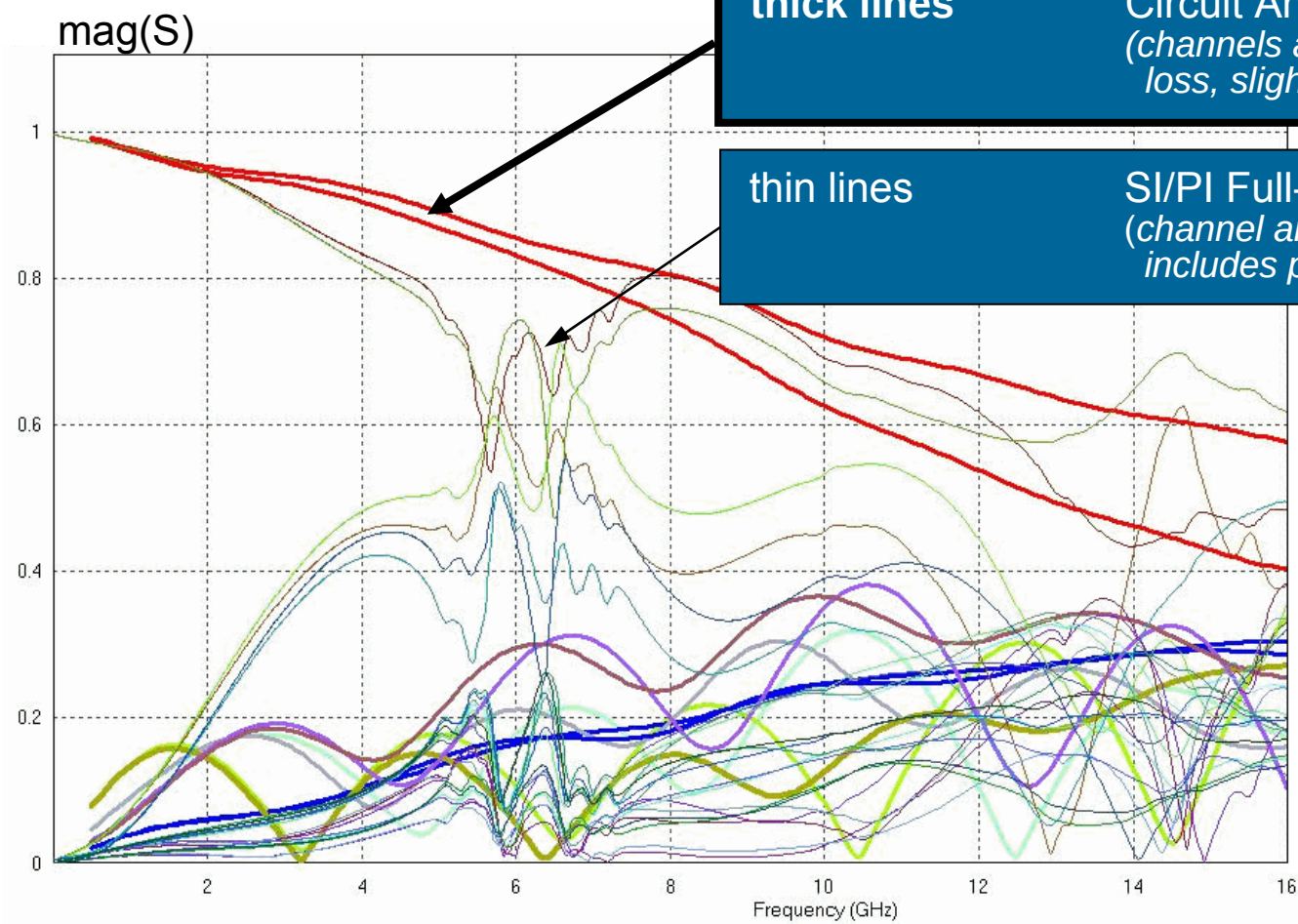








Power integrity *and* signal integrity !



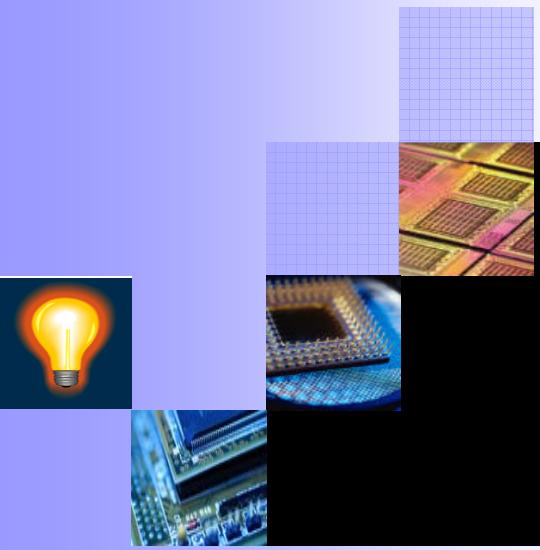
thick lines — Circuit Analysis *and* 3D EM Analysis
(channels and locally-shorted planes, loss, slight impedance mismatch)

thin lines — SI/PI Full-package Analysis
(channel and full planes, includes power plane resonances)

WARNING:

A false sense of security is established if only circuit simulation is applied.

If 3D EM simulation is later applied as a "verification", this sense of security can falsely be reinforced if the full power planes are not included properly in the simulation.



Package Model Hierarchy

Bandwidth and other considerations for different types of package models.

Boards are a generalization with much greater bandwidth requirements and topology complexity.

Model generation techniques

Measurement

+ Accurate
+ High bandwidth
- Post fabrication
- Probing issues
✓ Equipment investment

Numerical Simulation

+ Accurate
+ High bandwidth
+ Pre fabrication
+ Pre fabrication
+ Arbitrary pin count
✓ Software investment

Equivalent Circuit

+ Quick and easy
+ Simple models
+ Low investment
- Low accuracy
- Neglects all PI

Package model hierarchy

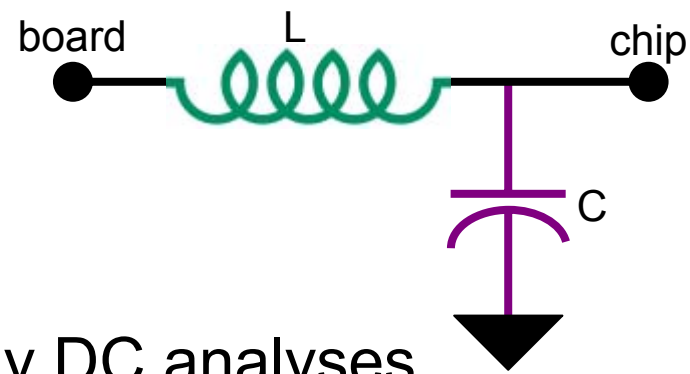
- Measurement *or* numerical simulation based
  1. Ideal (*connectivity topology*)
  2. Lumped, Single-stage, Symmetric
  3. Lumped, Single-stage, Asymmetric
  4. Lumped, Multi-stage, Optimized
  5. Pole-Zero
  6. S-parameters

- Equivalent circuit based
  A. Ideal (*connectivity topology*)
  B. Lumped, Single-stage
  C. Transmission Line
  D. Arbitrary Equivalent Circuits

Package model hierarchy

1. Ideal Connection

- Not strictly valid
- Easy



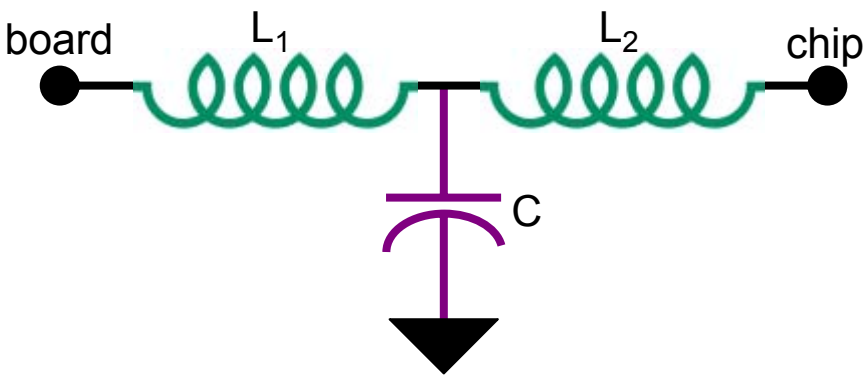
2. DC-based RLGC and IBIS

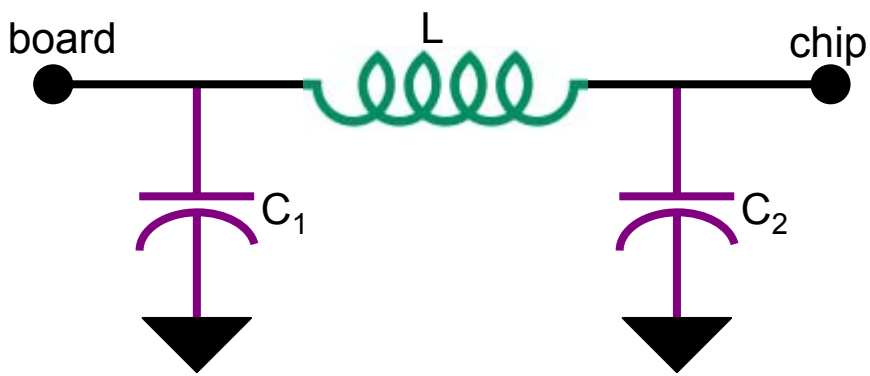
- DC to $\lambda/10$
- Based on separate L & C purely DC analyses
  - One L and R, one C and G – no knowledge how to distribute
- Classical extraction tool RLGC models
  - Can "*guess*" equal split of L or C to apply T or PI equivalent circuit rather than simple low pass filter of single L & C.

Package model hierarchy

3. AC-based optimized RLCK and IBIS

- DC to ≈ $\lambda/5$
- Based on full-wave analysis
- Optimization of component values to fit response
- RLCK IBIS and SPICE models
  - Large pin counts
  - Extended bandwidth

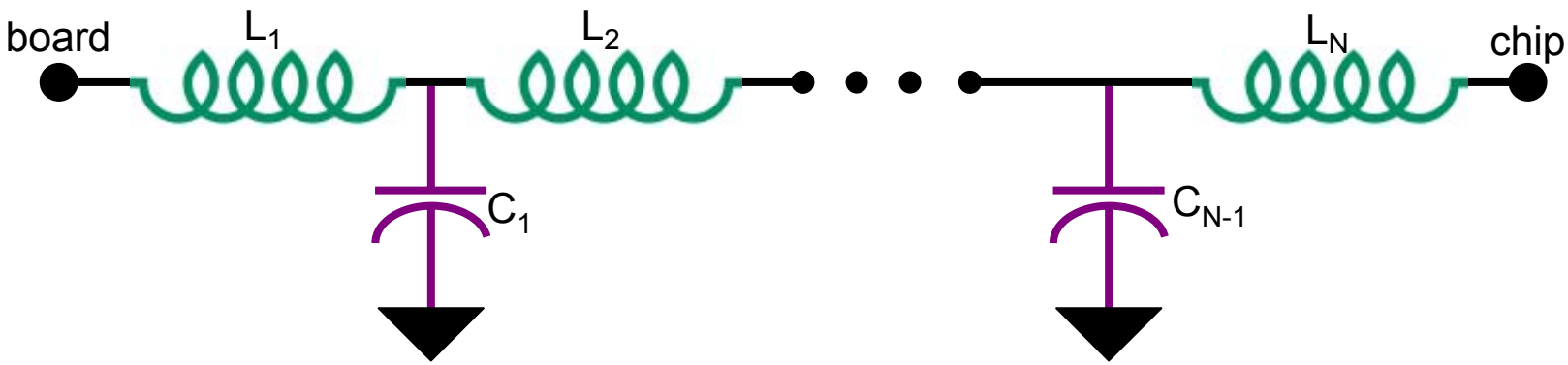




Package model hierarchy

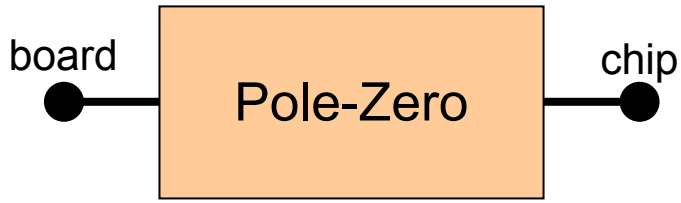
4. AC-based optimized broadband multi-stage RLCK

- DC to ≈ $\lambda/2$ *to* λ
- Based on broadband full-wave analysis
- Optimization of component values to fit response
- Multi-stage broadband RLCK
  - Larger Pin counts
  - Approximates frequency dependent loss
  - Highly efficient simulation time and model storage



Package model hierarchy

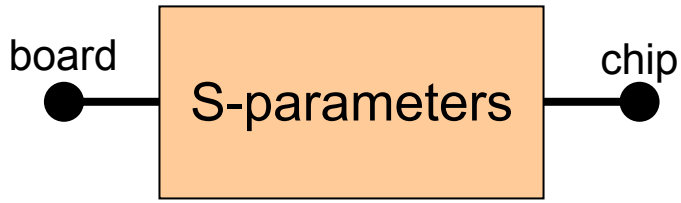
5. Behavioral, Pole-Zero



- Arbitrarily high bandwidth
- Based on full-wave S-parameters
  - Requires broadband S-parameters
  - Typically extracted from ***S*** by “vector fitting” algorithms
- Supports time domain circuit simulation well
  - Use S-parameters directly for frequency domain circuit simulation
- Potential issues
  - Bounded pin count ~ N < 100
  - Passivity and Causality can be difficult to preserve
  - DC difficult to model (long time settling level)

Package model hierarchy

6. S-parameters



- Arbitrarily high bandwidth
- Based on full-wave EM analysis
- Supports frequency domain circuit simulation well
  - Some time domain circuit simulators support for low pin count but usually better to use Pole-Zero models instead
- Benefits
  - High pin count (with very large data files)
  - Passivity and Causality easily preserved in model

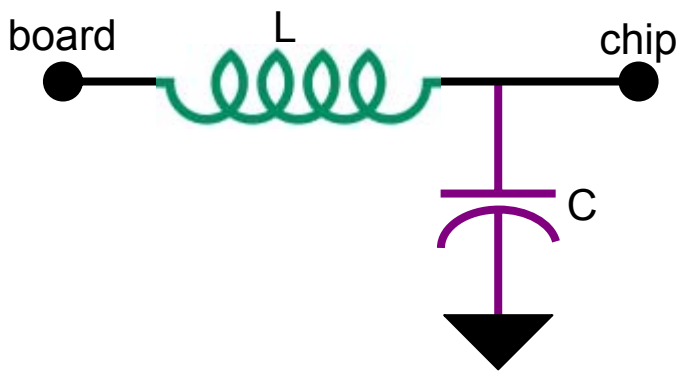
Package model hierarchy

A. Ideal Connection

- Not strictly valid
- Easy

B. DC-based RLCK and IBIS

- DC to $\lambda/10$
- Based on typical values
  - One L and R, one C and G – no knowledge how to distribute



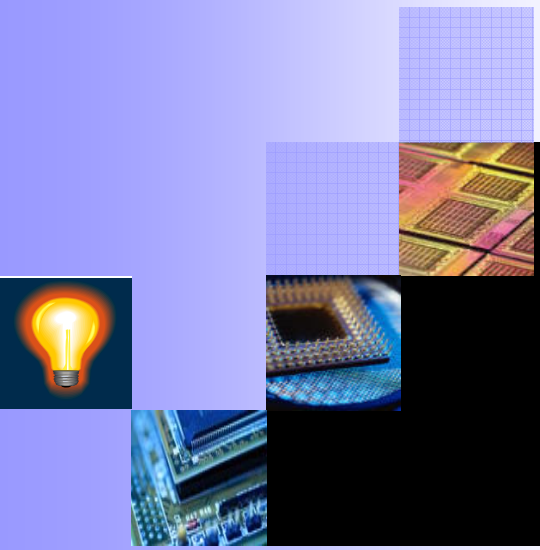
Package model hierarchy

C. Transmission Line

- Commonly called “W-element” model
- Equations or EM TL solvers provide impedance & delay
- Ignores: balls/bumps, vias, pads, return paths, …

D. Arbitrary Equivalent Circuits

- Quick and easy to generate.
  - easy for users to interpret
- Rarely have accuracy corresponding to complexity.
  - complexity provides false sense of confidence
- Ignores: non-ideal return paths, power plane resonances

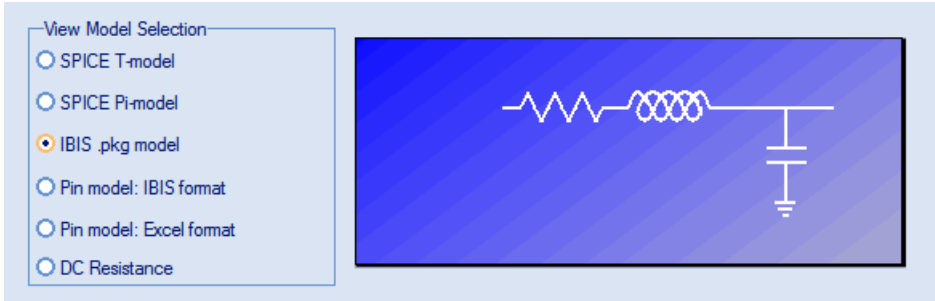


Multi-stage RLCK Models

An increasingly common application to address industry need for greater package model bandwidth.

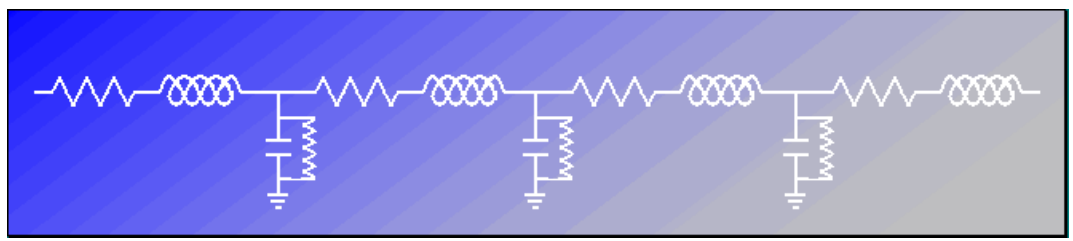
An application lacking robust IBIS model support.

RLCK models



- **single-stage RLCK**
  - IBIS models apply
    - standard coupling issues
      (Re: Sam's previous IBIS presentations.)

- **multi-stage RLCK Models**
  - more broadband
  - no IBIS format available
    - ICM does not support the required arbitrary section-to-section coupling



Why broadband multi-stage RLCK models?

- Significantly greater bandwidth
  - relative to single-stage RLCK models
  - both SI and PI effects to greater bandwidth
- Optimization of component values can yield high accuracy
  - analytically assured full-wave accuracy
    - contrast with unverified guess at distributing DC model data
  - frequency dependent loss for low bandwidth applications
- Model Size efficient
  - versus other broadband models
- Transient circuit simulation time efficient
  - versus pole-zero or S-parameters models

Multi-stage RLCK extraction
where bandwidth is bounded

In the following slide

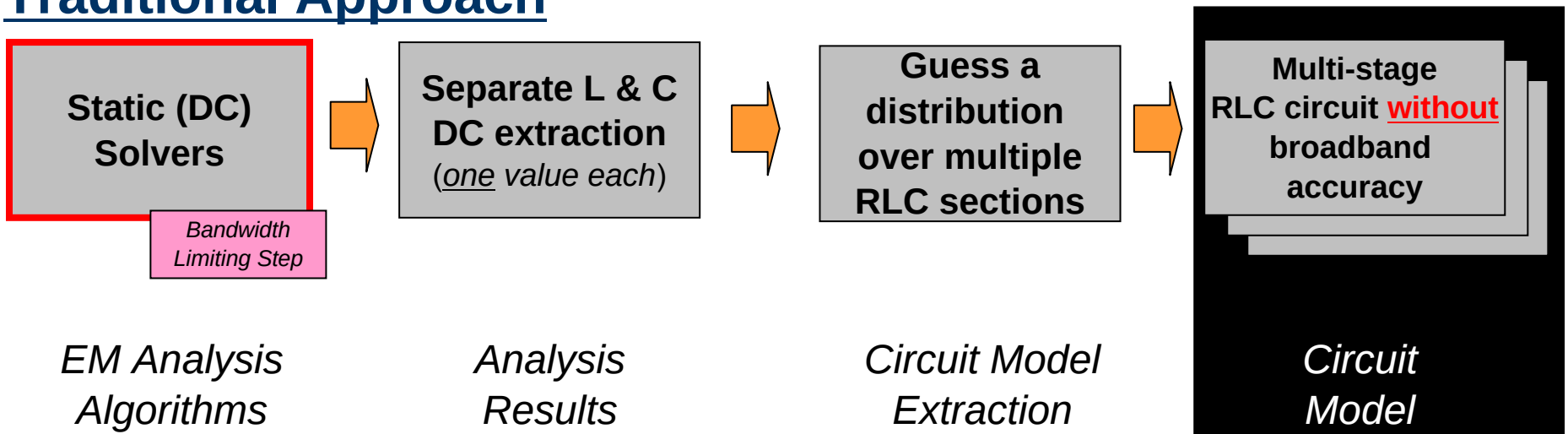
- bandwidth is bounded by the red-boxed step

- Traditional RLC extractors bound accuracy at the first step
  - solve at DC for independent L & C values
  - extract skin loss AC resistance from DC current
  - ***guess*** at distribution to RLC equivalent circuit
  - broadband behavior unverifiable (λ/10 bandwidth)

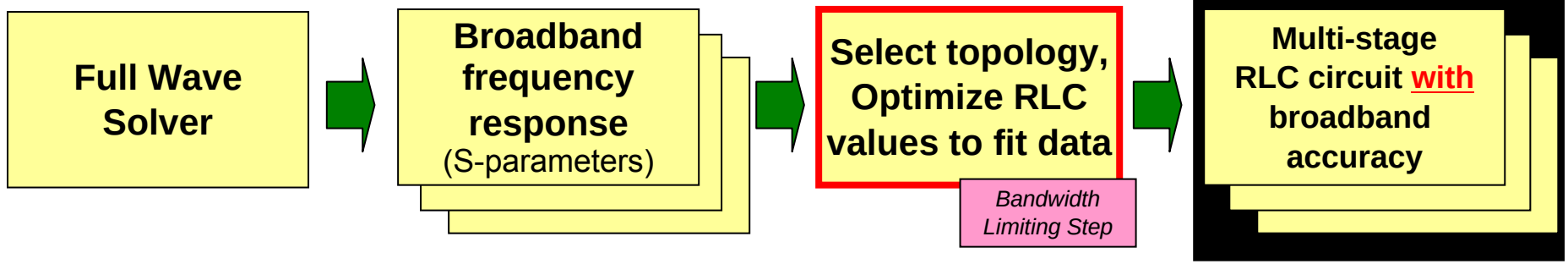
- Full-wave based, multi-stage RLCK broadband models bound accuracy by equivalent circuit topology
  - full-wave analysis of broadband response
  - user-selectable RLCK circuit topology complexity
  - ***optimization*** of RLC circuit components to broadband S-parameters
  - broadband accuracy verified in the GUI (λ/2 – λ bandwidth)
    - potentially higher, complexity tradeoffs kick-in

At what stage is bandwidth bounded?

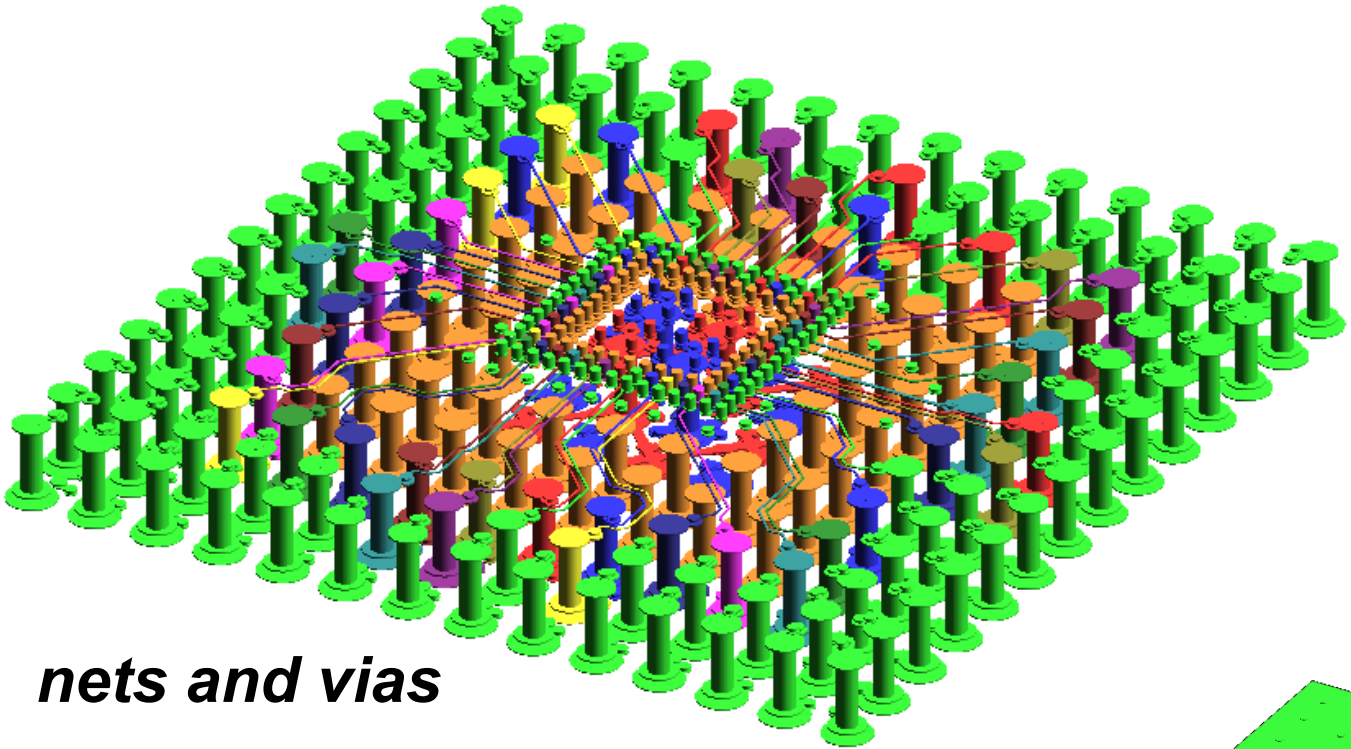
Traditional Approach



Multi-stage RLCK Approach

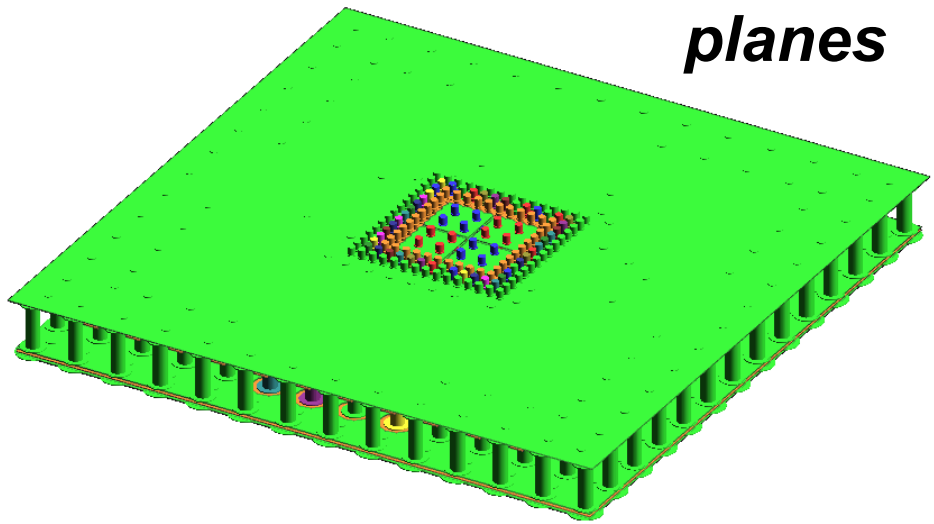


an example package



nets and vias

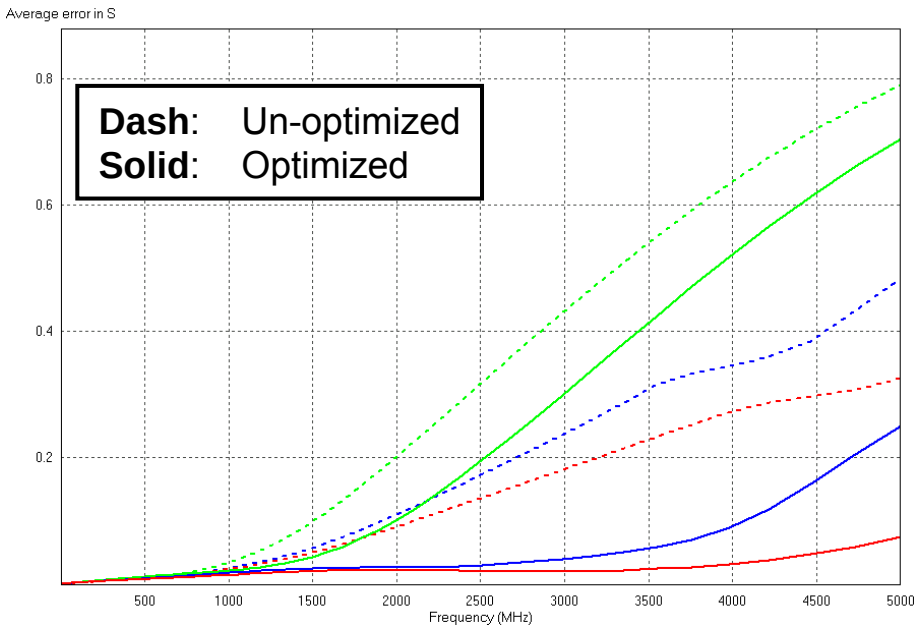
planes

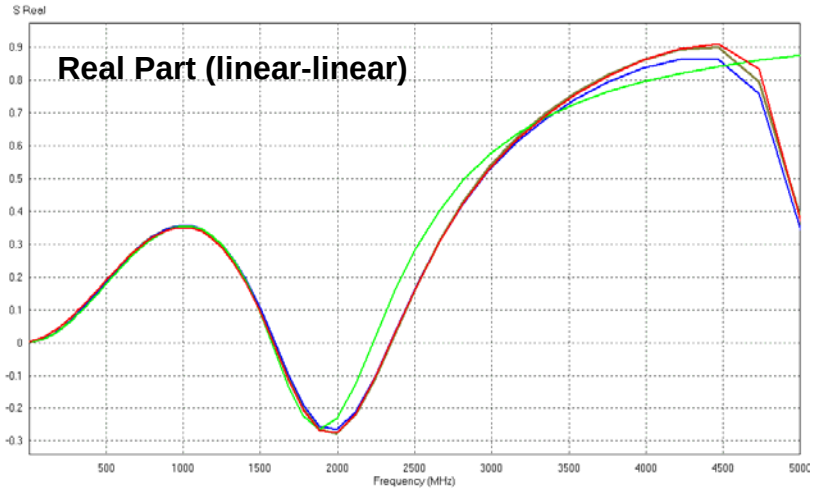


RLCK multi-stage broadband
typical accuracy and bandwidth

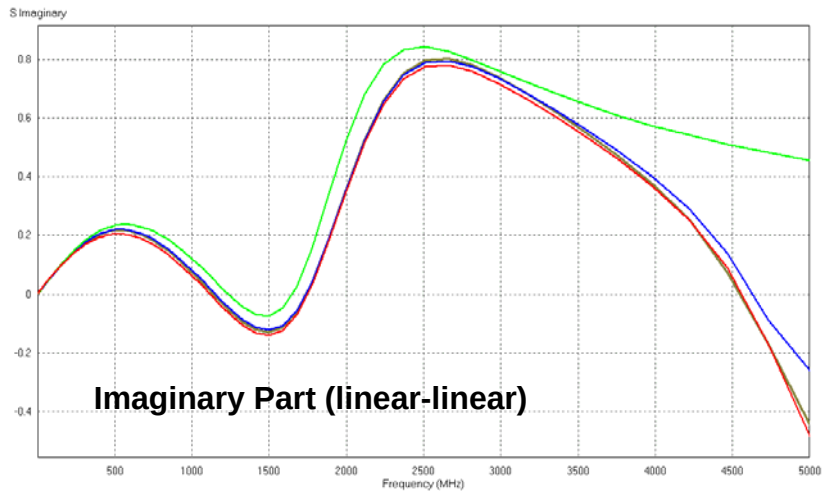
Tan: Original, Green: 1T, Blue: 2T, Red: 3T

Average Error in all S-parameters

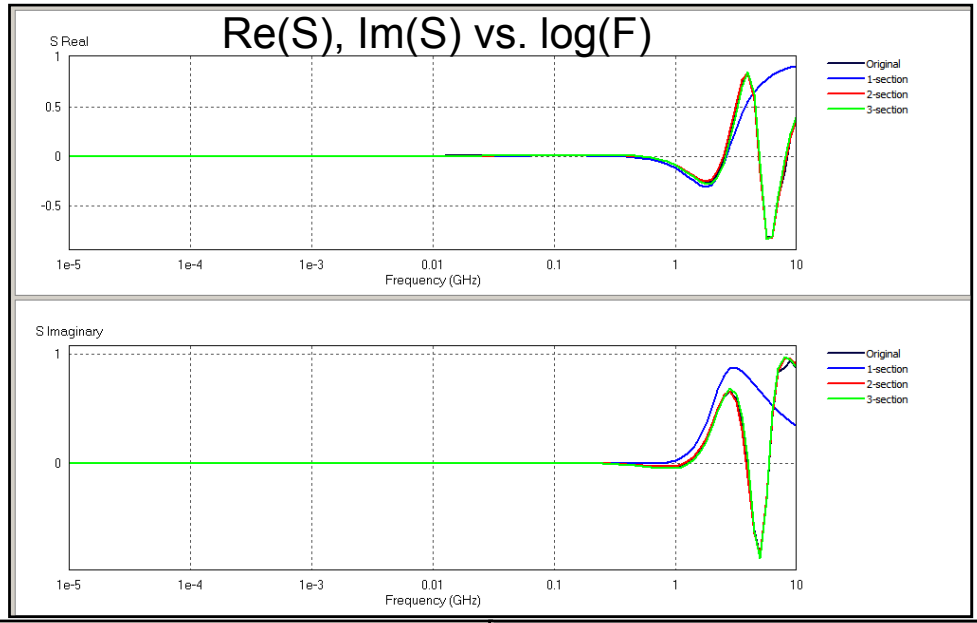


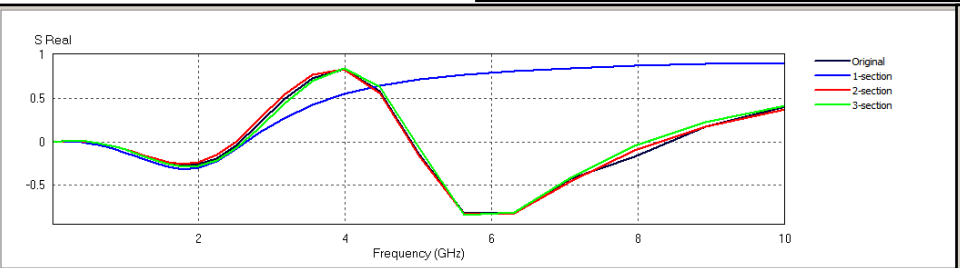


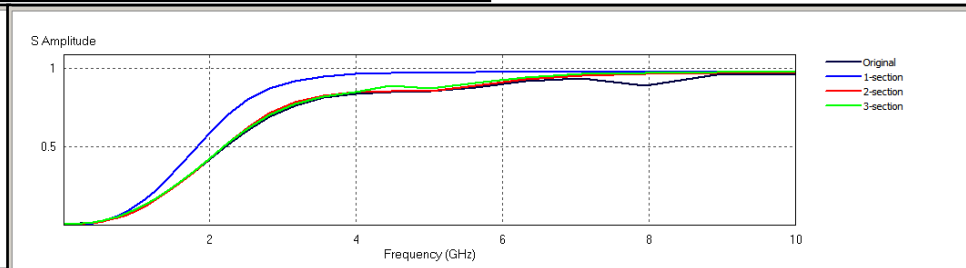
S11 for a Power Net

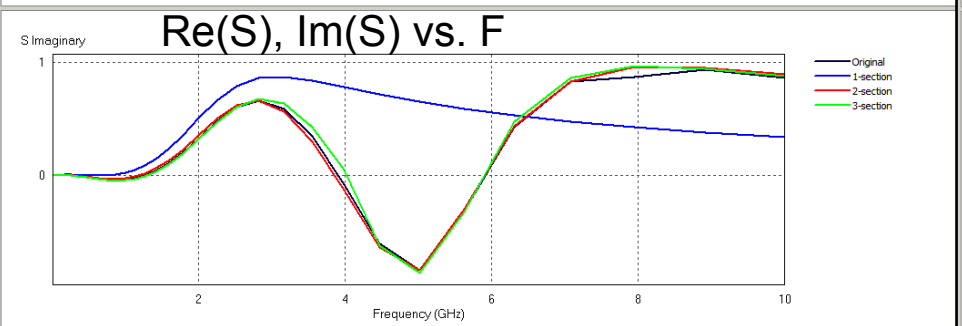


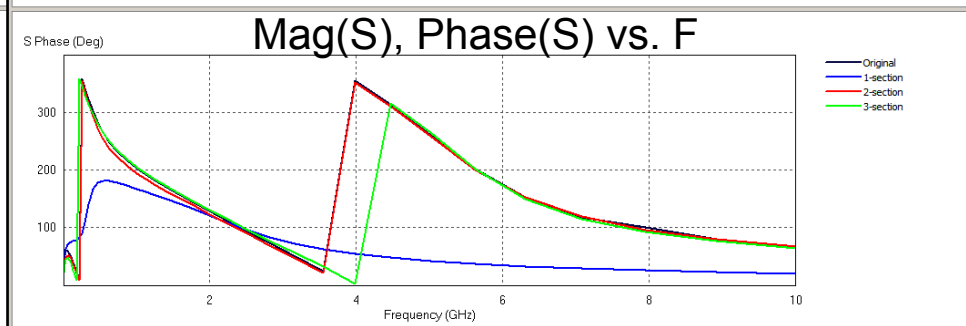
Broadband multi-stage RLCK model behavior





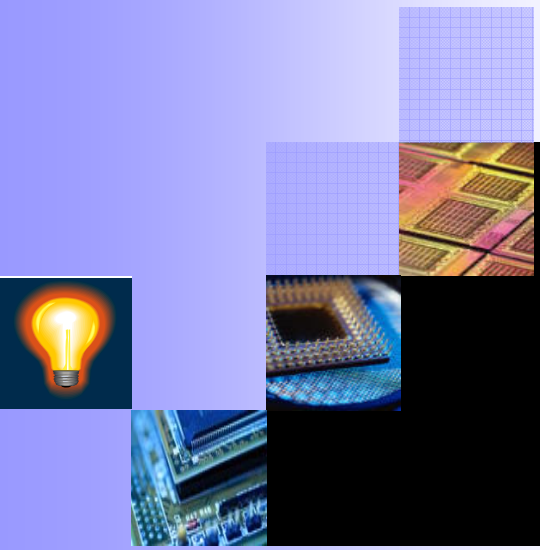






Multi-Stage RLCK broadband model file size

- Pole-Zero Behavioral Model
  - Vector-fitting pole-zero time domain model
  - works very well for this case
  - File size: 11.4Mb
- RLCK broadband file size reduction
  - 1-stage: 101kb (>99%)
  - 2-stage: 167kb (98.5%)
  - 3-stage: 233kb (98%)



Package/Board Model Representation Requirements

More complex topology support is required.

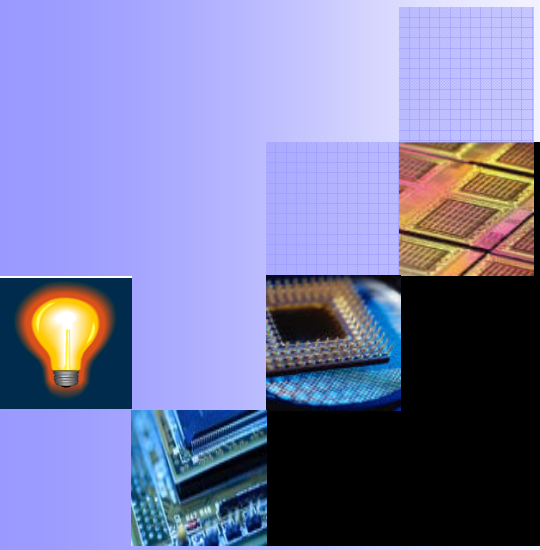
Present Topology Support

- IBIS [Pin] (1)
  - 1:1 pin-pad ratio, no branching, no coupling
  - applies to SI but not PI analysis
- IBIS [Define Package Model] – [Model Data] (1)
  - 1:1 pin-pad ratio, supports single-stage RLCK matrix data, including arbitrary branching and coupling
- ICM
  - multi-section topologies, branching, coupling
  - no inter-section coupling excludes multi-stage RLCK application
  - potential PI issues exist
  - others desire more general equivalent circuit topologies

(1) Sam Chitwood, “Proper IBIS Package Modeling Techniques and Usage in Ideal PDS and SSO Simulations”, IBIS Summit, DesignCon 2008, Santa Clara, CA, USA

How to address user needs for package interconnect ?

- Desire a “standard” model representation that will support for multi-stage RLCK
  - others desire arbitrary circuit (netlist) support with more than RLCK primitives.
  - without it users will continue using SPICE netlists to get required model accuracy and bandwidth for SI and PI analyses.
- A “standard” for netlist models?
  - a stand-alone format?
  - netlists require manual connection
    - tedious, error prone
- Extend ICM?
  - An arbitrary netlist within ICM?
  - How many EDA vendors support ICM?
  - How many device vendors support ICM?

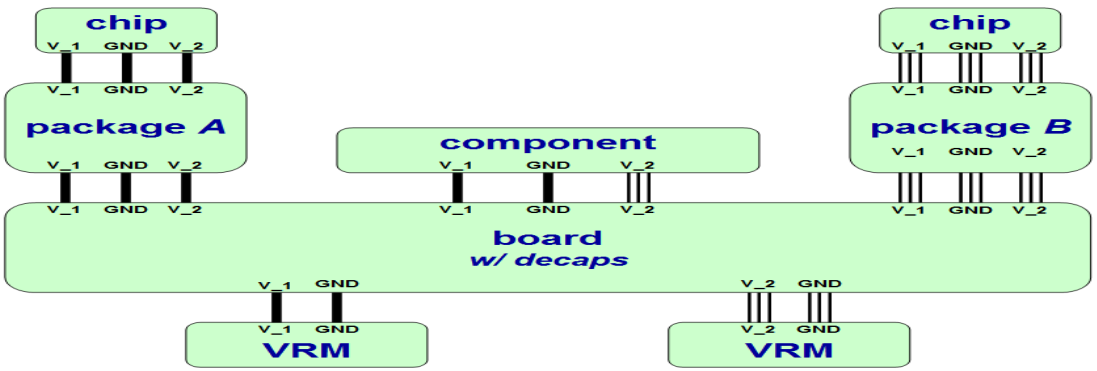


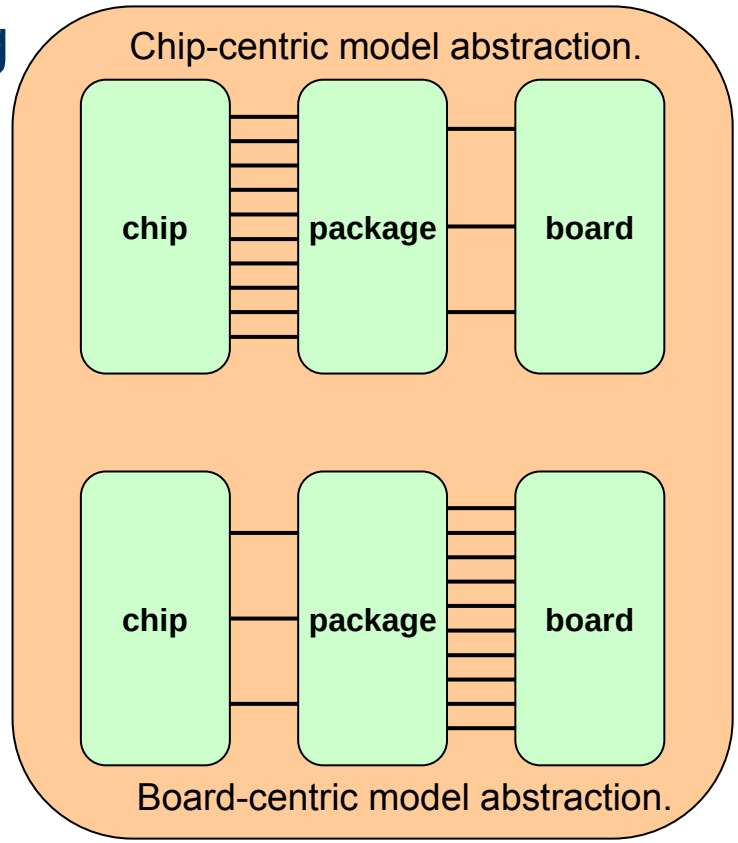
Multi-domain Model Application Requirements

More complex topology support.

Model resolution support

- Models with generalized pin grouping to support *Chip-Package Codesign*
  - Pin-based model at the die,
    net-based model at the board (right/top)
  - Pin-based at the board,
    net-based at the die (right/bottom)
  - Grid-based pin grouping for die or board





Chip-package codesign support

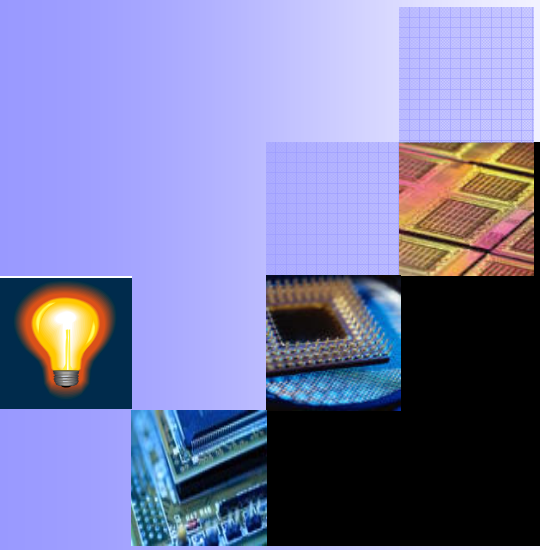
now only vendor-specific approaches

- Apache CPP
  - Supports a link between CPP compliant chip and package extraction tools
  - Header information provides
    - pin names/locations, net names, etc.
- Sigrity MCP
  - An open **m**odel **c**onnection **p**rotocol for application across chip-package-board

```
*
*Sigrity SpeedPKG Suite XtractIM Version 1.2.b0
*
* Start Chip Package Protocol
*
* Start Package Type
*   wirebond dieup
* End Package Type
*
* Start Units
*   Length mm
* End Units
*
* Start Signal Ports
* D1-4     -0.6375    -0.2    = D1-4   Net_0   DIE
* D2-4     -1.3875    -0.5    = D2-4   Net_0   DIE
* D1-3     -0.6375    0    = D1-3   Net_1   DIE
* D2-3     -1.3875    0    = D2-3   Net_1   DIE
* D1-2     -0.6375    0.2    = D1-2   Net_2   DIE
* D2-2     -1.3875    0.5    = D2-2   Net_2   DIE
* D1-7     -0.2    -0.6375    = D1-7   Net_3   DIE
```

How to meet industry needs for model connectivity for multi-domain codesign ?

- ICM partially meets needs with sectioning and port pinmap/nodemap
  - ICM shortfall of arbitrary topologies
    - especially with inter-section coupling
- SPICE-like netlist may have shortfall of manual connectivity
  - potential for standardization of header info?
  - potential for ICM-like wrapper within which arbitrary netlist could be applied?



Summary

Review of key points.

Summary

- End-users require ready access to accurate package models with increasingly …
  - complex packages, detailed PI consideration, higher bandwidth.

- Present “standard” model formats do not support user needs for modern packages.
  - complexity of model topology must be increased
    - require multi-stage RLCK with arbitrary branching and coupling
    - require support for PI issues, not just SI
    - require support for arbitrary equivalent circuits
  - interoperability must be maintained or expanded
    - header protocols for SPICE netlist header protocols are now vendor specific
    - arbitrary netlists require manual connection – tedious and error prone

Thank You!