IBIS-ATM Update: SerDes Modeling and IBIS

Presented by: Todd Westerhoff, SiSoft

DAC IBIS Summit

June 5, 2007

Who Needs SerDes Models?

- System Designers
  - Predict end-end link BER
  - Evaluate system-level design tradeoffs
- ASIC designers
  - Evaluate different TX/RX behavior
- SerDes circuit designers
  - Validate with standard test setups
- Test Equipment Vendors
  - Model device-specific equalization & clock recovery

Serial Link Analysis Needs

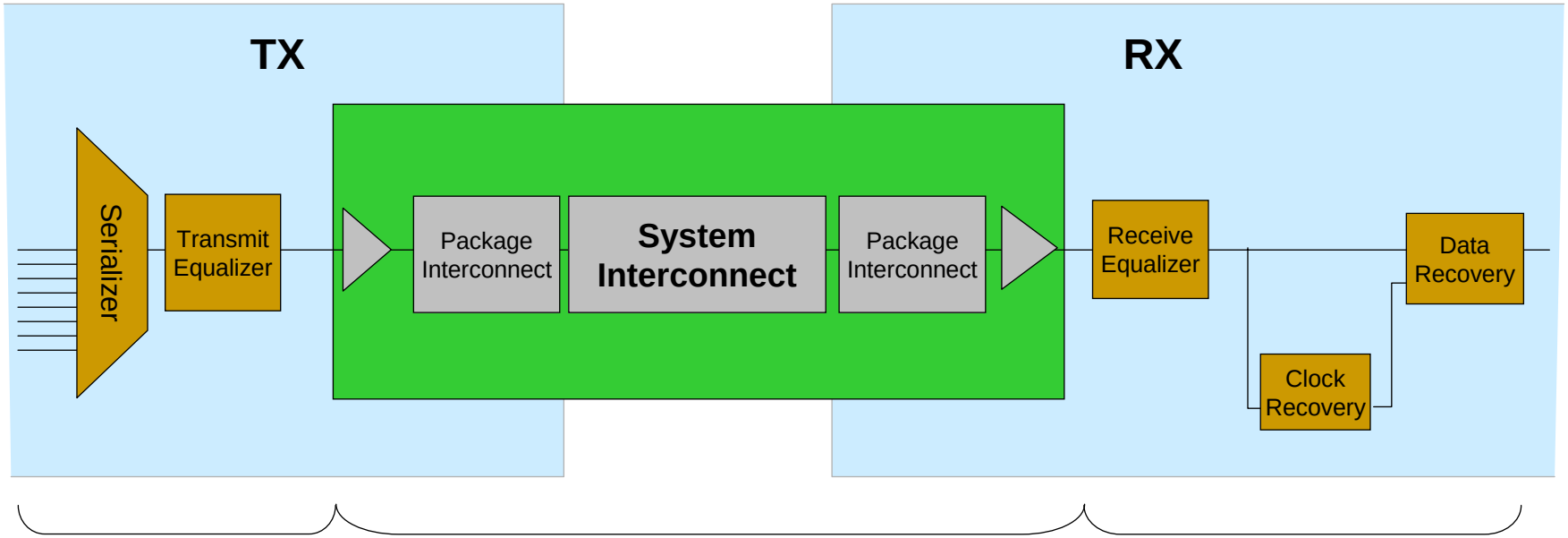
- Analyze link behavior > 10^7 bits
- Model transmit / receive equalization
- Model clock recovery behavior

- Serial link analysis is best addressed through a combination of analytical methods
  1. Characterization of the analog channel
  2. Equalization & clock recovery modeling

Why Use Separate Steps?

- Exploit linear behavior of serial channel analog components for computational efficiency
- Leverage existing techniques for modeling equalization and clock recovery
  - Communication systems theory
- Enable multiple analytical approaches
  - Commercial EDA tools
  - Matlab / StatEye
  - IP vendor tools

Serial Link Analysis



TX EQ
LTI or non-LTI

- TX Equalization
- TX Optimization

Channel & Analog I/O
Linear, Time-Invariant

- Channel Characterization (Impulse response)

RX EQ, CDR
LTI or non-LTI

- RX Equalization
- RX Clock Recovery
- RX Optimization

Serial Link Modeling Assumptions

- Analog channel can be considered LTI
  - Does not apply to fiber optics
- Equalization cannot always be considered LTI
  - e.g. DFE involves quantization of received signal
  - Time-varying (adaptive) behavior
- On-die noise and associated jitter is important, but measurement / modeling is not well defined
  - This will evolve as techniques improve
- IP vendors want to supply models that correspond to silicon as closely as possible

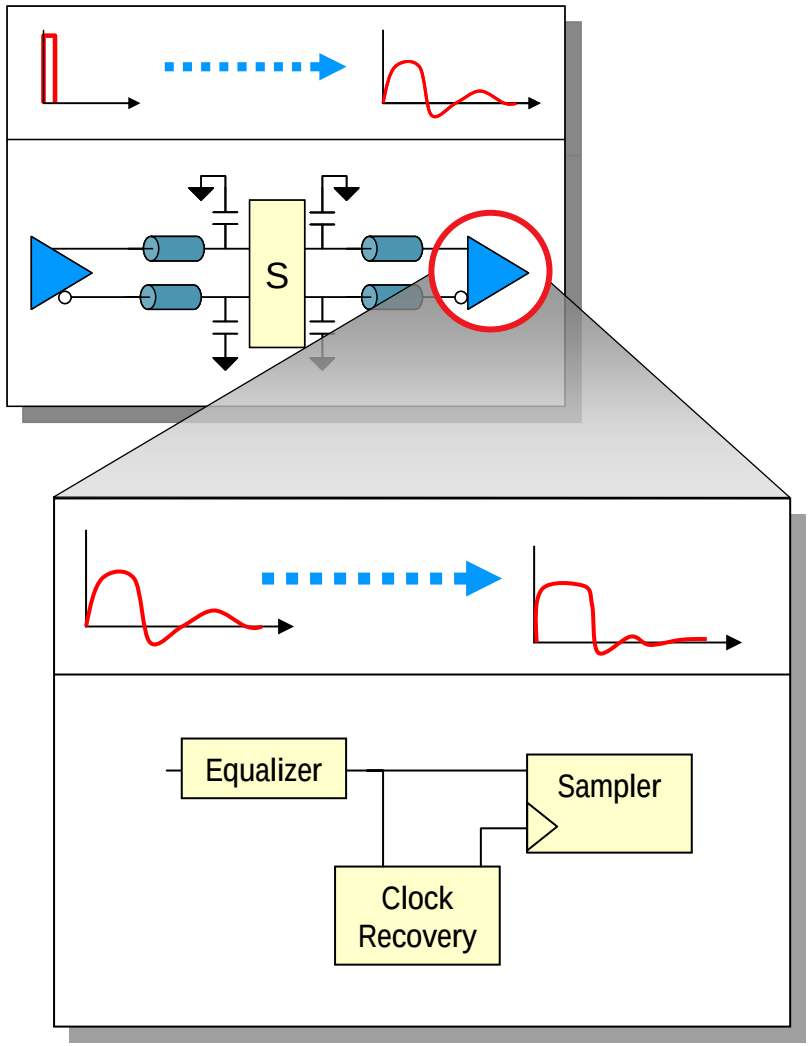
IBIS-ATM Effort

- Goal: SerDes Rx/TX model interoperability
  - Multiple EDA environments
  - Multiple SerDes vendor models
  - Protect SerDes vendor IP
- IBIS-ATM committee participation
  - EDA: SiSoft, Cadence, Mentor, Agilent
  - Semiconductor: IBM, TI, Intel, Micron, Xilinx, ST-Micro
  - System: Cisco
- Two part modeling standard
  - Electrical model: TX / RX analog characteristics
  - Algorithmic model: equalization, clock recovery, device optimization algorithms

IBIS-ATM Activities Since DesignCon

- Weekly IBIS-ATM calls
- EDA vendor meetings
  - Cadence/SiSoft/Mentor meeting in Chelmsford, MA
  - Weekly conference calls
- Regular meetings with IP vendors
  - Weekly conference calls
- Developed & refined draft BIRD

Required SerDes Device Models



- Characterization (analog)
  - Existing IBIS 4.2 syntax

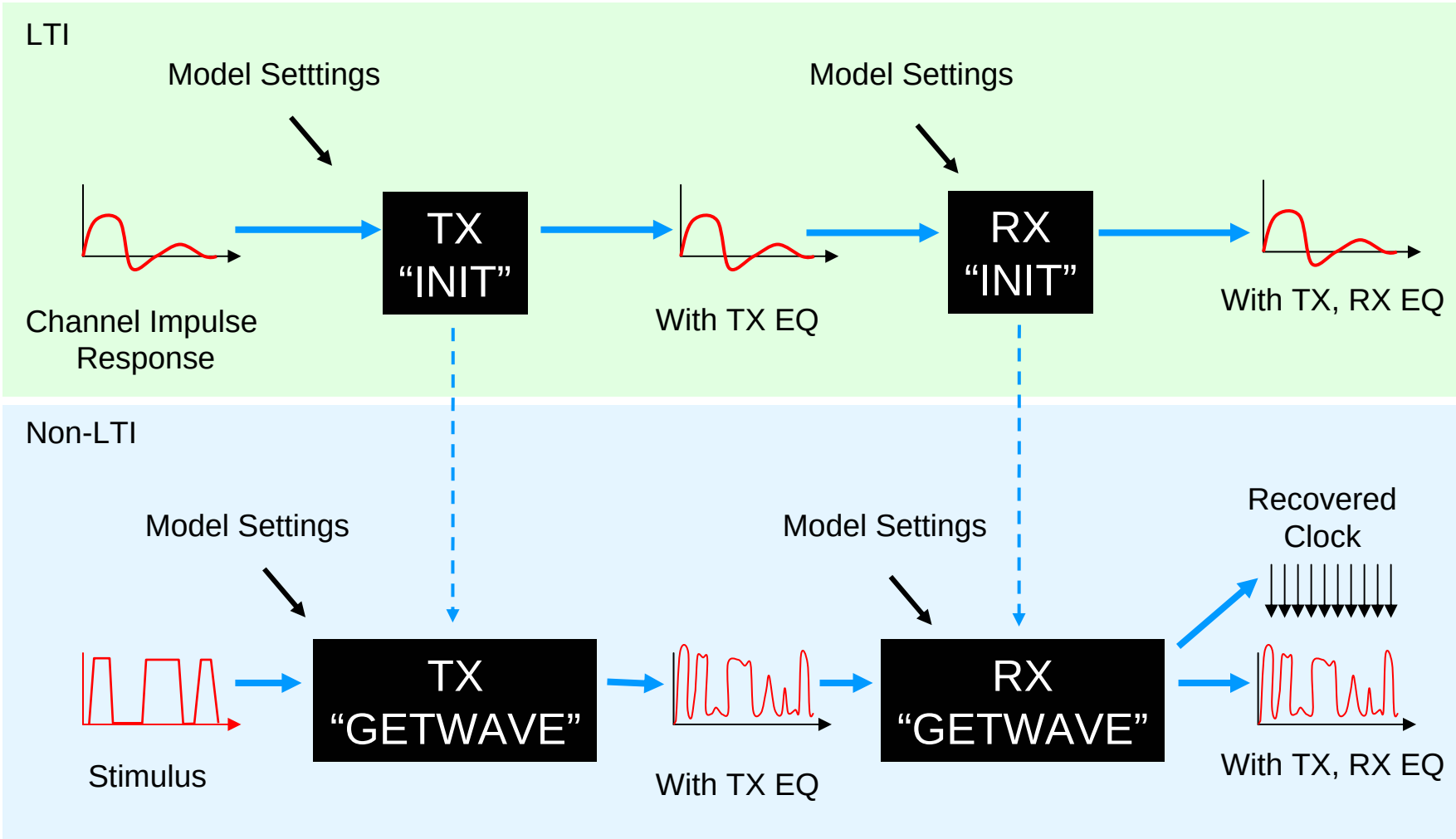
Communications models

- LTI
  - Equalization
  - RX clock PDF
- Non-LTI
  - Nonlinear equalization
  - Adaptive equalization
  - Clock recovery behavior

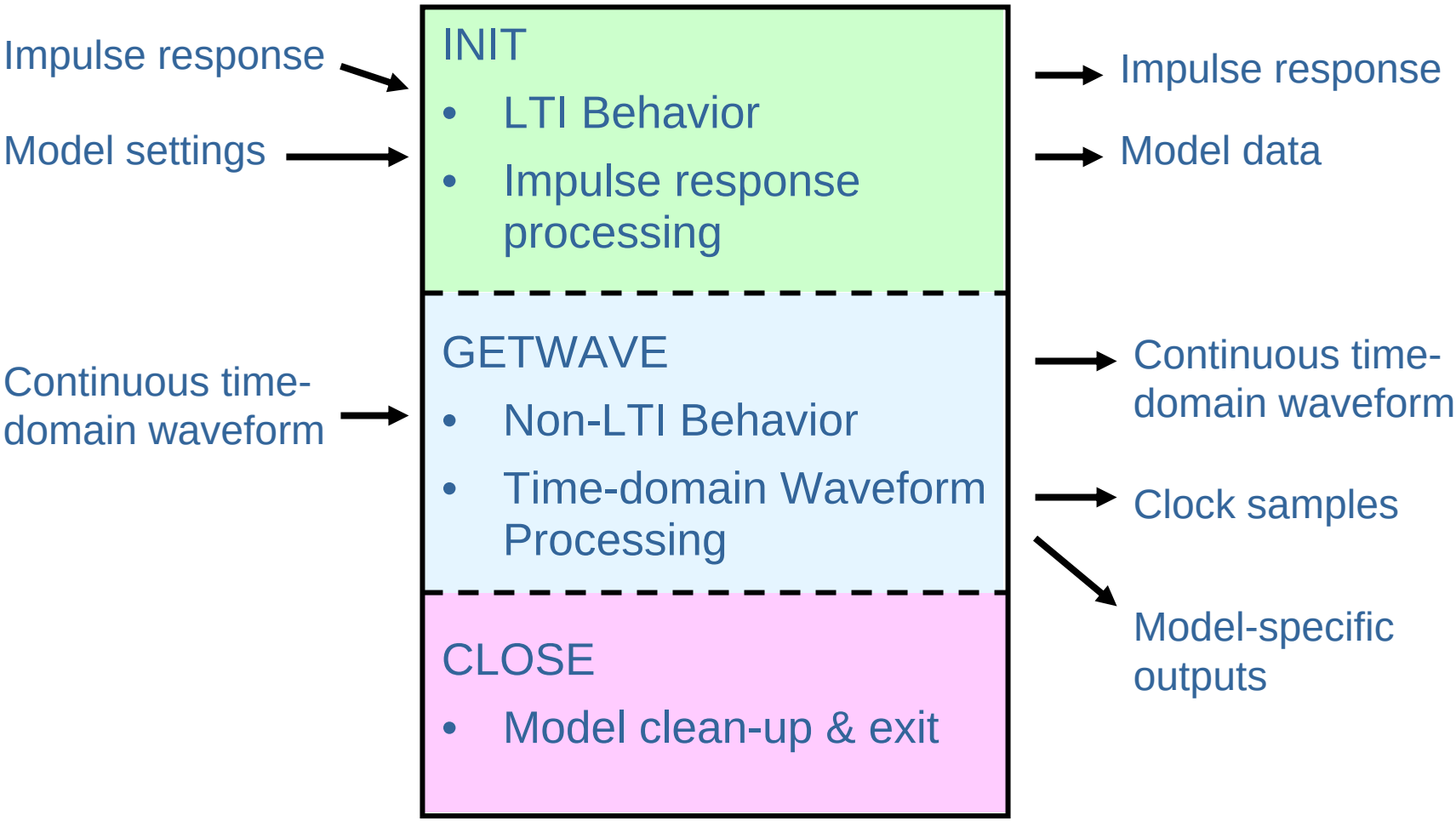
IBIS-ATM Algorithmic Models

- Models provided as executable [binary] code
  - Fast, efficient execution
  - Protects vendor IP
  - Extensible modeling capability
  - Allows models to be developed in multiple languages
- Standardized execution interface
  - Module loading mechanism & call signature
  - Data input/output formats
- Standardized model parameter interface
  - “Reserved parameters” interpreted by EDA platforms
  - Model-specific parameters can be exposed to and set by end-users

IBIS-ATM Algorithmic Models



Executable Model Architecture



Executable (DLL) Call Arguments

- Init (impulse response processing)
  - Bit time
  - Number of waveform samples per bit
  - Number of crosstalk aggressors
  - Channel impulse response(s)
  - Model parameters and values
  - Pointers to free memory, data return area
- Getwave (waveform processing)
  - Input waveform(s)
  - Pointers to data return area
    - Equalized waveform
    - Clock times
    - Optimized parameters

Model Parameters

- Additional data passed between executable model & simulator
- Model-specific parameters
  - Allow IP vendors to define data required for / provided by a specific model
  - Defined parameter declaration and usage format
    - Allows end-users to set and display model-specific data
- Reserved parameters
  - Predefined parameter list used by EDA tools to alter analysis flow
  - Allows models to tell EDA platform what data the model does/doesn't provide

Current IBIS-ATM Status

- Original proposal submitted by Cadence in 2006
- Current proposal authored by Cadence, SiSoft, Mentor
- Technical issues settled between EDA vendors
- Proposed solution reviewed with IP vendors
- Detailed documentation in development
- Plan to distribute sample models and “wrapper code” to aid model developers

Next Steps

1. Preliminary approval by IBIS-ATM subcommittee
2. Complete BIRD documentation
   - Target: June 2007
3. Develop sample models & prototype EDA integration; resolve detailed issues with spec
   - Target: September 2007
4. Bring to IBIS-ATM committee for final approval
5. Bring to IBIS committee for approval

* Note: Steps 3 and 4 in parallel