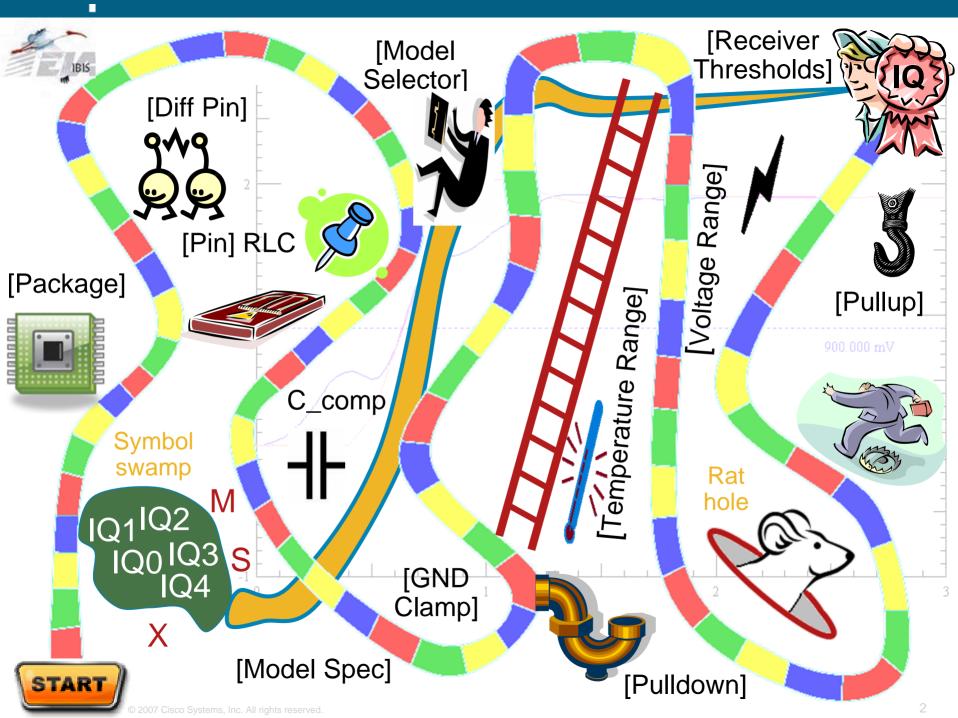


### **IBIS** Quality Report



A progress report of the IBIS Quality Task Group Mike LaBonte, Cisco Systems IBIS Summit Meeting, 5 June 2007



# Regular IQ Meeting Participants

- David Banas, Xilinx
- Moshiul Haque, Micron Technology
- Kim Helliwell, LSI Logic
- Mike LaBonte, Cisco Systems, chair
- Eckhard Lenski, Siemens
- Roy Leventhal, Leventhal Design & Communications
- Bob Ross, Teraspeed Consulting Group

## **Brief History**

- Barry Katz started IBIS-Quality in March 2002
- Review of 1.0 IQ specification completed October 2004
- IQ checklist released October 2004
- Parser bug 90 submitted and approved August 2005
- Parser bug 94 submitted and approved March 2006
- Book "IBIS Model Creation & Validation" discusses IQ
- Version 1.1 IQ specification initiated August 2006

## **Specification Version 1.1**

#### IBIS Quality Levels

IQ0 - Not Checked

IQ1 – Passes IBISCHK

IQ2 – Suitable for Waveform Simulation

IQ3 – Suitable for Timing Analysis

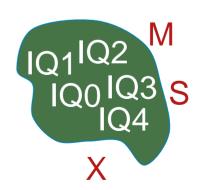
IQ4 – Suitable for Power Analysis

#### Special Designators

S – Simulation correlated

M – Measurement correlated

X - Exceptions



# **IQ Check Example**

# 3.2.5 {LEVEL 3} [Pin] RLC parasitics are present and reasonable

For a LEVEL 2 model, pin parasitics are optional, but they are mandatory for a LEVEL 3 model (that is, a model suitable for timing). To pass this check the RLC values must be present for all signal pins in the [Pin] section, or [Package Model] must be present. Pin parasitics should either be measured or extracted using a 2D or 3D solver. Reasonable signal pin parasitics will result in impedance and delay characteristics that fall in the ranges:

TD = SQRT(LC) < 300ps

Z0 = SQRT(L/C) < 100ohm

Note that IQ check 3.1.2. also requires that each [Pin] RLC value falls within the min/max range as given by the [Package] keyword. The [Package] keyword can be adjusted to accommodate.

#### **Current Activities**

- Working on feature-selective validation for correlation
- Reviewing IQ checks
  - Updating to new level numbering system
  - -Rationale documented to avoid future confusion

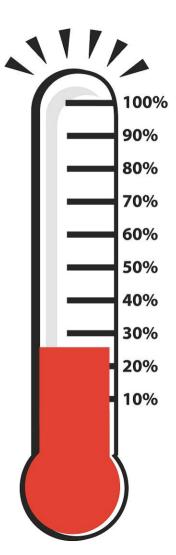






# **Summary of 1.1 Review Progress**

- 2.0 General Header Section
  8 of 8 checks reviewed
- 3.0 Component Section
  17 of 19 checks reviewed
- 4.0 Model Section0 of 68 checks reviewed
- 5.0 Possible Errors
  Needs rework, maybe a name change
- 6.0 Correlation
  David and Roy working on this
- 7.0 Model Limitations and Model Maker Notes ???



## **IBIS** Quality Task Group

Web:

http://www.vhdl.org/pub/ibis/quality\_wip

Email list:

http://www.freelists.org/list/ibis-quality

–Or send email

To: ibis-quality-request@freelists.org

Subject: subscribe

- Meetings:
  - -Tuesdays from 11:00am to 12:00pm Eastern Time
- Questions? Mike LaBonte milabont@cisco.com