IBIS-to-Spice Correlation
a story of 5 metrics

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Introduction

A Brief History of IBIS Accuracy

(blatantly plagiarized from the *I/O Buffer Accuracy Handbook*)

- 1997 – The *IBIS Accuracy Subcommittee* (IAS) convenes for the first time; their mission: to specify what it means for an IBIS model to be “accurate”. (Happy 10-yr. reunion, by the way!)
- 1998 – IAS release their initial version of the *IBIS Accuracy Specification*, which later becomes the *I/O Buffer Accuracy Handbook*. In this document, IAS define the *Curve Overlay Metric*, an attempt at standardizing the quantification of model accuracy by specifying the method of correlation of the IBIS model’s predictions to bench measurements of the silicon itself…

- 2007 – 10 years has passed since the IAS first met with the intent of defining IBIS model accuracy. Recently, unrest has surfaced more and more frequently in the IBIS galaxy. Customers of semiconductor vendors have been heard to complain, “Your IBIS models suck! They’re not accurate enough to use in our system level timing closure analysis. Fix them or we’re sending our most vicious procurement agent, Darcy Trader, over there. She’ll chew up your sales guys and spit ‘em out like raisins!
- Something had to be done…

Model Correlation Committee

- And so it was decided, at an IBIS Quality Task Group (IQTG) teleconference (which, thanks to the miracle of modern telecommunications, wasn't really all that far away) that the *Model Correlation Committee* (MCC) would be formed.
- Two Knights of Accuracy (KofA), one a fairly well known and respected figure in the semiconductor modeling world, and the other a pompous upstart looking to ride the coattails of the former in the hopes of quickly gaining some cheap and unearned notoriety, were chosen to co-chair this committee.

MCC (cont’d.)

- Together these two KofA would defend the galaxy from inaccurate IBIS models correlating with neither the Spice models from whence they came nor the silicon they were intended to represent (after they finished their lunch at KFC, that is).
- As a prelude to their work, they would first have to undergo an exhaustive training in the *Way of the 5 Metrics*…
  (Alright, alright, it’s only 2 hours per week. That’s all my boss will allow; sheesh!)
- (Aside: This being the real World where peer buy-in matters and Hollywood-style egocentric solo efforts don’t accomplish all that much, we’re really hoping to get your feedback on all of this. Thanks!)

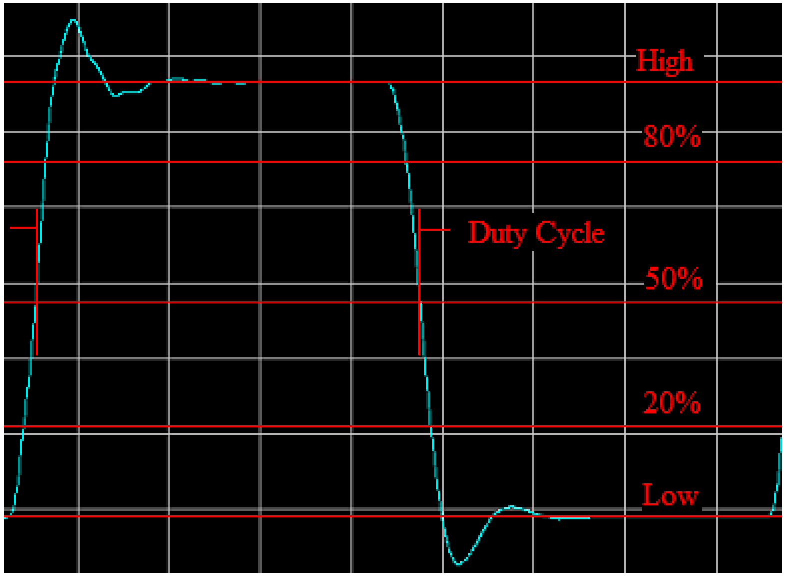
Chapter IV – *A New Approach*

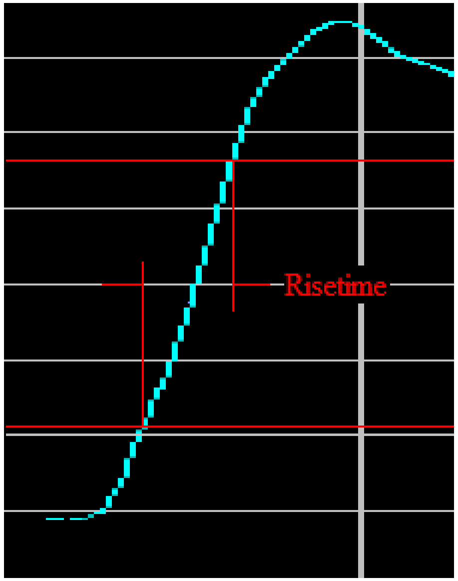
Why a New Approach?

- The *Curve Overlay Metric* is an excellent first step towards quantifying the correlation between IBIS and Spice models (or between IBIS models and bench measurements).
- However, narrowing the focus of the correlation to several specific features or *metrics* of the waveforms can provide additional insight into the possible sources of any observed discrepancies.
- (The *I/O Buffer Accuracy Handbook* actually suggests this.)

5 Metrics Defined

- We propose the following 5 metrics/features for waveform comparison:
  - high level, low level, rise time, fall time, and duty cycle

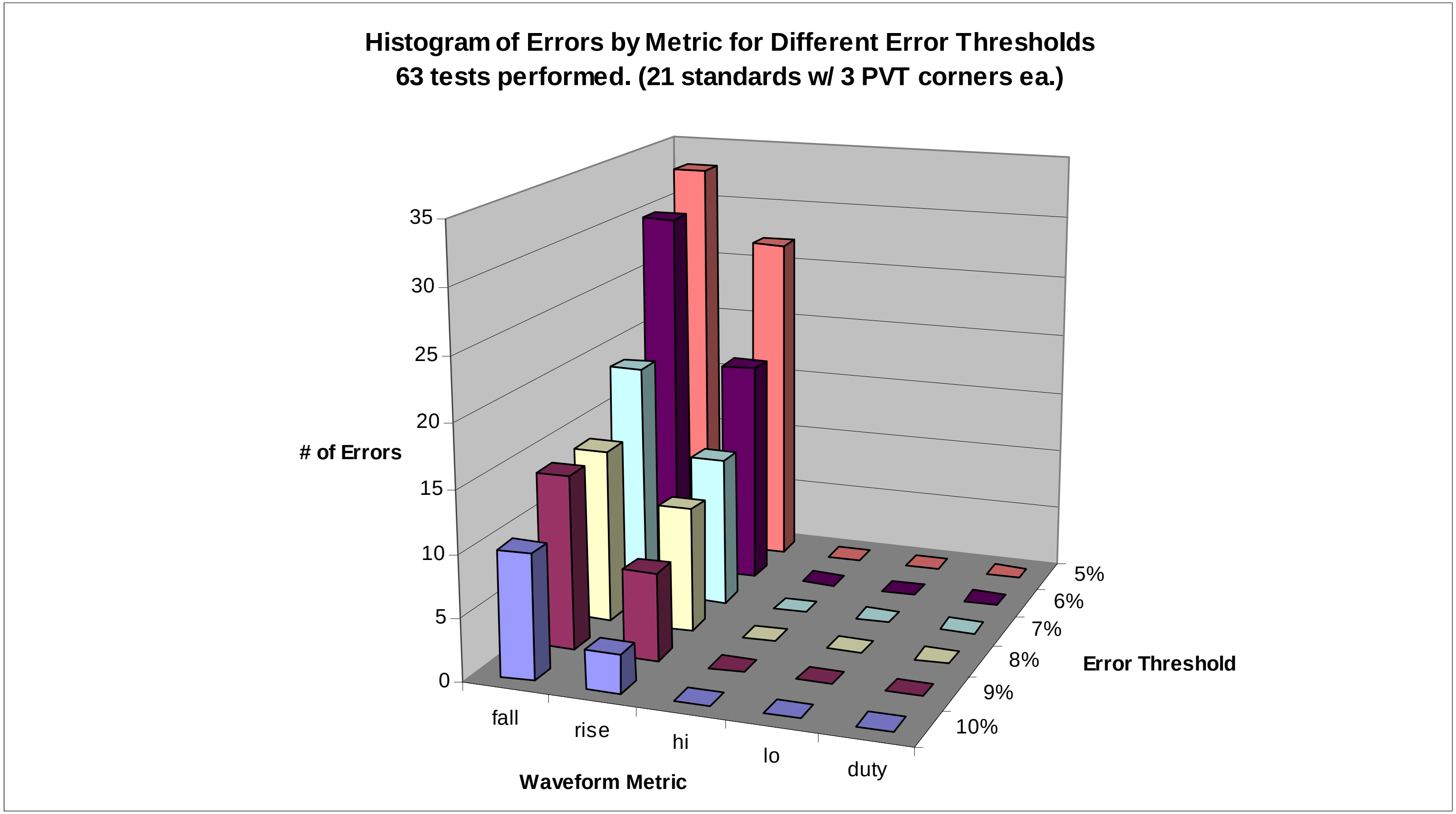




A Real World Example

“IBIS vs. Spice” Comparison

Results of a random sampling of I/O standards

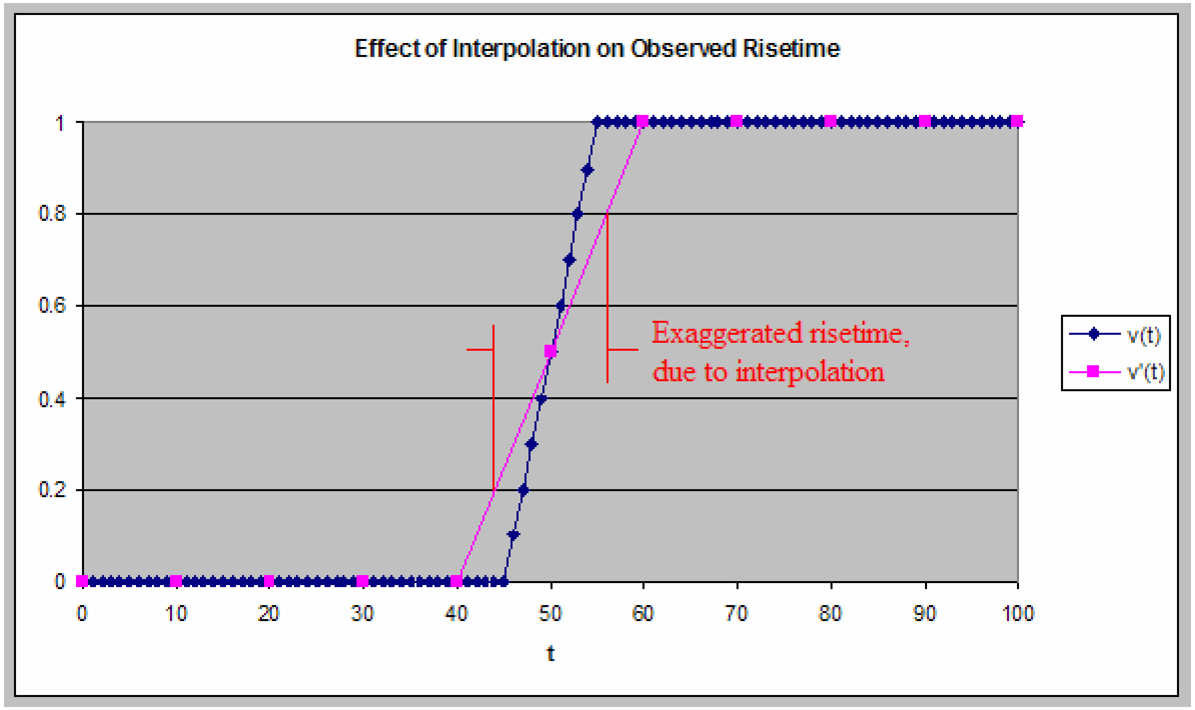


Possible Explanations for Discrepancies

- IBIS drivers are weaker than Spice drivers?
  - Survey says, “Annggch!”
  - If they were, we’d see errors show up in the “High” and “Low” metrics, as well. (This is a great example of the utility of breaking the comparison up into metrics!)
- Might the linear interpolation between data points in the IBIS V/T tables be the cause?...

Cause of Rise/Fall Errors Identified

- Yes! Observe:



Rise/fall-time errors due to interpolation, NOT weak IBIS drivers!

Measurement Automation

Example Spice Deck Excerpts

- The Spice "B" element can be used to instantiate IBIS buffers. This allows a single Spice deck to compare the Spice and IBIS drivers side-by-side.

```
B1_io nd1_pu nd1_pd nd1_out clkin 0
+     V_out_of_in1 [nd1_pc nd1_gc]
+ file = '../../../virtex5.ibs'
+ model = 'HSTL_I'
+ typ = 'typ‘
```

- Also, Spice *.MEASURE* directives can be used, in order to automate the measurement and comparison of the 5 waveform metrics.

(Example Spice syntax on next page.)

```
* An arbitrary threshold of max/2 is used to "bootstrap" the measurements.

.MEASURE TRAN max_sp MAX v(rnr_pad)
+ FROM = "5ns"
+ TO   = "5ns + clk_period"

.MEASURE TRAN half_max PARAM="(max_sp/2)"


* Measure the delays in the first rising edges of IBIS and Spice waveforms.
* This tells us where to take our "high" and "low" averages.

.MEASURE TRAN dly_sp
+ TRIG AT=5ns
+ TARG v(rnr_pad) VAL=half_max TD=TRIG RISE=1

.MEASURE TRAN dly_ib
+ TRIG AT=5ns
+ TARG v(nd1_out) VAL=half_max TD=TRIG RISE=1


* Now, find the average "high" and "low" values, which will be compared,
* and used to calculate the "20%", "50%", and "80%" points that are used
* in subsequent measurements.

.MEASURE TRAN high_sp AVG v(rnr_pad)
+ FROM = "5ns + dly_sp + (clk_period/6)"      $ Using the middle third to
+ TO   = "5ns + dly_sp + (2*clk_period/6)"    $ calculate the high level.

.MEASURE TRAN high_ib AVG v(nd1_out)
+ FROM = "5ns + dly_ib + (clk_period/6)"
+ TO   = "5ns + dly_ib + (2*clk_period/6)"

.MEASURE TRAN low_sp AVG v(rnr_pad)
+ FROM = "5ns + dly_sp + (clk_period/2) + (clk_period/6)"
+ TO   = "5ns + dly_sp + (clk_period/2) + (2*clk_period/6)"

.MEASURE TRAN low_ib AVG v(nd1_out)
+ FROM = "5ns + dly_ib + (clk_period/2) + (clk_period/6)"
+ TO   = "5ns + dly_ib + (clk_period/2) + (2*clk_period/6)"


* Calculate 20/50/80 points.

.MEASURE TRAN eighty_sp
+ PARAM="low_sp + (high_sp-low_sp)*0.8"

.MEASURE TRAN eighty_ib
+ PARAM="low_ib + (high_ib-low_ib)*0.8"

.MEASURE TRAN fifty_sp
+ PARAM="low_sp + (high_sp-low_sp)*0.5"

.MEASURE TRAN fifty_ib
+ PARAM="low_ib + (high_ib-low_ib)*0.5"

.MEASURE TRAN twenty_sp
+ PARAM="low_sp + (high_sp-low_sp)*0.2"

.MEASURE TRAN twenty_ib
+ PARAM="low_ib + (high_ib-low_ib)*0.2"

* Measure rise/fall times.

.MEASURE TRAN tr_spice
+ TRIG v(rnr_pad) VAL=twenty_sp TD=5n RISE=1
+ TARG v(rnr_pad) VAL=eighty_sp TD=TRIG RISE=1

.MEASURE TRAN tr_ibis
+ TRIG v(nd1_out) VAL=twenty_ib TD=5n RISE=1
+ TARG v(nd1_out) VAL=eighty_ib TD=TRIG RISE=1

.MEASURE TRAN tf_spice
+ TRIG v(rnr_pad) VAL=eighty_sp TD=5n FALL=1
+ TARG v(rnr_pad) VAL=twenty_sp TD=TRIG FALL=1

.MEASURE TRAN tf_ibis
+ TRIG v(nd1_out) VAL=eighty_ib TD=5n FALL=1
+ TARG v(nd1_out) VAL=twenty_ib TD=TRIG FALL=1


* Measure duty cycles.

.MEASURE TRAN th_spice
+ TRIG v(rnr_pad) VAL=fifty_sp TD=5n RISE=1
+ TARG v(rnr_pad) VAL=fifty_sp TD=TRIG FALL=1

.MEASURE TRAN th_ibis
+ TRIG v(nd1_out) VAL=fifty_ib TD=5n RISE=1
+ TARG v(nd1_out) VAL=fifty_ib TD=TRIG FALL=1

.MEASURE TRAN tl_spice
+ TRIG v(rnr_pad) VAL=fifty_sp TD=5n FALL=1
+ TARG v(rnr_pad) VAL=fifty_sp TD=TRIG RISE=1

.MEASURE TRAN tl_ibis
+ TRIG v(nd1_out) VAL=fifty_ib TD=5n FALL=1
+ TARG v(nd1_out) VAL=fifty_ib TD=TRIG RISE=1

.MEASURE dc_spice
+ PARAM='th_spice/(th_spice + tl_spice)'

.MEASURE dc_ibis
+ PARAM='th_ibis/(th_ibis + tl_ibis)'


* Measure the errors.

.MEASURE TRAN high_err
+ PARAM="(high_ib - high_sp)/high_sp"

.MEASURE TRAN low_err
+ PARAM="(low_ib - low_sp)/low_sp"

.MEASURE TRAN risetime_err
+ PARAM="(tr_ibis - tr_spice)/tr_spice"

.MEASURE TRAN falltime_err
+ PARAM="(tf_ibis - tf_spice)/tf_spice"

.MEASURE TRAN dutycycle_err
+ PARAM="(dc_ibis - dc_spice)/dc_spice"
```

Conclusion

Summary

- I/O Buffer Accuracy Handbook provides excellent foundation for refinement of IBIS model accuracy quantification.
- Correlating specific features or *metrics* of the waveforms provides insight into the causes of any discrepancies.
- Metric measurement/comparison techniques can be automated in Spice.

Request for Comments

- Is this approach useful and/or novel enough to continue pursuing?
- Does it make sense to try and say something formal about it in the *IBIS Quality Specification*? (i.e. – Is there a need for us all to “be on the same page” when we talk about this?)
- What would you like to see added? (i.e. – other “metrics”, etc.)

Acknowledgements & References

- **Roy Leventhal** – *Model Correlation Committee* co-chair and author of *Semiconductor Modeling*.
- **IBIS Accuracy Subcommittee** – original authors of the *IBIS Accuracy Specification*, which has become the *I/O Buffer Accuracy Handbook*. (10 years ago; Wow!)
- **Xilinx IC Design Staff** – for their patience, tolerance, and timely responses to my many requests for changes/improvements to our model generation/checking procedures.
- **IBIS Quality Task Group** – for their tolerance of my propensity to dominate our meetings with my own agenda and for believing in my ability to co-chair the new MCC with Roy, despite my recent arrival on the IBIS modeling scene.

General Q&A

Thanks for Listening & Participating!