IBIS Summit Meeting

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IBIS Quality Review

A status review of the IBIS Quality specification

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(Presented by Bob Ross, Teraspeed Consulting Group)

IBIS Quality Task Group

- **Web:**

  http://www.vhdl.org/pub/ibis/quality_wip

- **Email list:**

  http://www.freelists.org/list/ibis-quality

  –**Or send email**

  To: ibis-quality-request@freelists.org

  Subject: subscribe

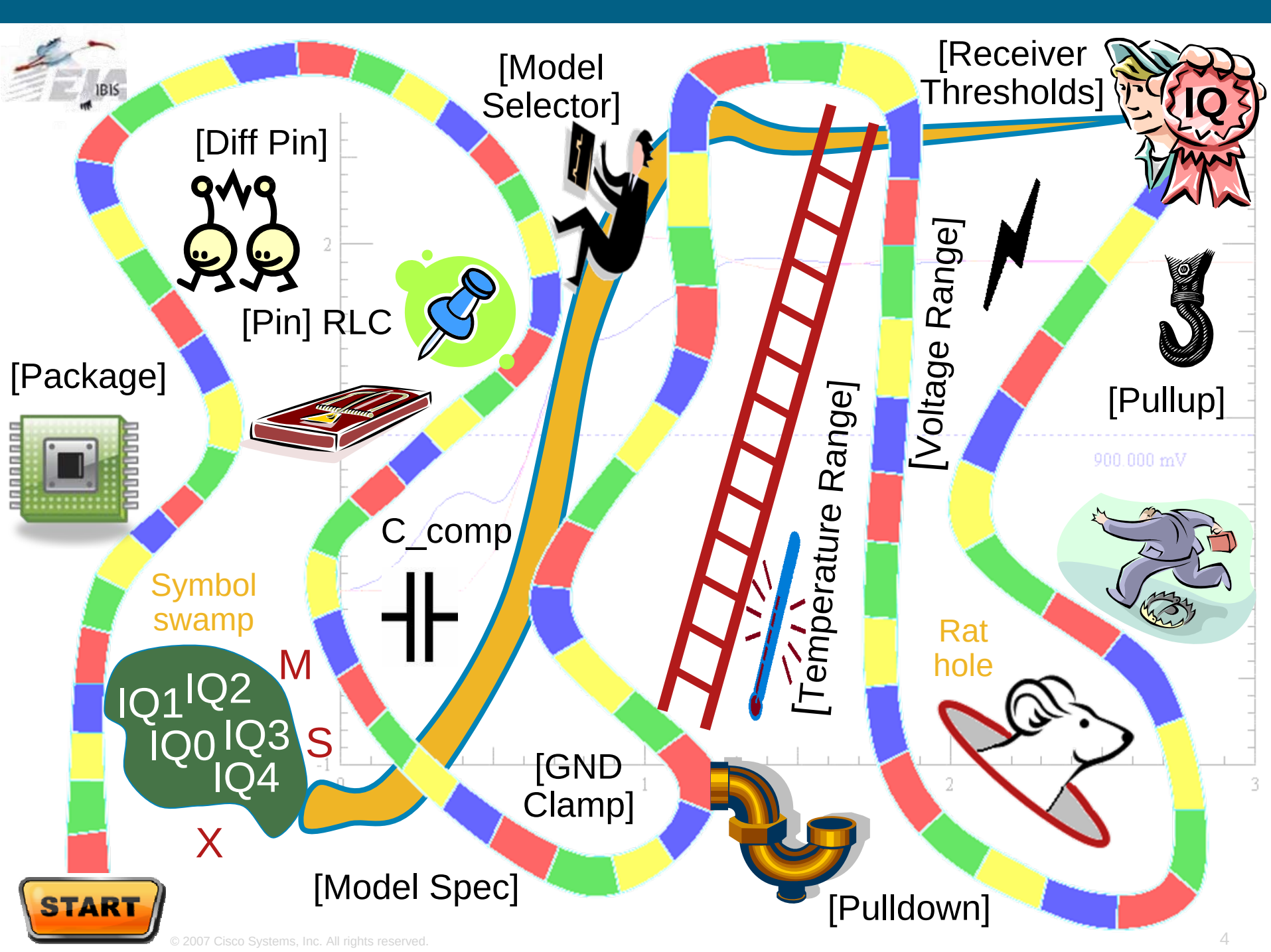
- **Meetings:**

  –**Tuesdays from 11:00am to 12:00pm Eastern Time**

- **Questions? Mike LaBonte milabont@cisco.com**

Brief History

- 2002 March - Barry Katz started IBIS-Quality
- 2004 November - IQ 1.0 specification completed
- 2005 August - Parser bug 90 submitted and approved
- 2006 March - Parser bug 94 submitted and approved
- 2006 April - Book “Semiconductor Modeling” discusses IQ
- 2006 August - IQ 1.1 specification initiated
- 2009 August – IQ 1.1 specification release expected



Specification Version 1.0

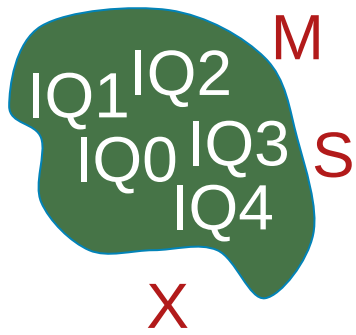
- IBIS Quality Levels
  - 0 – Can be checked by IBISCHK, plus a few others
  - 1 – Correctness, completeness, and simulation checks
  - 2a – Simulation correlated
  - 2b – Bench measurement correlated
  - 3 – Simulation and measurement correlated

Issues with IQ Version 1.0

- Passing IQ Level 0 does not sound like much of an accomplishment
  - Is a non-compliant file level -1?
- There should be a strict level for “Passes IBISCHK”
- No other IQ check should duplicate IBISCHK
- Can’t have a correlated model without full IQ check
- Some checks are weak (“should” vs. “must”)
- Feedback from JEITA

Specification Version 1.1

- IBIS Quality Levels
  - IQ0 – Not Checked
  - IQ1 – Passes IBISCHK
  - IQ2 – Suitable for Waveform Simulation
  - IQ3 – Suitable for Timing Analysis
  - IQ4 – Suitable for Power Analysis * (defined, but no checks)
- Special Designators
  - S – Simulation correlated
  - M – Measurement correlated
  - X – Exceptions
  - G – Has Golden Waveforms



The Only LEVEL 1 Check (IBISCHK)

2.1 {LEVEL 1} IBIS file passes IBISCHK

IBIS models are expected to pass the checks performed by the IBISCHK program before they are released to the public. Passing IBISCHK insures that the file will attain at least an IQ1 level designation. The IBISCHK program is found at http://www.eigroup.org/ibis/tools.htm.

A best practice is to insert the full output from the IBISCHK program into the IBIS file as comments, with explanation for any warnings annotated within. When doing this it is important to insure that the added comments do not cause new “line too long” IBISCHK warnings.

In general it is best to use the latest available version of the IBISCHK program, as the latest version may include new tests and fixes for bugs found in the older versions. The IBISCHK program used must, at a minimum, be able to accommodate the [IBIS Ver] of the IBIS file at hand. The [IBIS Ver] used in the IBIS file is set by the model maker based on the set of IBIS keywords required to completely and correctly represent the behavior of the part. The [IBIS Ver] value can be set to at least 3.2 because this version is supported by a wide variety of EDA tools.

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Example LEVEL 2 Checks (Waveforms)

5.2.5 {LEVEL 2} [Model Spec] S_Overshoot subparameters complete and match data sheet

All input and I/O buffers have S_overshoot_high and S_overshoot_low in the [Model Spec] section. The values must match the voltage limits beyond which the device may not function correctly. These limits may be different from the absolute maximum ratings, which may be related to device destruction. The functional limits may not be found in some data sheets.

5.2.6 {LEVEL 2} [Model Spec] S_Overshoot subparameters track typ/min/max

When overshoot voltage limits are different in min and max corners, S_overshoot_high and S_overshoot_low should track these differences. For example, S_overshoot_high may increase with the higher supply voltage assumed for max mode.

Example LEVEL 3 Checks (Timing)

3.2.2. {LEVEL 3} [Pin] RLC parasitics are present and reasonable

For a LEVEL 2 model, pin parasitics are optional, but they are mandatory for a LEVEL 3 model (that is, a model suitable for timing). To pass this check the RLC values must be present for all signal pins in the [Pin] section, or [Package Model] must be present. Pin parasitics should either be measured or extracted using a 2D or 3D solver. Reasonable signal pin parasitics will result in impedance and delay characteristics that fall in the ranges:

TD = SQRT(LC) < 300ps

Z0 = SQRT(L/C) < 100ohm

Note that IQ check 3.1.2. also requires that each [Pin] RLC value falls within the min/max range as given by the [Package] keyword. The [Package] keyword can be adjusted to accommodate.

3.3.1. {LEVEL 3} [Diff Pin] Vdiff and Tdelay_* complete and reasonable

For input and I/O pins Vdiff must be defined, non-zero and positive. For output and I/O pins Tdelay_typ, Tdelay_min, and Tdelay_max data can be zero, but must be defined. Both Vdiff and Tdelay_* are measured relative to the die pads and must not include additional package delays and offsets. Output pins should have NA for Vdiff. For input pins Tdelay_typ, Tdelay_min, and Tdelay_max must be NA.

No Level 4 Checks (Power)

- A [Pin Mapping] Complete and Correct check was proposed
- Power analysis really needs new features:
  - BIRD95 - Power Integrity Analysis using IBIS
  - BIRD98 - Gate Modulation Effect (table format)
- IBIS 5 adoption still in progress
  - Not yet an EIA/ANSI standard
  - IBISCHK 5 parser in development now
  - Have not yet seen IBIS 5 power keywords in IBIS files
- IQ 1.2 will have level 4 checks

Notes on IQ Version 1.1

- “Possible Errors” section removed
  - Some items made into regular checks
- “Correlation” section minimized
  - Refers to IBIS Accuracy Handbook for details
- IC vendor push-back on overshoot parameters
  - Not many IBIS files have this
  - Buffer developers simply do not measure it
  - Difference between functional and destruction limits
  - BIRD103 D_overshoot parameters may work better

IQ Version 1.1 Status

- 44 draft revisions posted
- In editorial review phase
  - Going through feedback from Anders Ekholm
  - Need to have consistent spelling of terms, etc
- Probably will take 5 or 6 more meetings

After Version 1.1

- File parser bug reports
- Update the IBIS Accuracy Handbook
  - Emphasis on feature-selective correlation
- Begin drafting IQ 1.2
  - Level 4 power analysis checks

Regular 2009 IQ Meeting Participants

- Cisco Systems
- Ericsson
- Huawei Technologies
- Micron Technology *
- Nokia Siemens Networks
- Texas Instruments *
- Teraspeed Consulting Group *
- Xilinx *

* IBIS model makers

Not participating: JEDEC

- IC makers increasingly defer to JEDEC specs
  - IBIS gets lower priority
  - Lack of certain keywords is a barrier to IQ compliance
- JEDEC specifies parameters beyond IBIS
- Why so few IBIS files with [Receiver Thresholds]?
  - Developed for JEDEC DDR conformance
  - DDR2 “area” specs go beyond [Receiver Thresholds]
  - BIRD103 addresses this in IBIS 5
- JEDEC could produce IBIS files to facilitate adoption