Signal Integrity/ Power Integrity Co-analysis for I/O Interfaces

Myoung Joon Choi, Vishram S. Pandit
Intel Corp.
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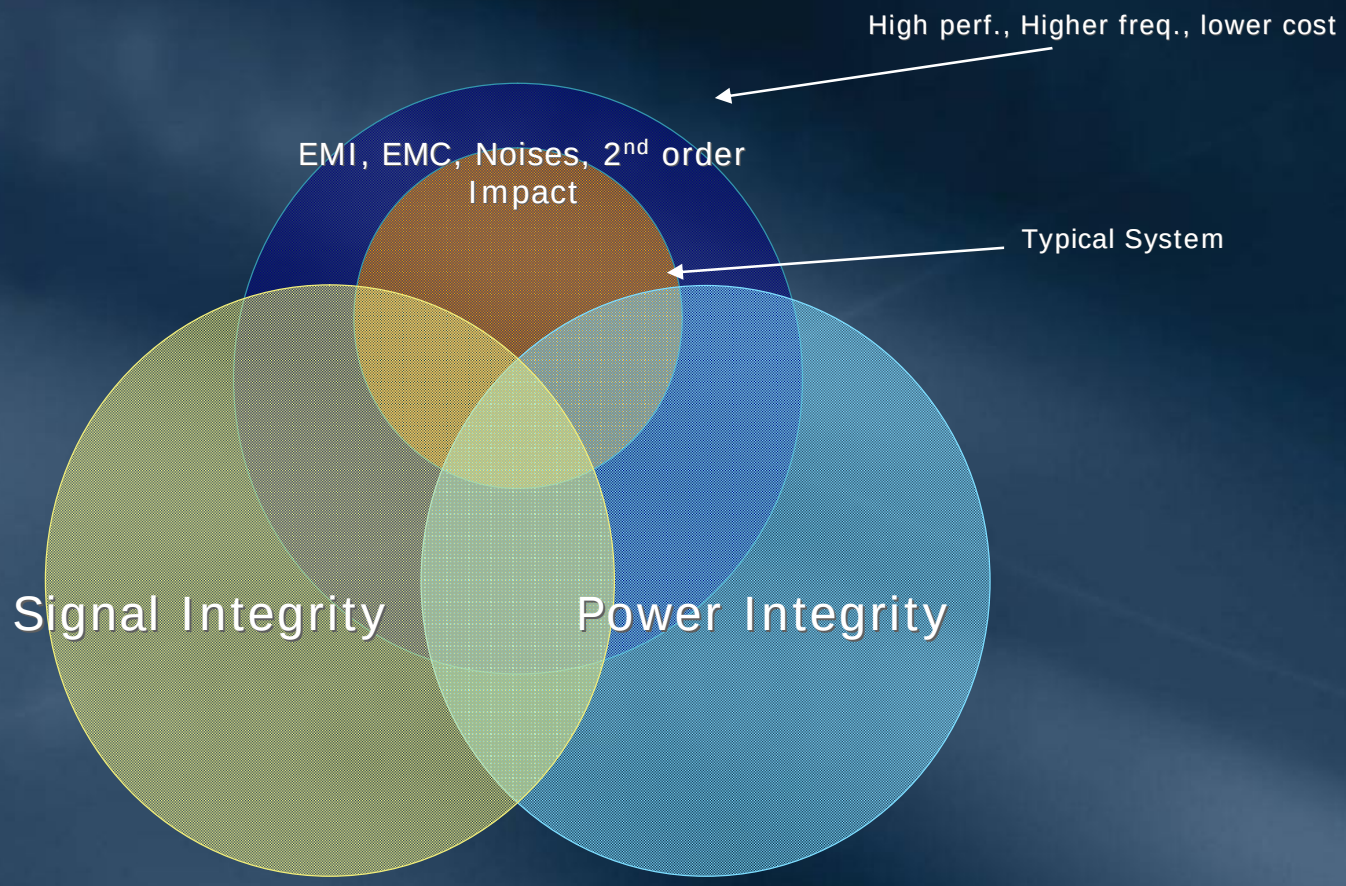
Michael Mirmak, Woong Hwan Ryu, Joe Salmon

Special thanks to Wei-hsing Huang for SI-PI buffer model

Outline

- SI-PI Motivation, Requirement
- Overview
- Buffer Requirement
- SI-PI Co-simulation Methodology
- Lab Correlation
- SI-PI Full Time Domain Simulation
  - Single Ended Signaling
  - Differential Signaling
- Conclusions

SI-PI Interaction

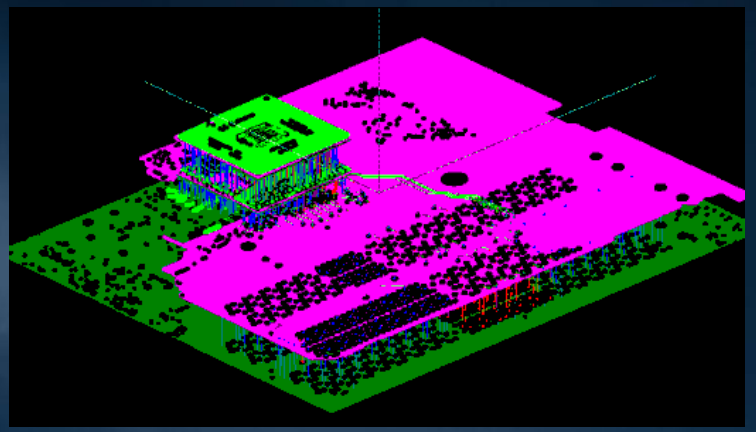


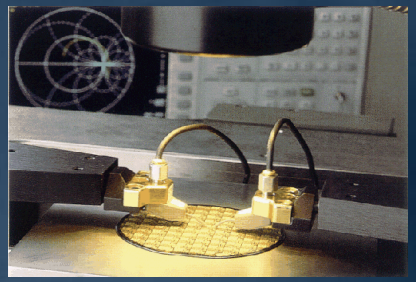
Motivation

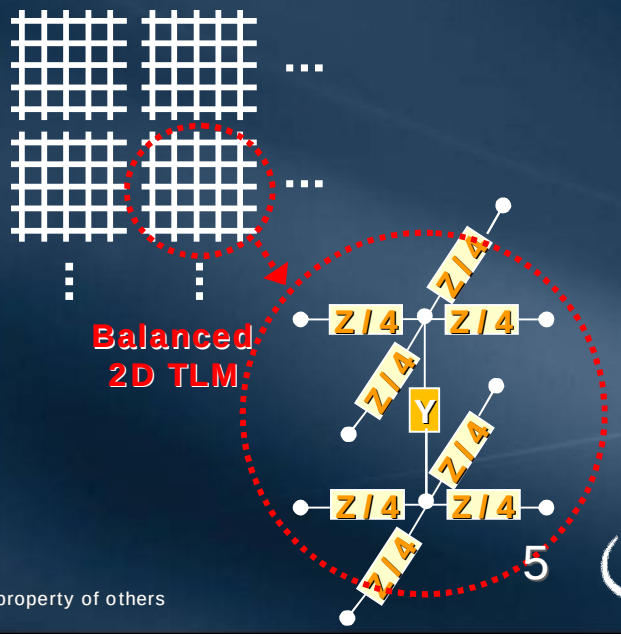
- What is SI-PI Co-sim?
  - Conventional Analysis
    - SI-only: ISI, Xtalk
    - PI-only: PD noise
  - SI-PI: System level simulation including SI and PI altogether
- Why SI-PI Co-sim? Need to save more margin?
    - Where? SSN, 3D coupling
  - System performance
    - Does SI-only or PI-only Simulation reflect my expectation?
  - PD to Signal coupling?
    - SSN
    - Referencing
    - PD to Signal cross-talk
  - PD impact on receiver eye, Jitter?

What do I need to run SI-PI ?

- Buffer model !
  - Multiple buffer Switching simulation
  - Accurate for SI & PI
  - Icc(t)
- Package, PCB, Connector
  - 2, 2.5D, 3D model
  - Coupling between PD and SI
- On-die PDN model
  - Powergrid
  - Cdie, Rdie







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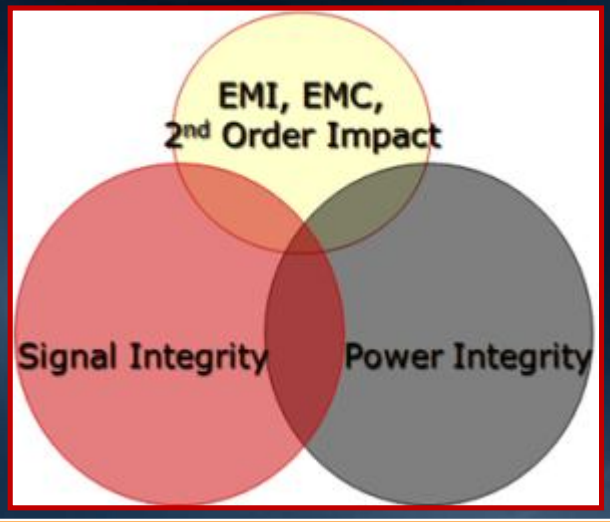
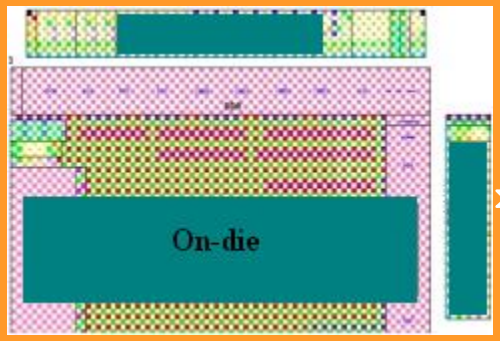
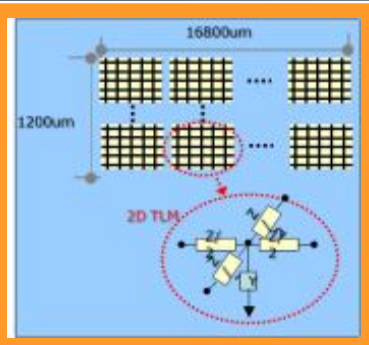
SI-PI Co-sim Overview

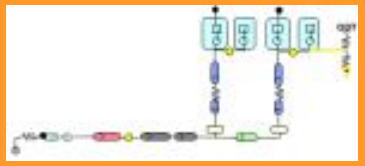
<Buffer, On-die Model> Indispensible to SI-PI Co-sim

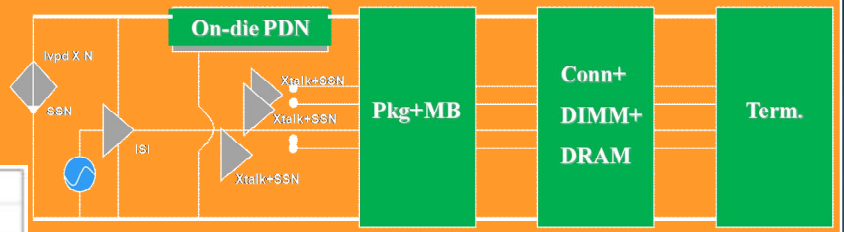


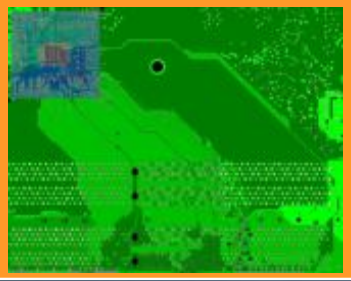
<SI-PI co-sim>
- **PD-to-SI interaction**
- **Assess Cdie**
- **Referencing Impact**
- **3D EM impact**

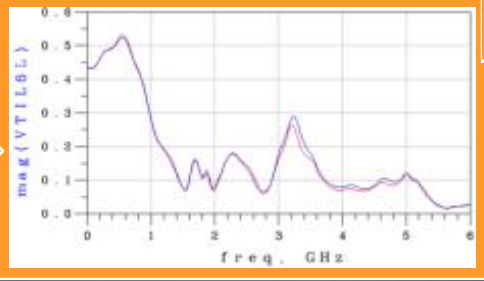












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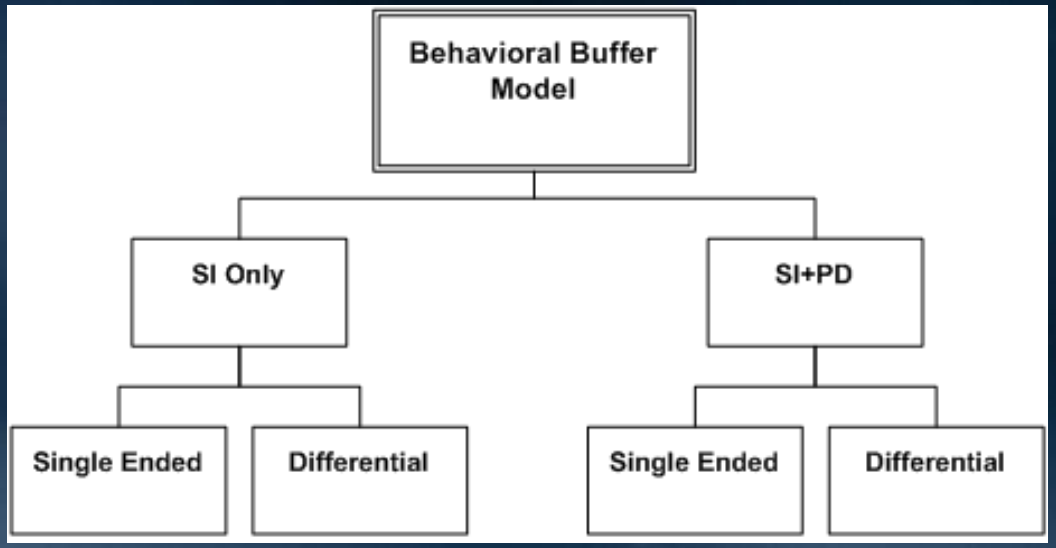
Buffer Behavioral Model

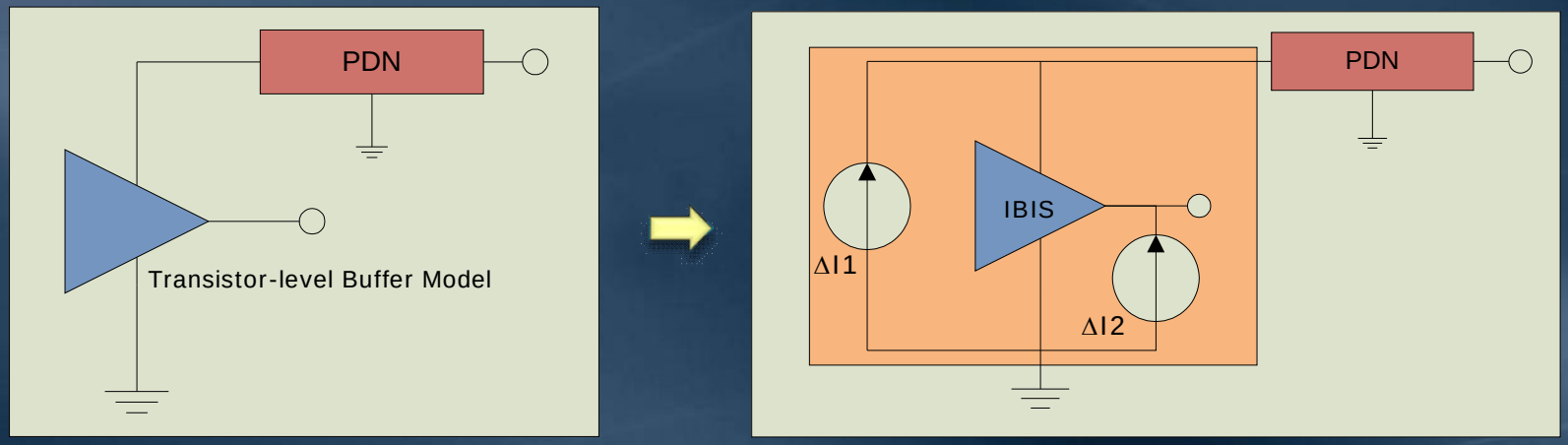


- SI only
  - I/V and V/T characterization, C_comp**
- SI+PD
  - I/V and V/T characterization, C_comp**
  - Ability to accommodate PD level variation
  - Output timing/voltage variation based on PD noise

** C_comp(Freq, V) is not used here but recommended

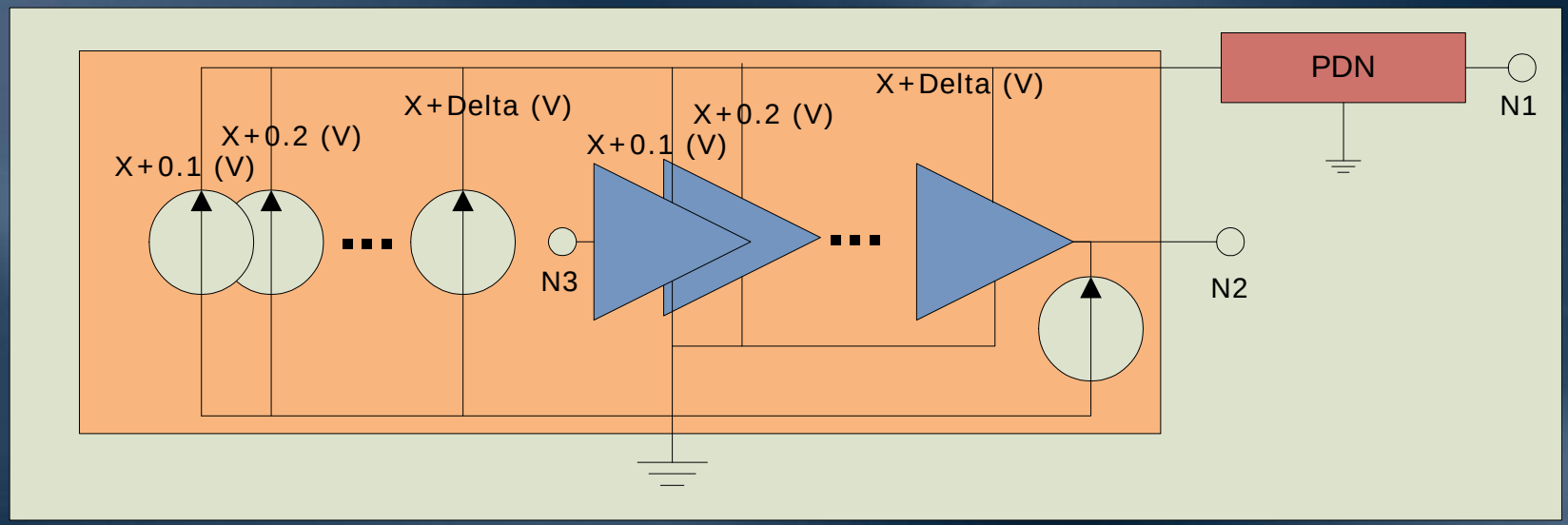
Buffer Model

- **SI-PI behavioral model:**
  - Work with existing IBIS model
  - Add ΔI1 and ΔI2 to account for difference between Xtor and Ibis;
    - Verilog-A module: Table based
      - Instead of using IBIS keywords - ISSO_PD, ISSO_PU
  - ΔI1 is f(Vccd, t, Vout)
    - account for Icct difference
  - ΔI2 is f(Vccd, t, Vout)
    - account for jitter/buffer strength difference;



Buffer Model

- **Conceptually, the generated model is like this..**
  - Has many ICCT data extracted at different conditions;
  - Has many VPAD (VT/IV) data extracted at different conditions;
  - Switches toggle dynamically during simulation based on V(N1~N3)



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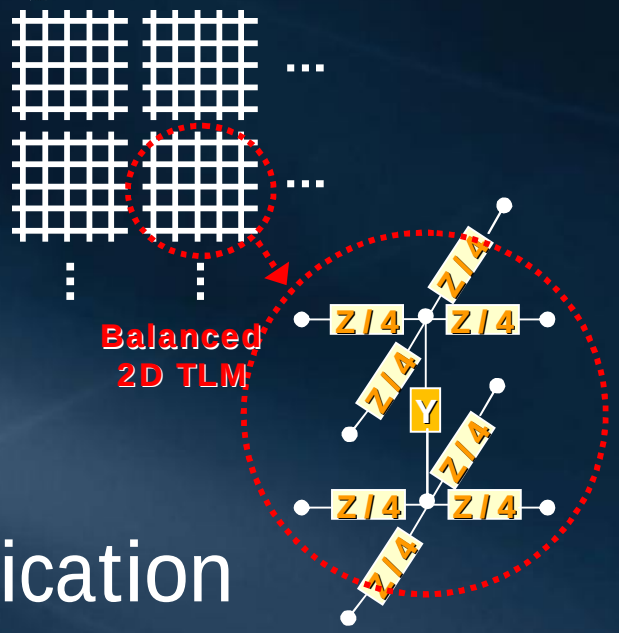
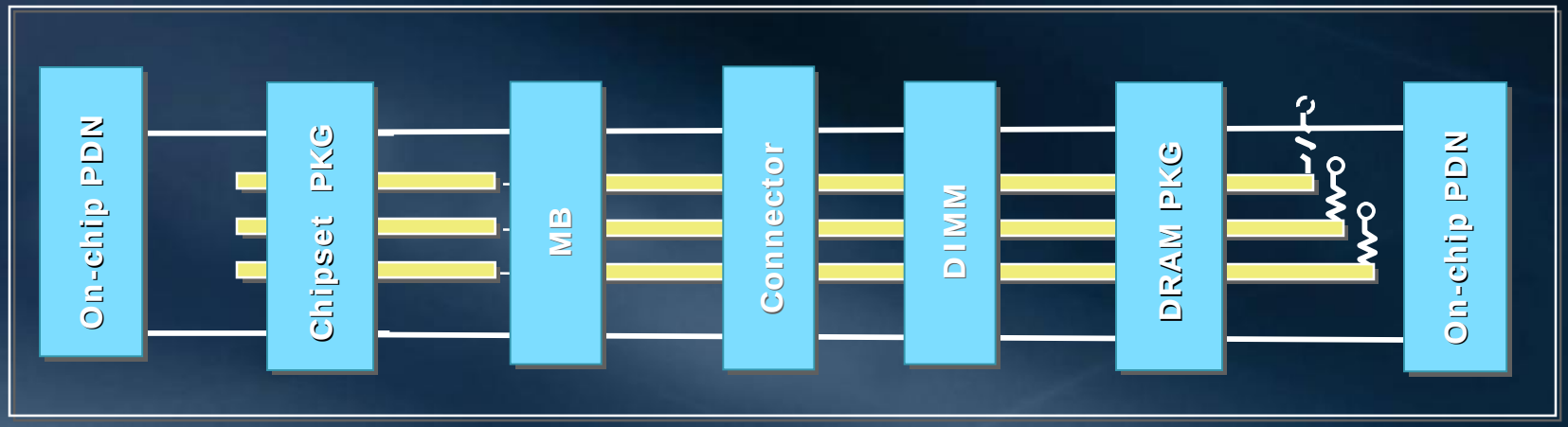
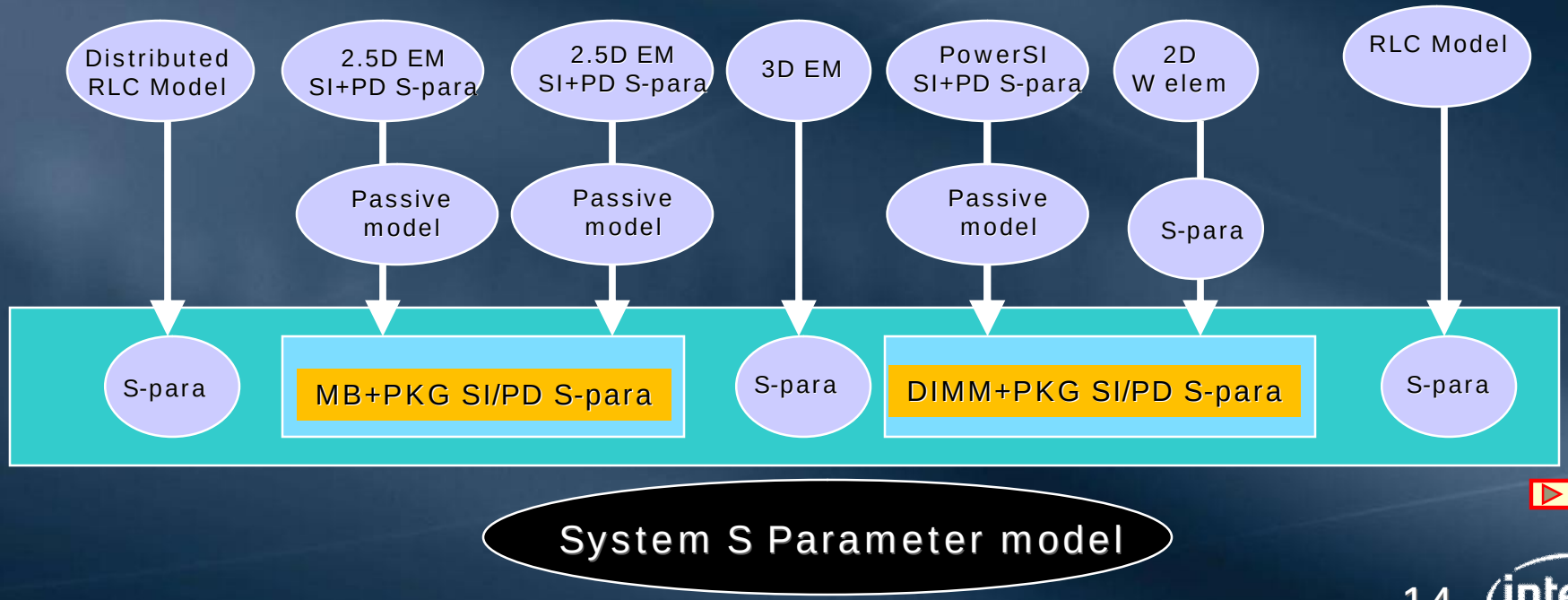
SI-PI Co-simulation Steps

1. Buffer model
2. On-die PDN Model
3. SI-PI EM Model
4. Deck Construction
5. Worst Case pattern identification
6. Full Time Domain Simulation Run
7. Response Decomposition
8. Sensitivity Analysis



SI+PD Model Generation



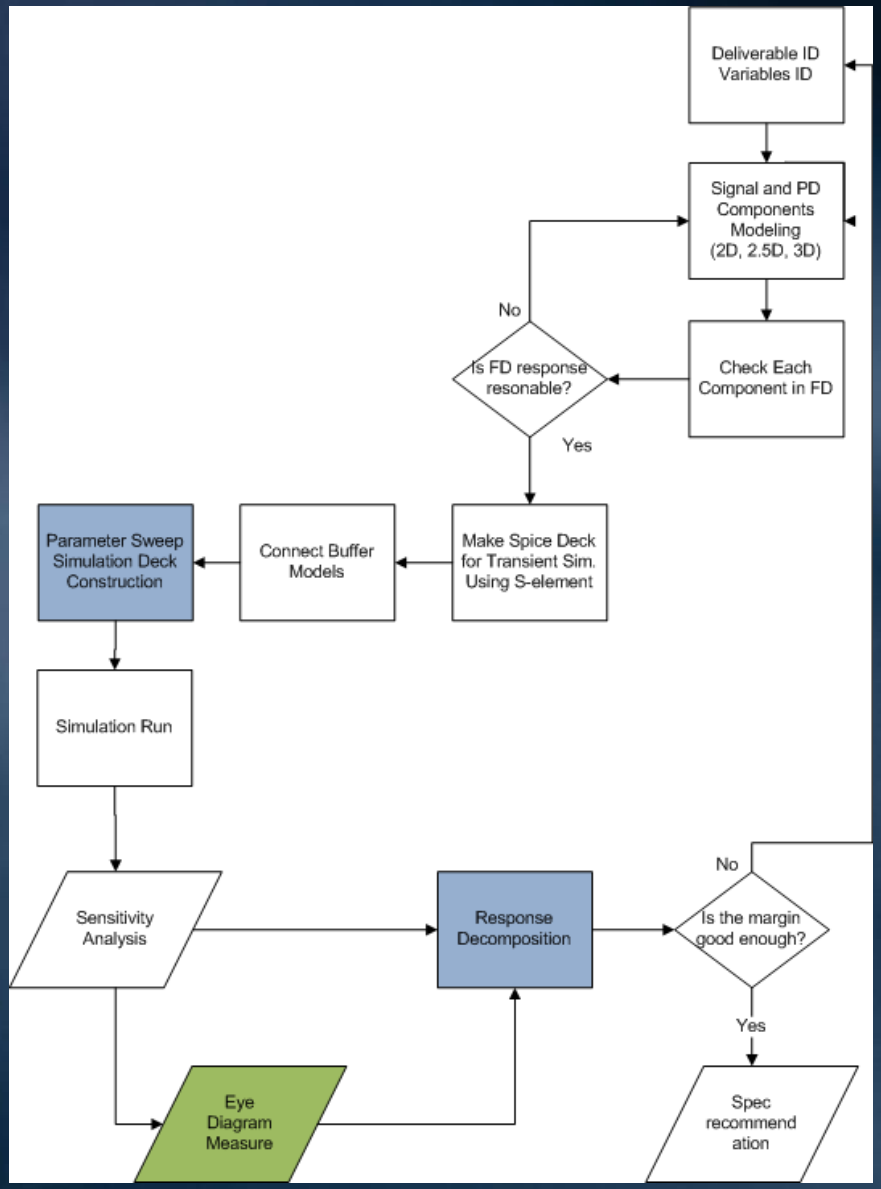


System S Parameter model

S parameter quality

- S parameter preconditioning is key to successful SI/PD simulations
- Convergence: The TD solution need to converge (DC and AC)
  - Tool Improvement
    - HSPICE 2009.03-SP1*, Sigrity PowerSI 9.0*, Ansoft HFSS 11*, Ansoft Siwave 4*.
- Passivity: Energy transferred cannot exceed energy stored
- Causality: Response cannot occur before the stimulus
- Singularity: Z response shall not go to infinity
- DC point: S parameters shall include DC point
- LF points: Tool needs to simulate LF points accurately.
- Reference Impedance: Zref for signal nets and power nets

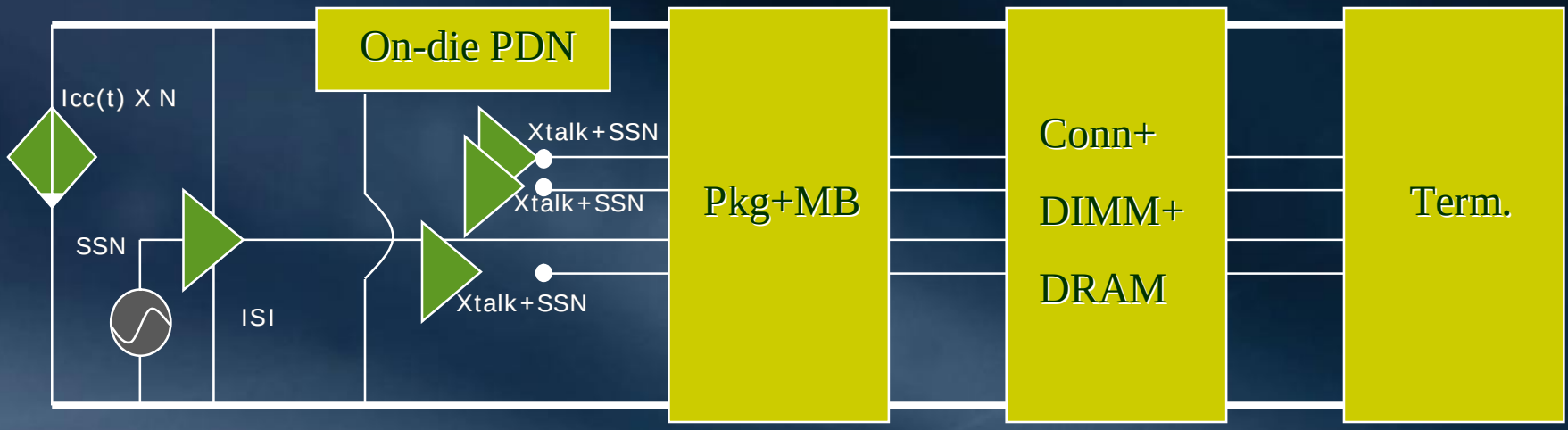
SI-PI Co-sim Run Flow



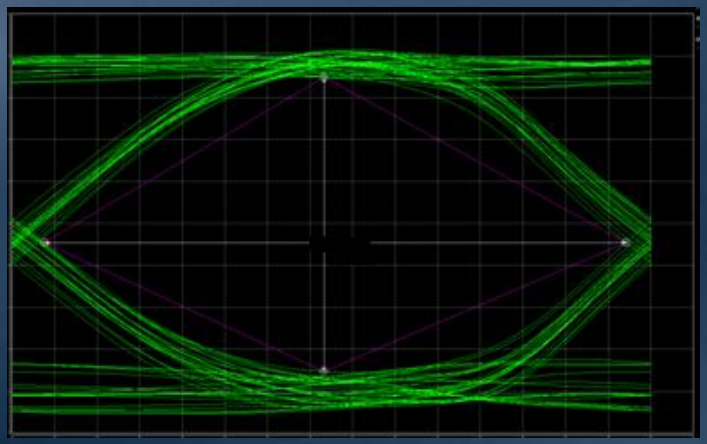
For SE

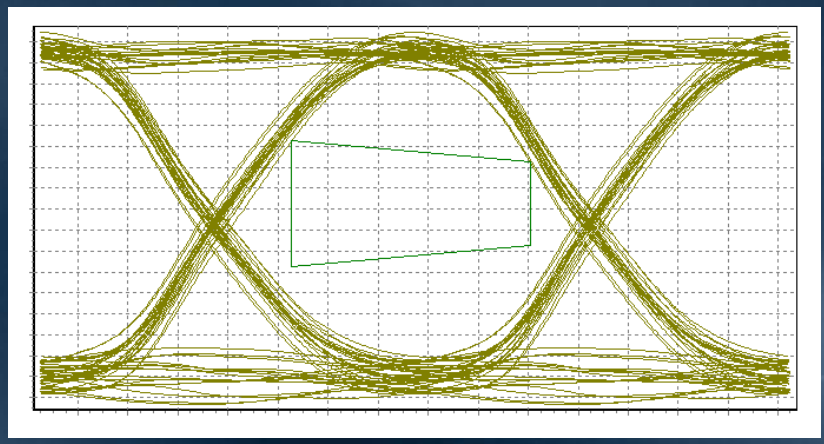
- Sim Run (Full TD Sim)
  - 0: PDA* for WC pattern[1,2]
  - 1: ISI-Only
  - 2: ISI+SSN
  - 3: ISI+XTALK+SSN
  - 4: ISI+SSN*N
  - 5: ISI+XTALK+SSN*N
- Eye Meas.
  - AC/DC
  - Differential
- Response Decomposition
  - ISI
  - Xtalk
  - SSN

Full Time Domain simulation of entire SI-PI

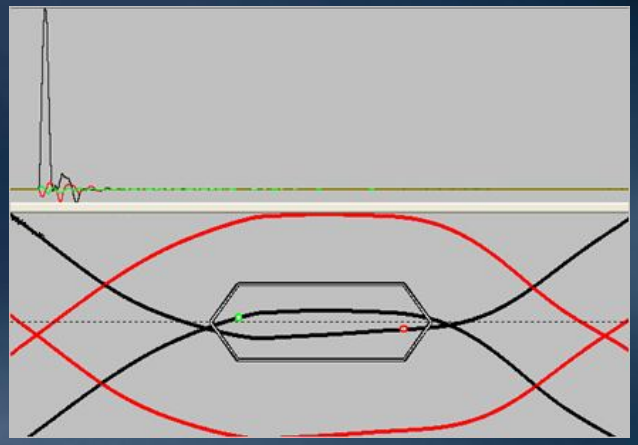


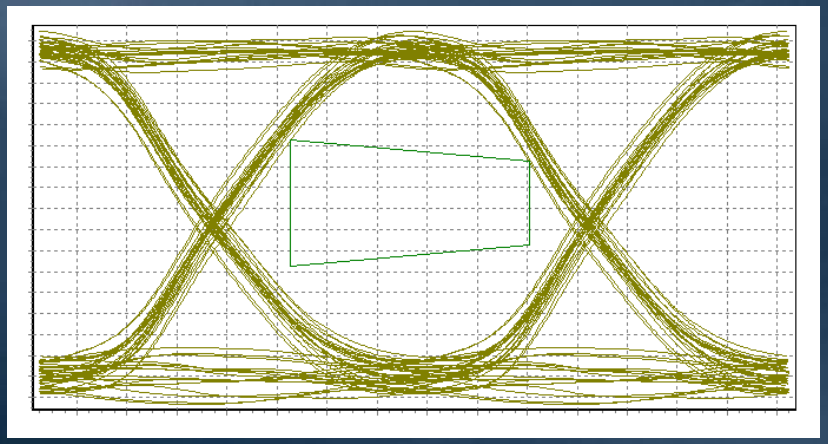
DDR Single Ended Signaling Example





Non-linear Impact?





- WC pattern from PDA* [1,2]
  - Used for full time domain Sim
  - Doesn't match
    - WC eye from PDA
    - Full time domain Eye
  - PDA Difficulty
    - Applying SSN
  - SI: LTI, PI: LTI
  - SI-PI
    - Somewhat non-linear
      - Superposition will have 0~20% error

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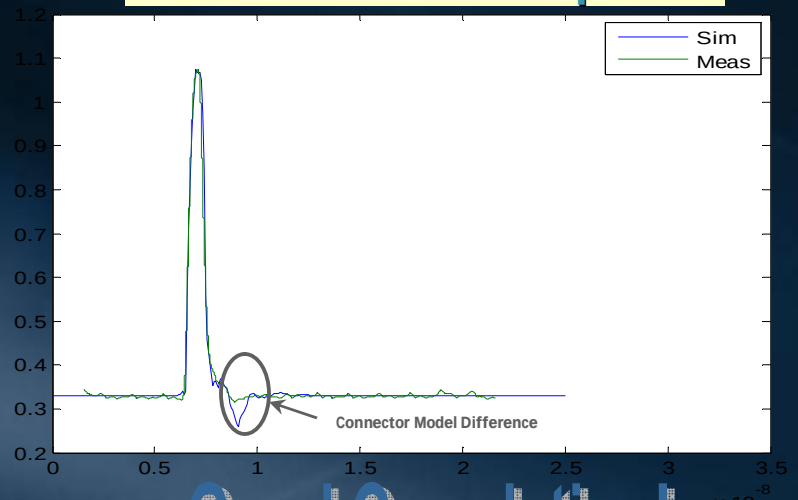
SI-PI Co-sim Correlation

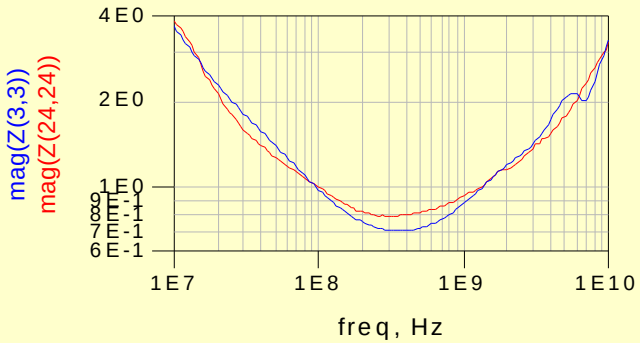
Chipset Platform

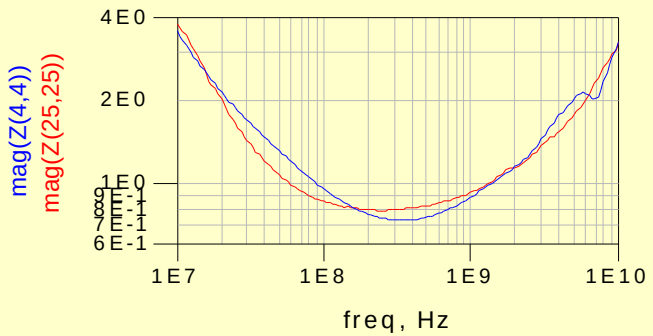
Channel Pulse Response



Good Correlation!

On-Chip PDN





Simulated

Measured

Accurate Distributed Powergrid model
=> Ability to attach more # of Buffers

<PDN Cdie Impact>
Matched ~ within 10pS

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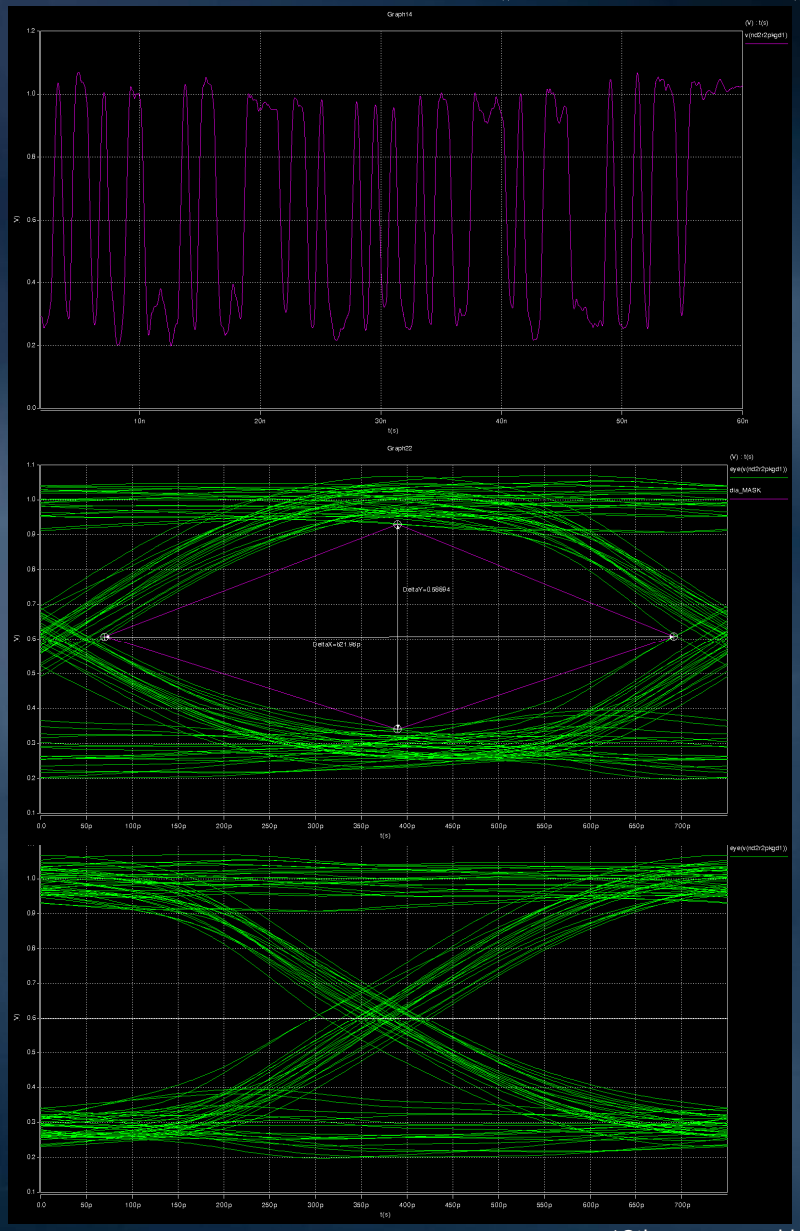
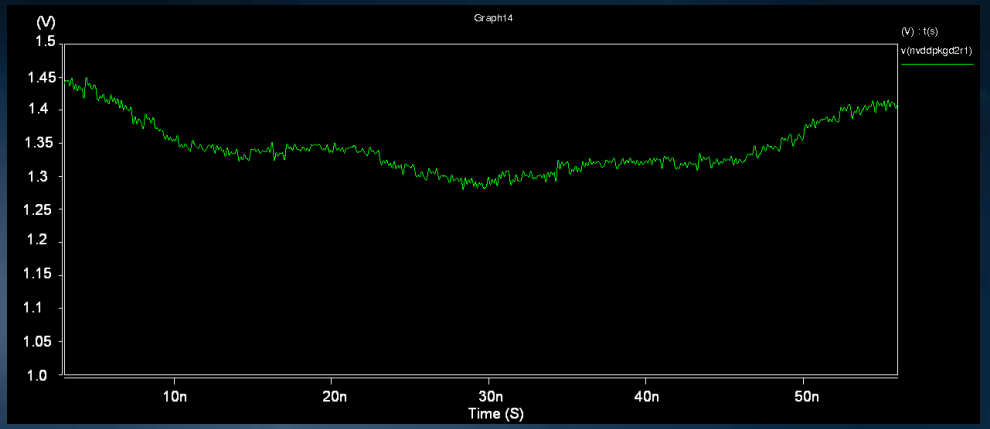
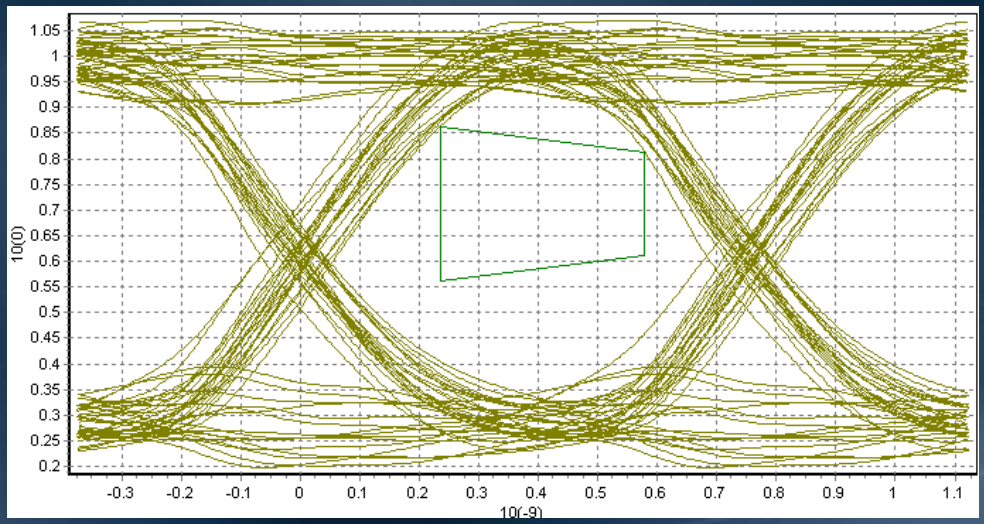
Case: MB #1

- Single Ended Signaling
- DDR Channel Performance
  - Package Impact
  - Cdie Impact
  - MB Impact
- SI-PI Sim Result: Decision making aid

Y-Layer Pkg, MB#1, XnF/Ch







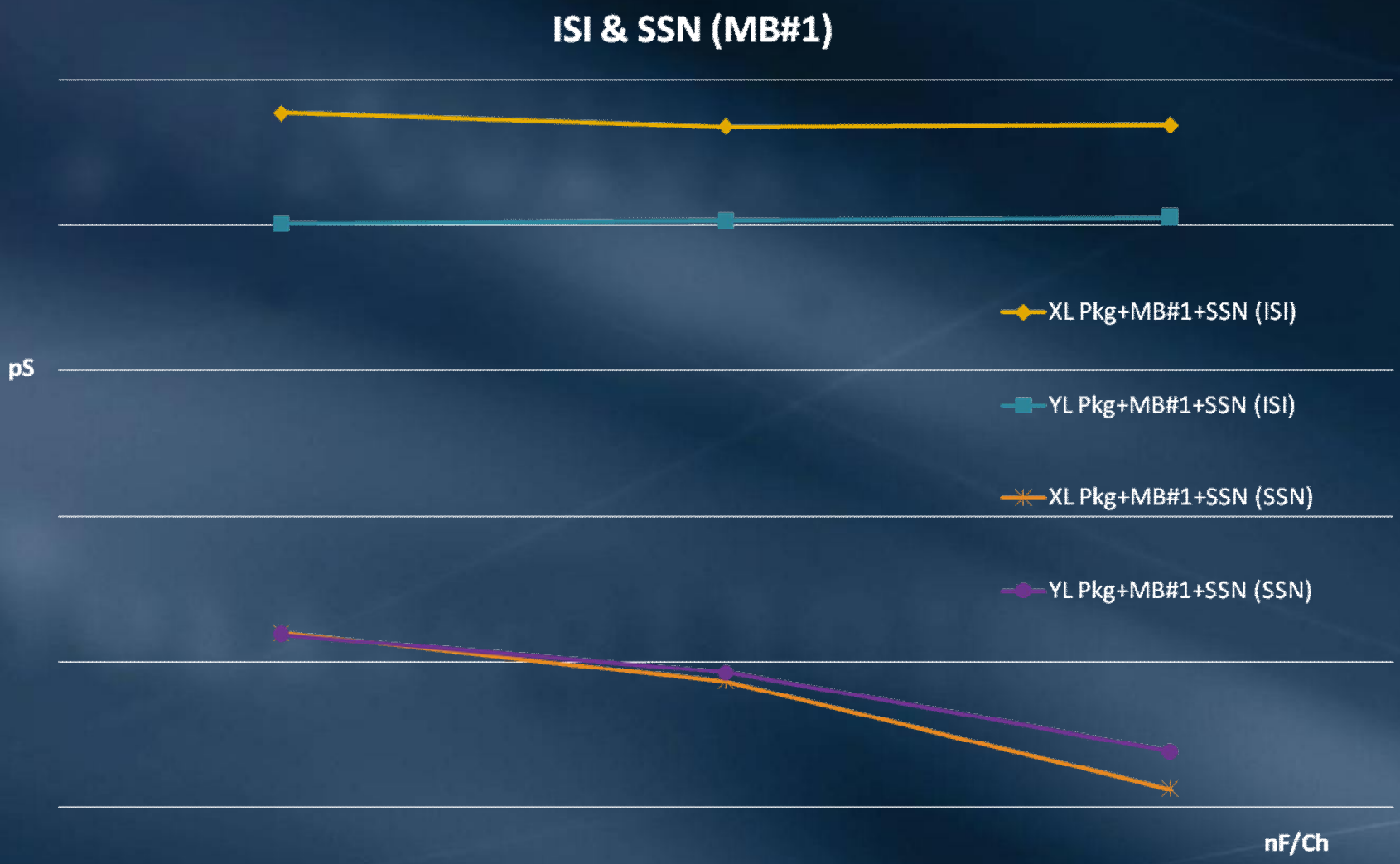
*Other names and brands may be claimed as the property of others

DDR Application: Full TD Sim.

<MB #1>
Pkg #2 @ XnF/Ch – Pkg #1 @ XnF/Ch ~ 30p
Pkg #2 @ YnF/Ch – Pkg #1 @ YnF/Ch ~ 10p

No Freebie! – Want to go to Pkg #1? Add more Cdie!

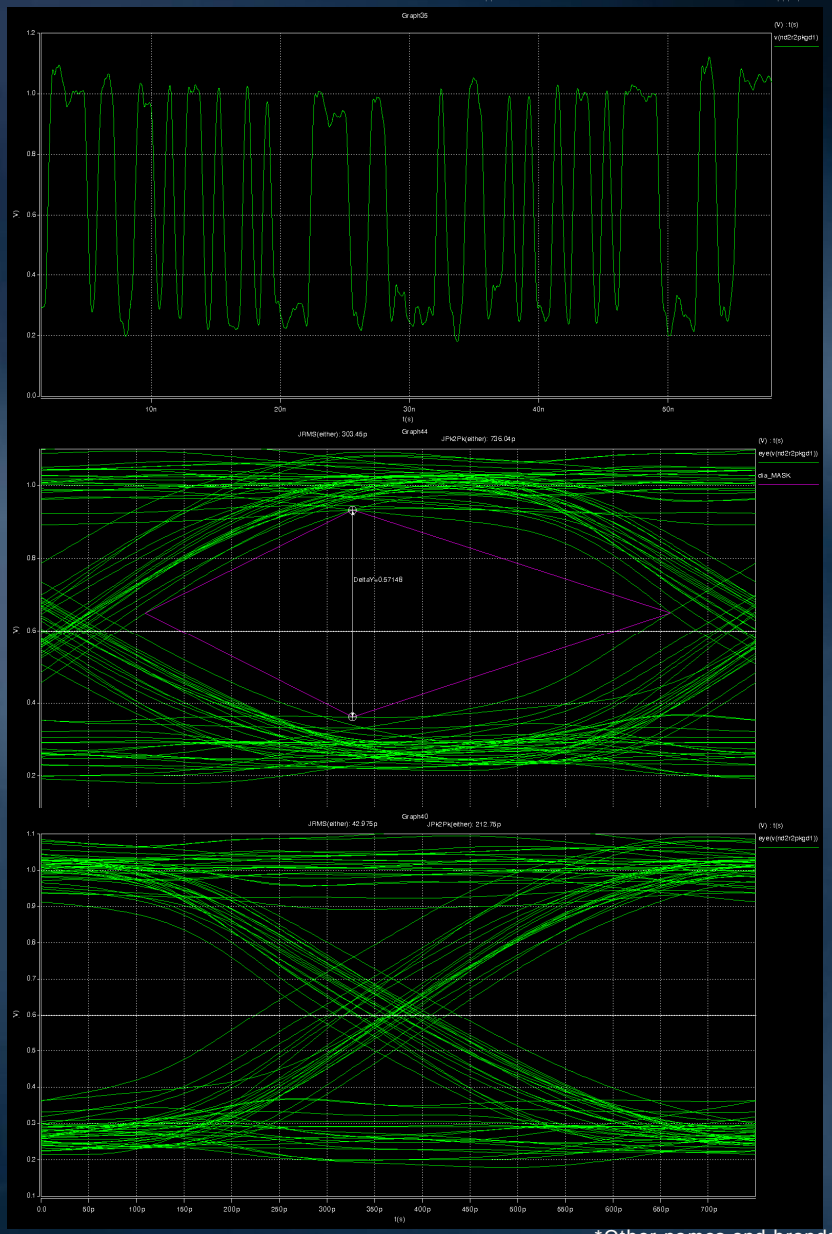
Noise (MB #1)

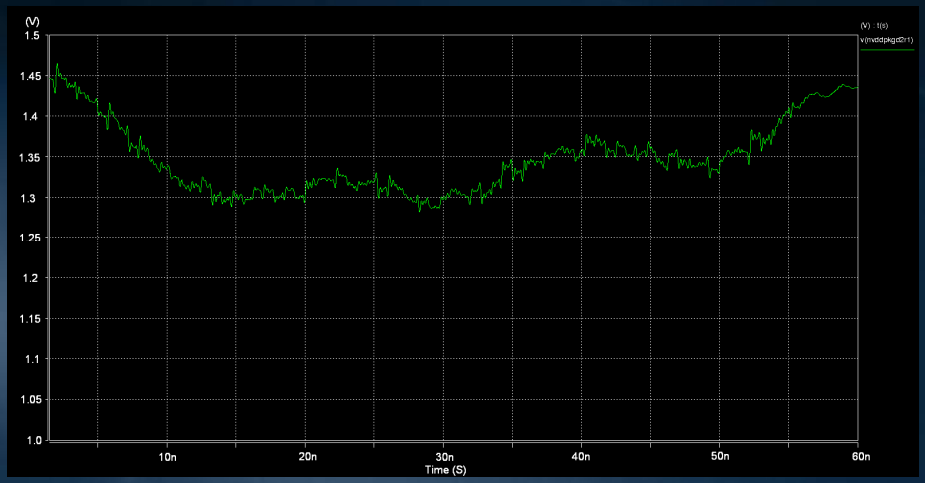


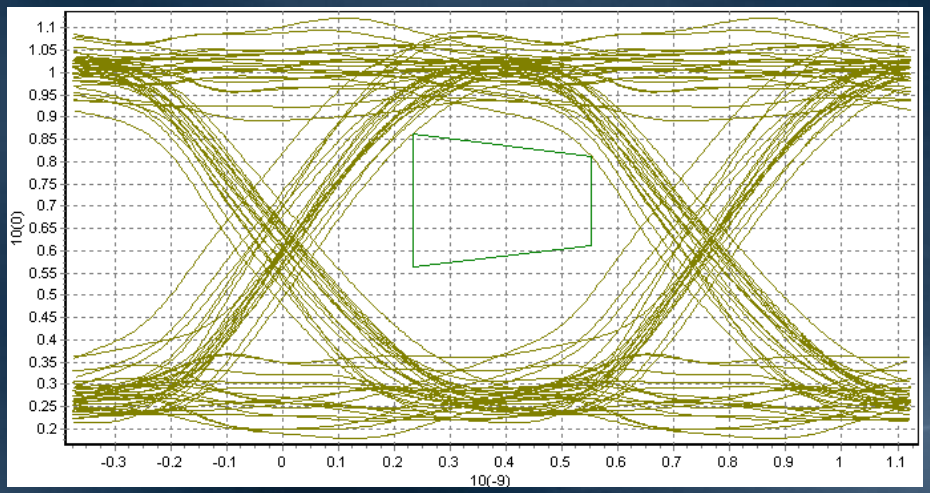
Case: MB #2

- Single Ended Signaling
- DDR Channel Performance
  - Package Impact
  - Cdie Impact
  - MB Impact
- SI-PI Sim Result: Decision making aid

Y-Layer Pkg, MB#2, XnF/Ch







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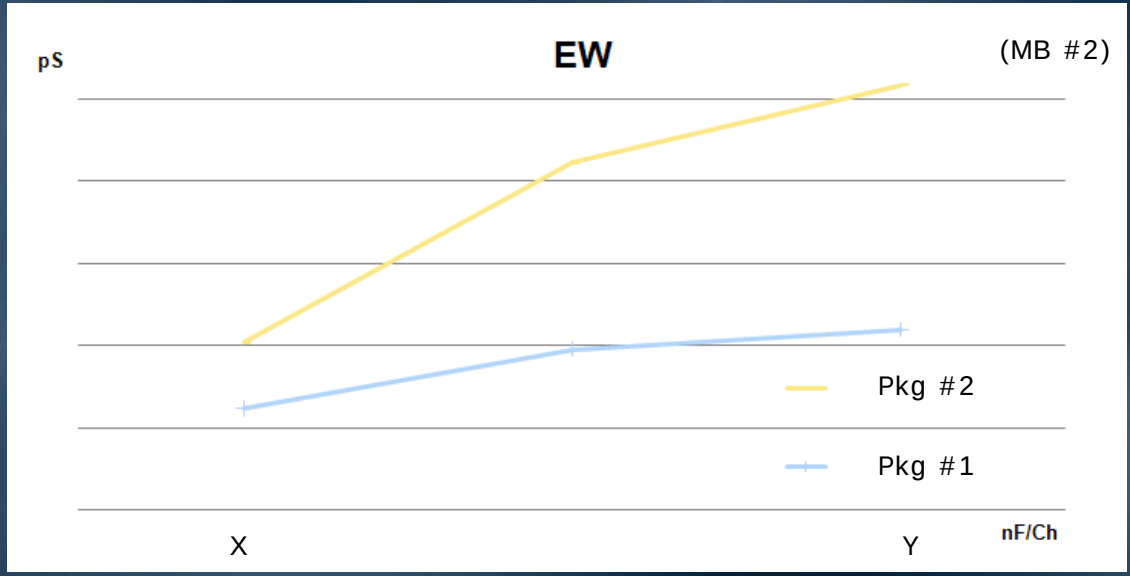
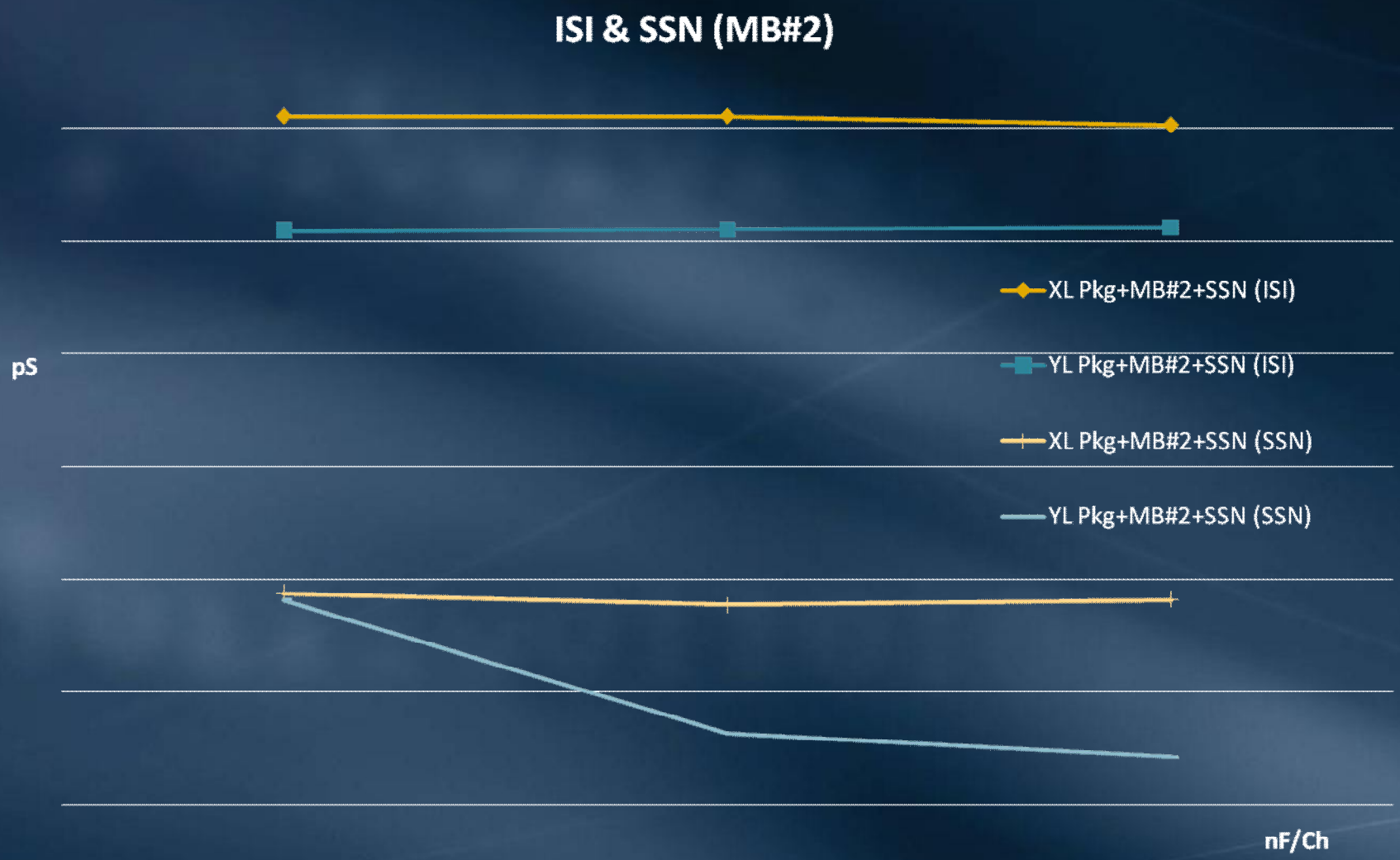
DDR Application: Full TD Sim.

<MB #2>
Pkg #2 @ XnF/Ch – Pkg #1 @ XnF/Ch ~ 10p
Pkg #2 @ YnF/Ch – Pkg #1 @ YnF/Ch ~ 0p

No Freebie! – Want to go to Pkg #1? Add more Cdie!



Noise (MB #2)



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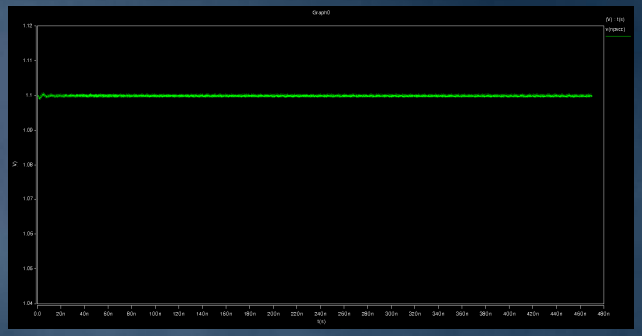
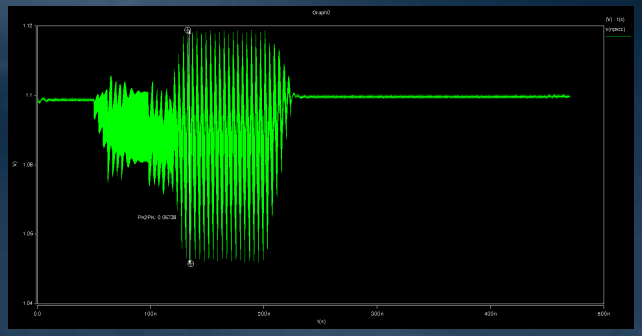
Differential Signaling Application

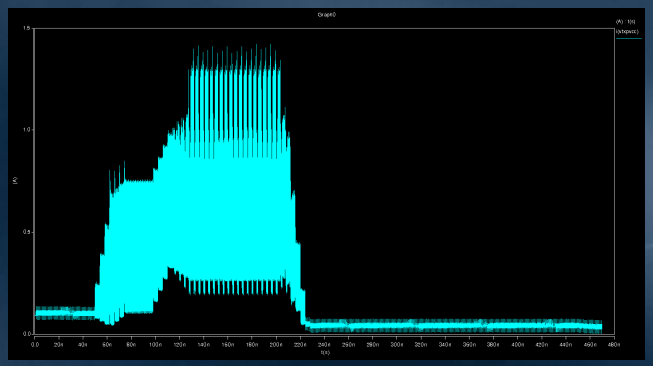
- First evaluate the noise in the PD network
- Reduce the noise by changing the Z11
- Architectural controls for power on/ off
- Perform SI/PI co-simulations for jitter impact

No SSN



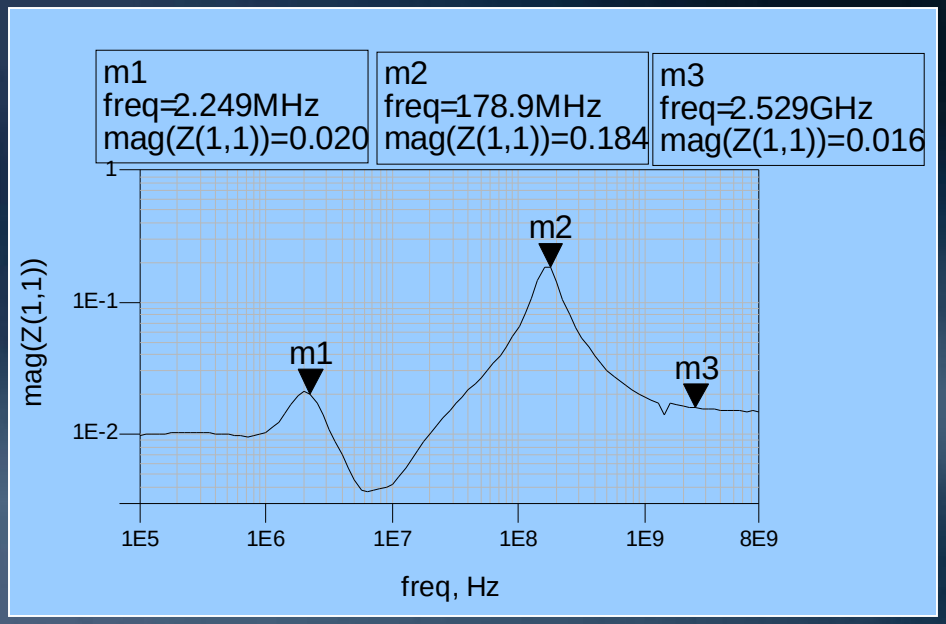
SSN: 16TX & 16 RX

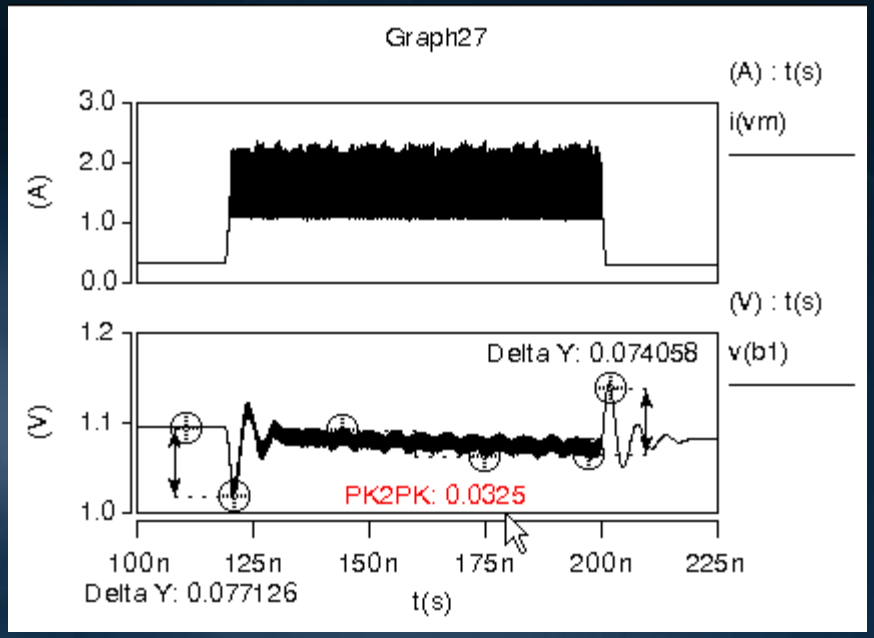




- PD p2p: 1.2mV vs 67mV

Differential FD and TD

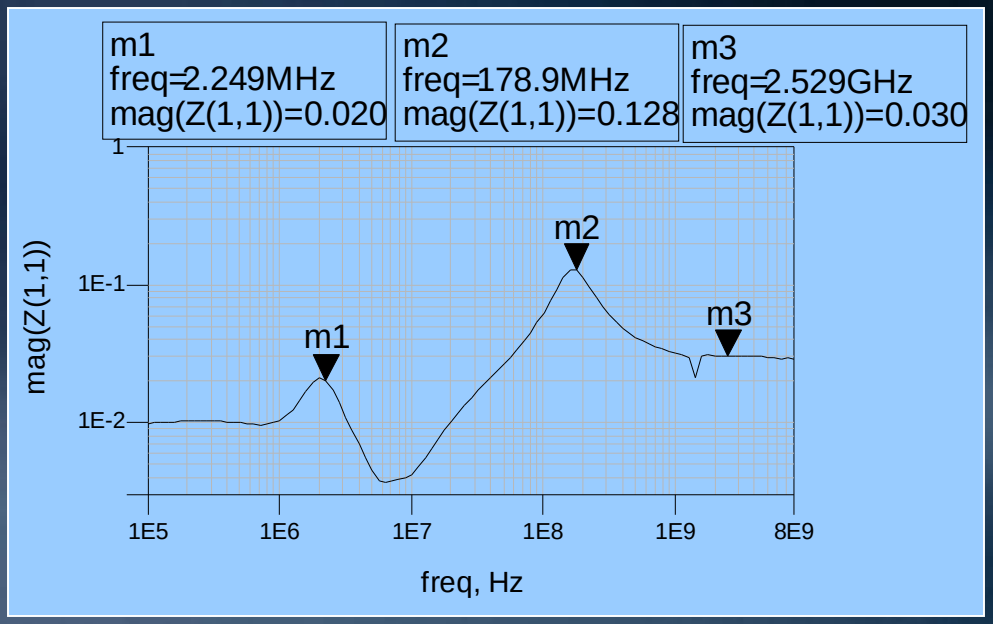


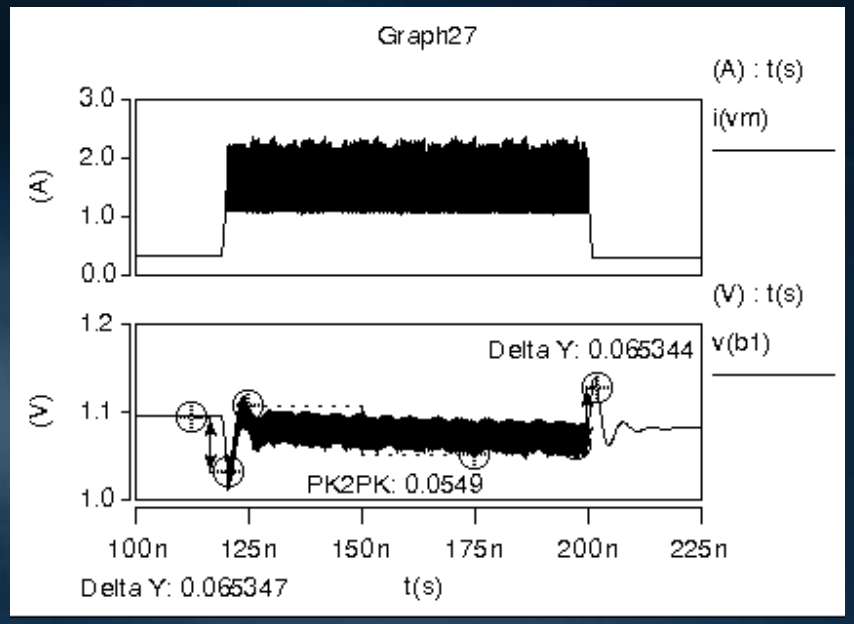


- For this Z11 Cdie = C1, Rdie = R1
- Fr = 0.184 Ω at 179 MHz
- Z=16 mΩ at 2.5 GHz

- Power-on droop (120 nS) and power-off bounce(200 nS) depends on Resonance
  - Ringing → Z11 at 179 MHz
  - Amplitude 77mV → Z11 of 0.184 m Ω
- Steady state 32 mV corresponds to 16 mΩ Z11@2.5 GHz

Effect of higher Rdie

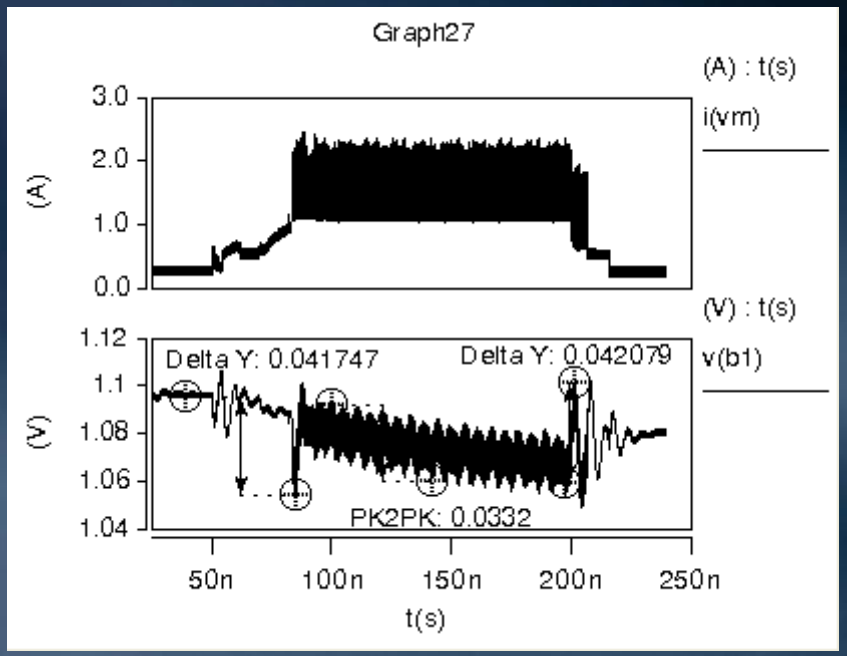


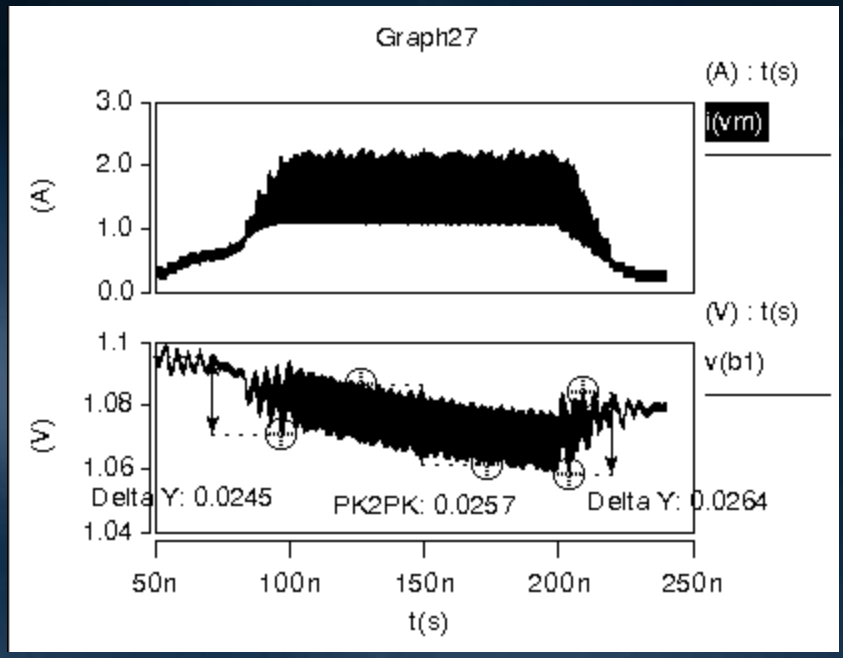


- For this Z11 Cdie = C1, Rdie = R2
- Z11@Fr = reduced from 0.184 Ω to 0.128 Ω
- Z11@2.5 GHz=Increased 16 mΩ to 30 mΩ

- Droop/ Bounce reduced to 65 mV
  - Steady state increased to 54 mV

Architectural Controls



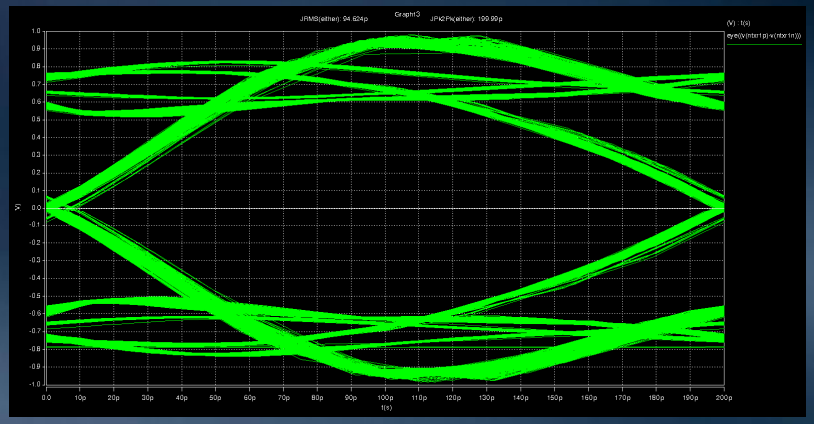


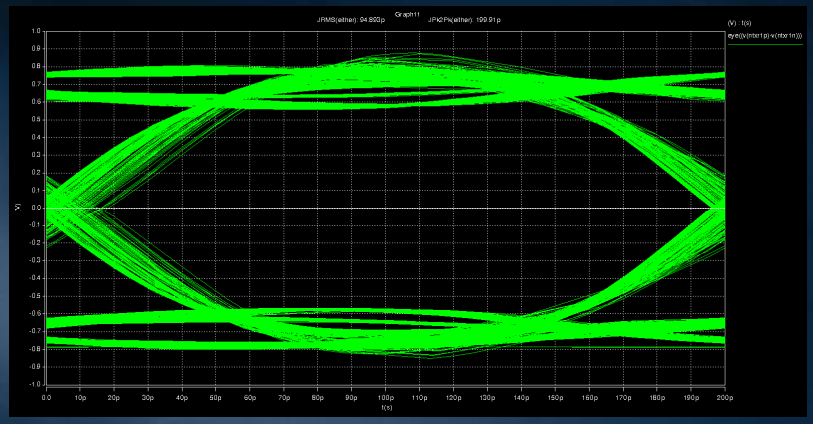
- Architectural controls: Control #1 reduces the initial droop
- More architectural controls Control #2 reduces noise further

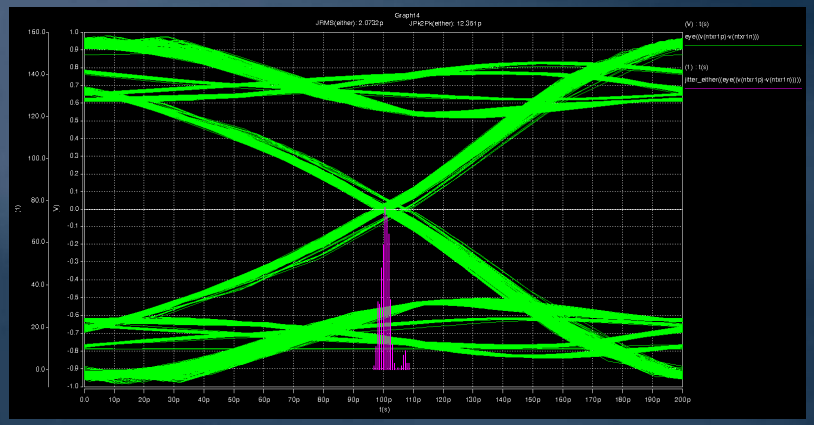
Differential Signaling Application

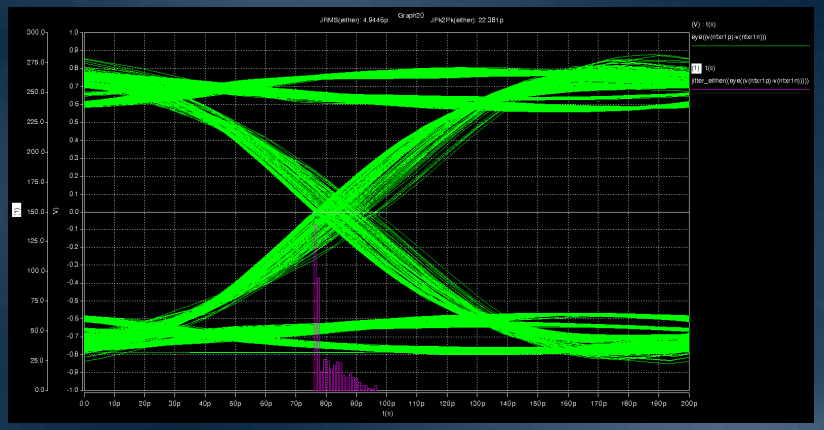
No additional SSN (Icc(t))

16TX+16RX+Clk









- Jitter: ~+10pS with Icc(t)

Conclusions

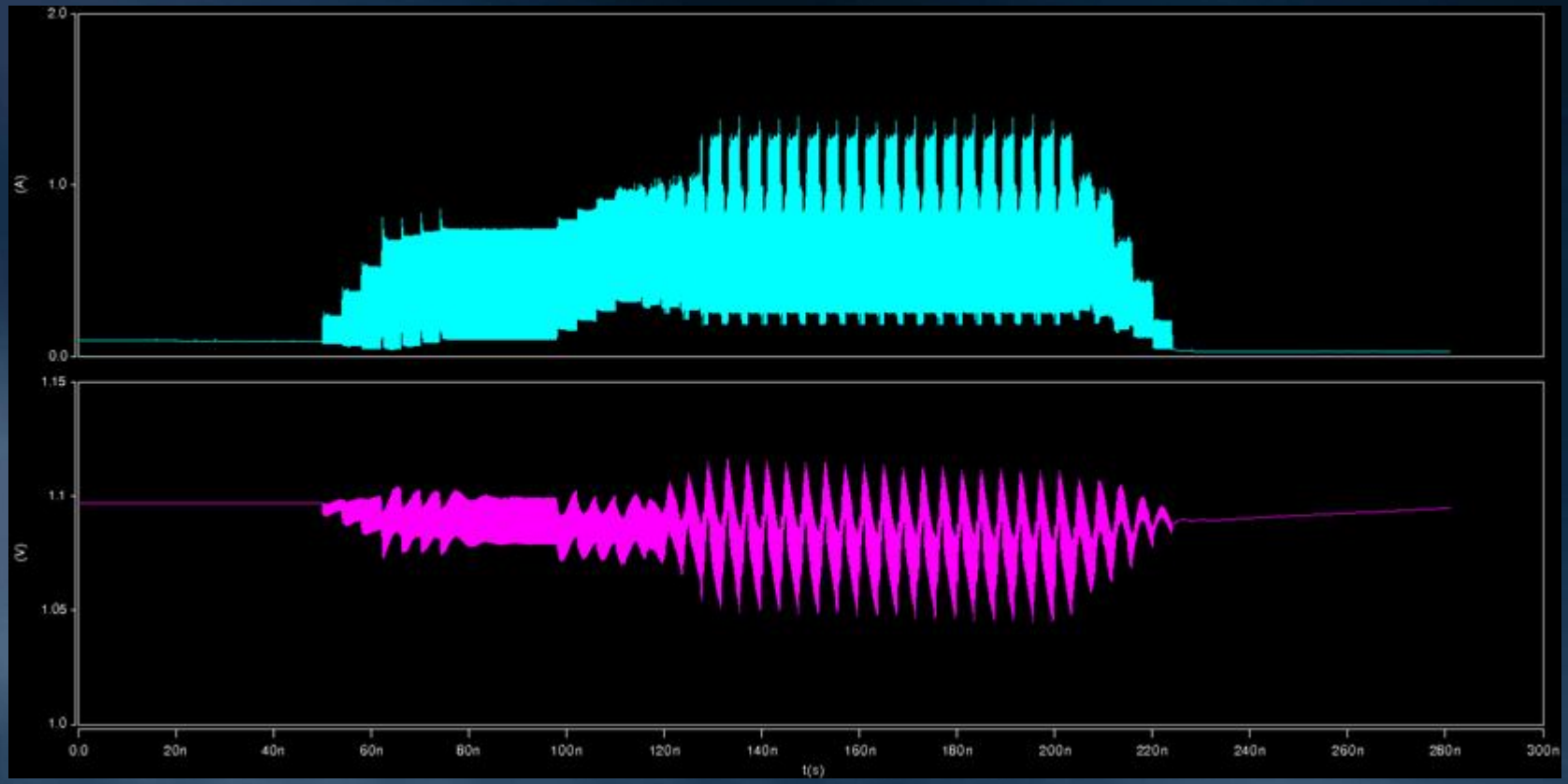
- SI / PI co-analysis methodology established to determine the performance impact due to Power Integrity
  - Quality S parameters and accurate buffer model that predicts the PD behavior is required.
- Single ended and differential system (die, pkg, board) modeled and full time simulations performed
- Timing variations due to different elements are studied.
- SI/ PI analysis is increasingly becoming important for system optimization

References

- [1] http://books.google.com/books?id=AB2DHvhSHpsC&pg=PA594&lpg=PA594&dq=peak+distortion+analysis&source=bl&ots=uhp7nY4o3v&sig=1Tn5YDSJ1gmej488rzyuu1o5L9Y&hl=en&ei=8V9pSs_0BITEsQPhx4yWBQ&sa=X&oi=book_result&ct=result&resnum=6
- [2] http://download.intel.com/education/highered/signal/ELCT865/Class2_15_16_Peak_Distortion_Analysis.ppt

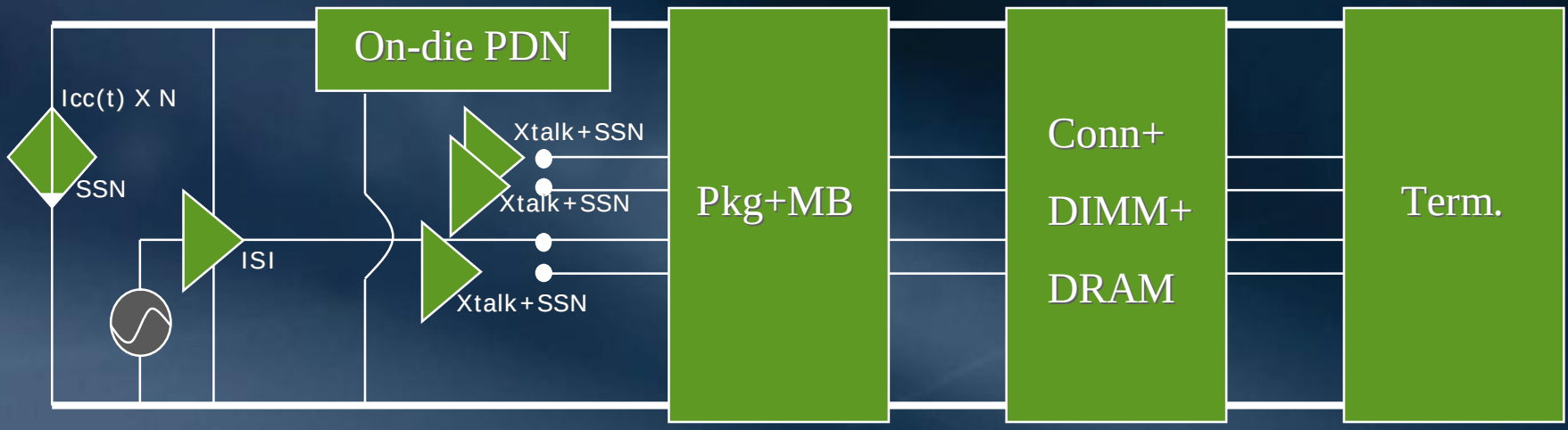
Backup

16 TX Icc(t) + 16 RX Icc(t) + TX buffers



72 mV of peak-to-peak with 240 MHz resonance coming from Icc(t)

SI-PI Co-simulation Overview



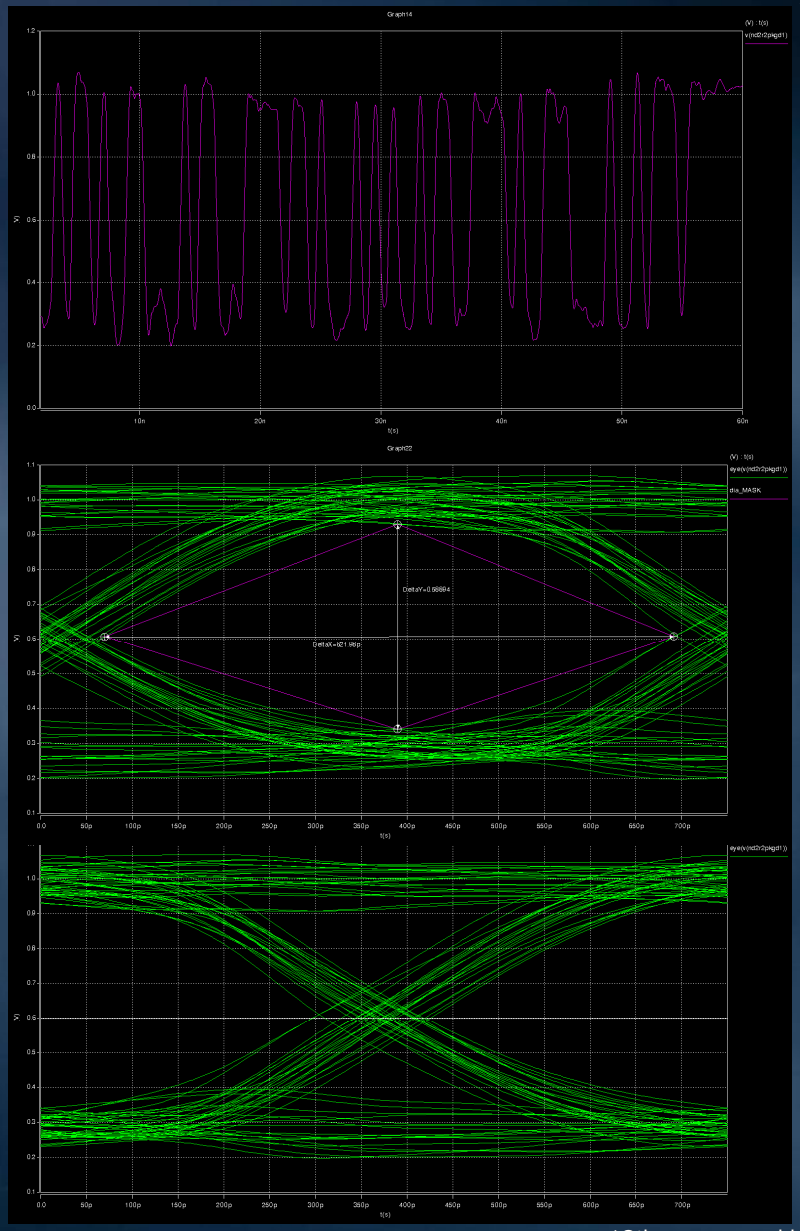
<Model Preparation>

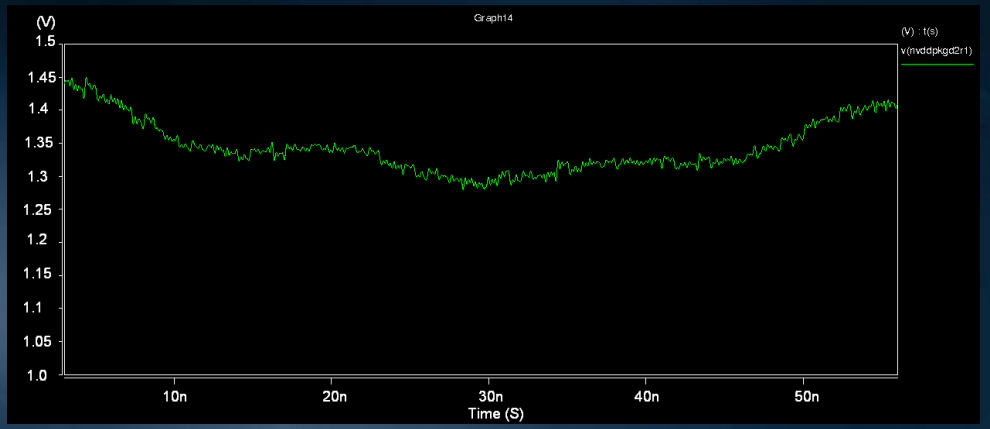
1. Buffer Model
   - Can it accommodate PD variation?
2. On-die PDN Model
   - Can it handle SSN?
3. 2~3D Model: Package, PCB, Connectors
   - Can it capture PD to Signal coupling?
   - Can it capture EM impact?

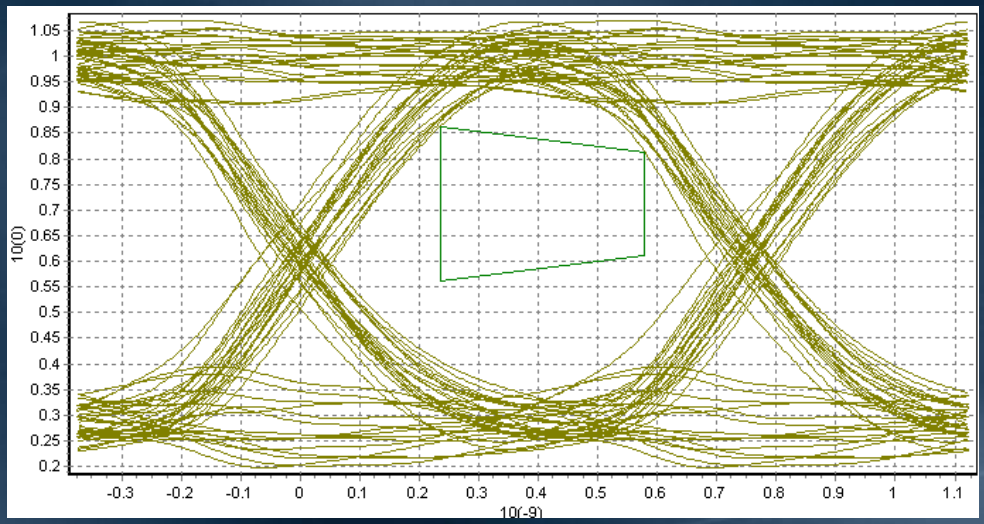
Case: MB #1

- Single Ended Signaling
- DDR Channel Performance
  - Package Impact
  - Cdie Impact
  - MB Impact
- SI-PI Sim Result: Decision making aid

Y-Layer Pkg, MB#1, XnF/Ch

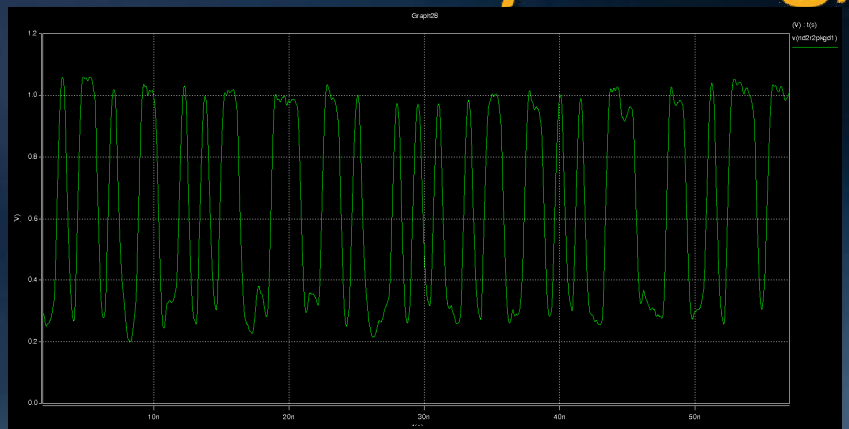


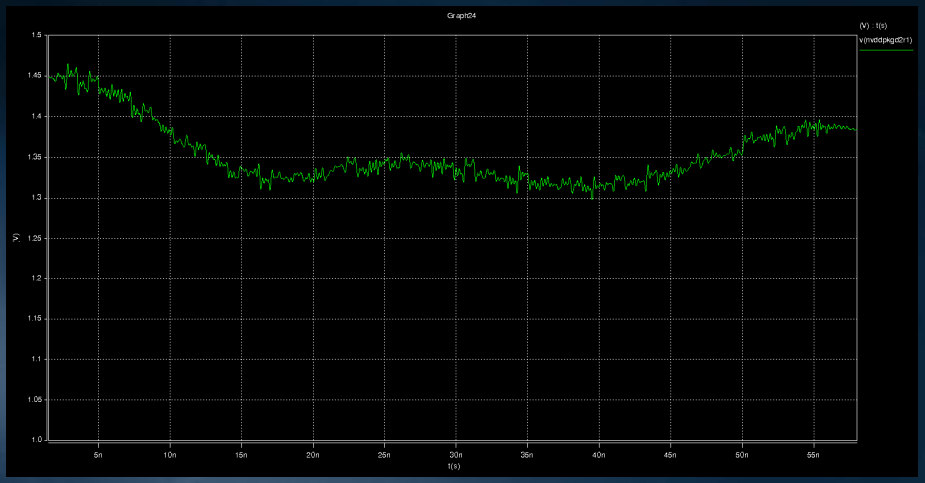


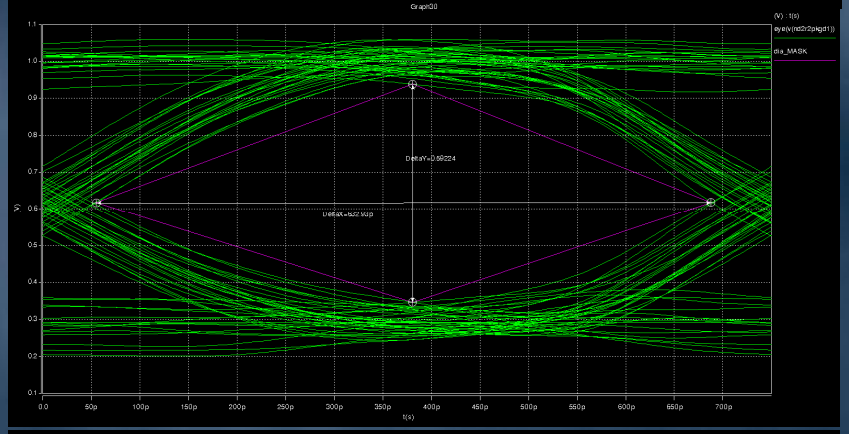


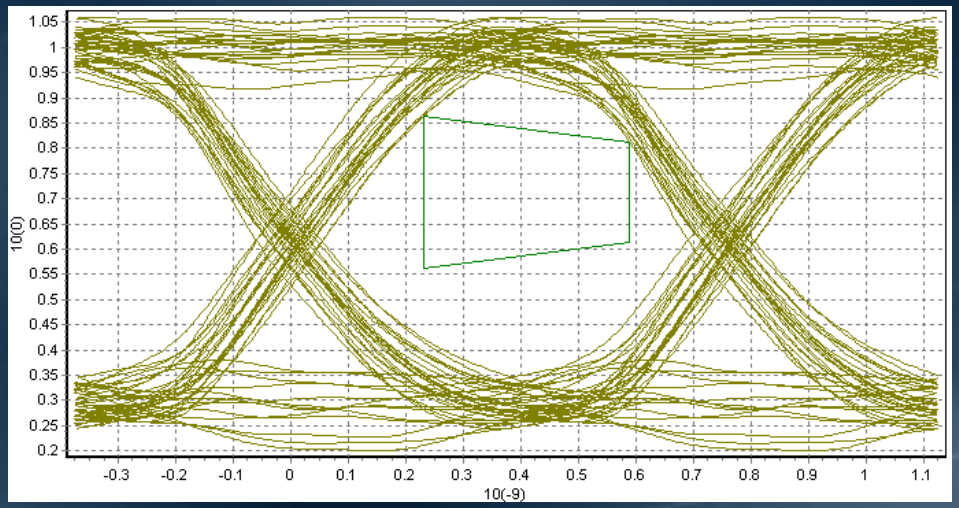
*Other names and brands may be claimed as the property of others

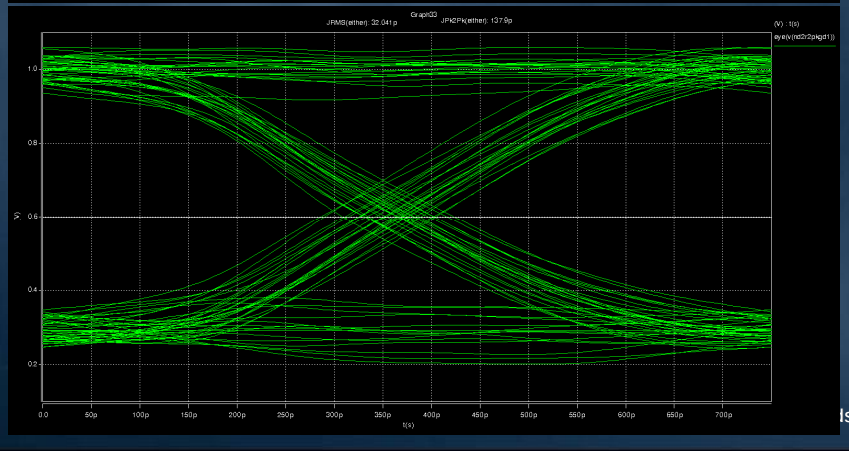
X-Layer Pkg, MB#1, YnF/Ch







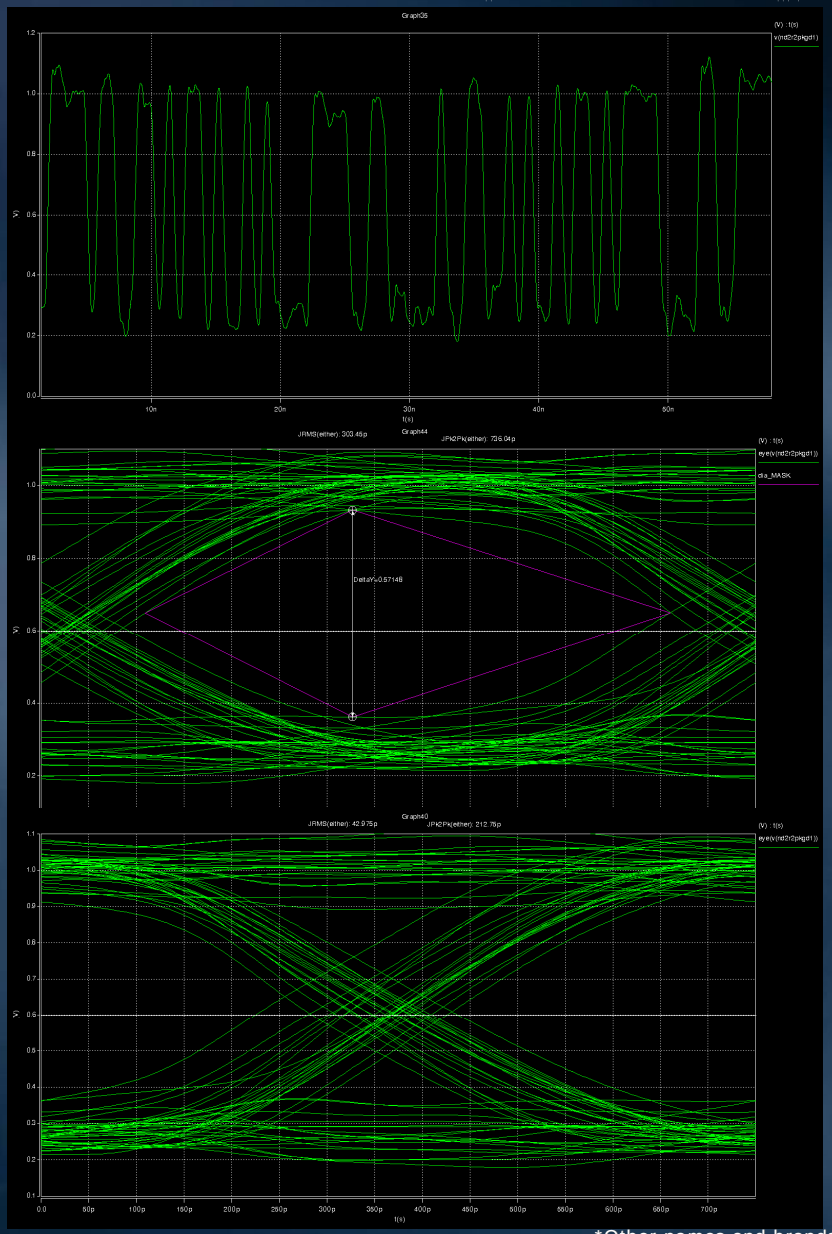


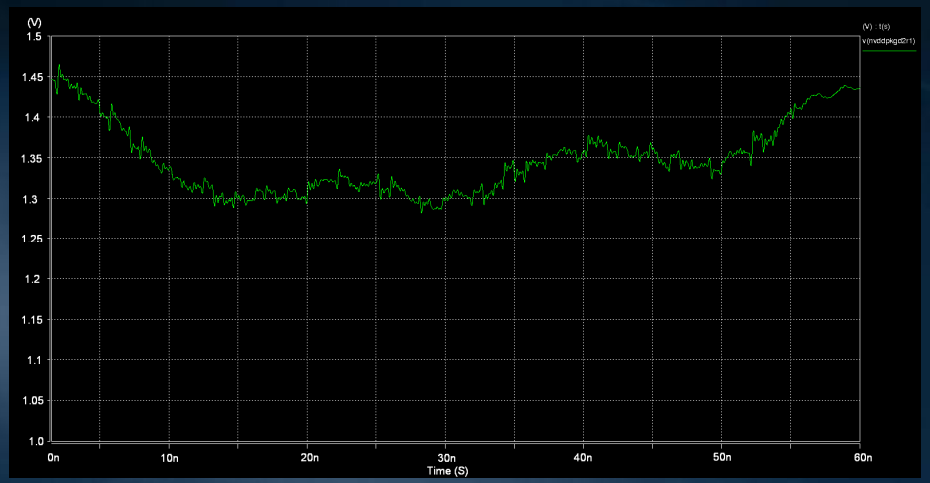


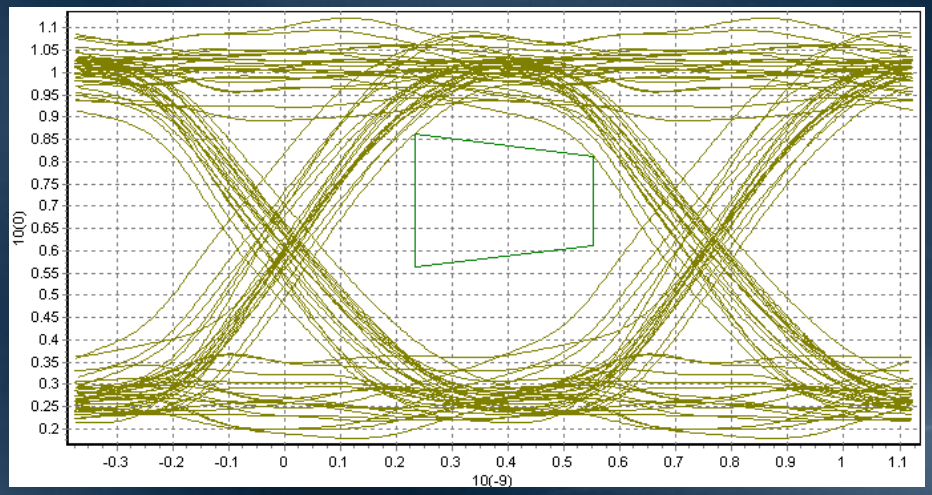
Case: MB #2

- Single Ended Signaling
- DDR Channel Performance
  - Package Impact
  - Cdie Impact
  - MB Impact
- SI-PI Sim Result: Decision making aid

Y-Layer Pkg, MB#2, XnF/Ch

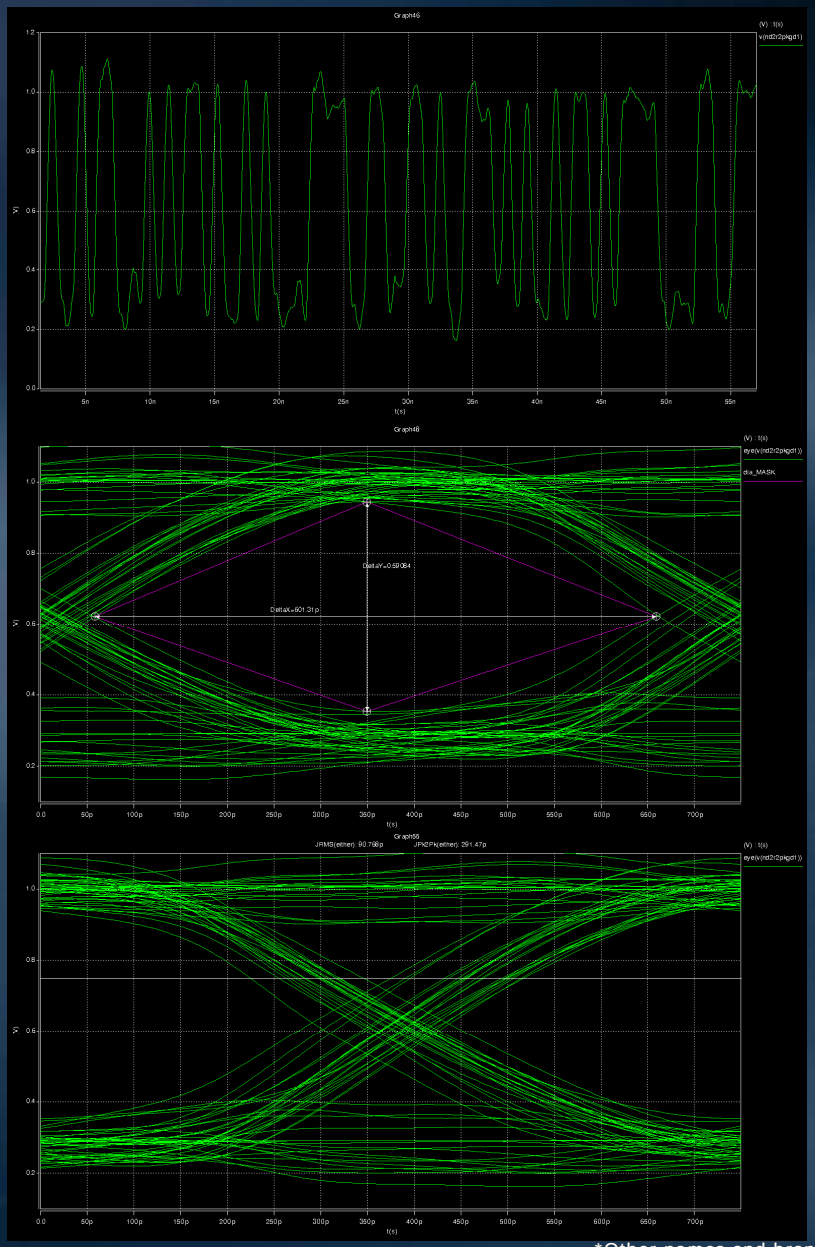


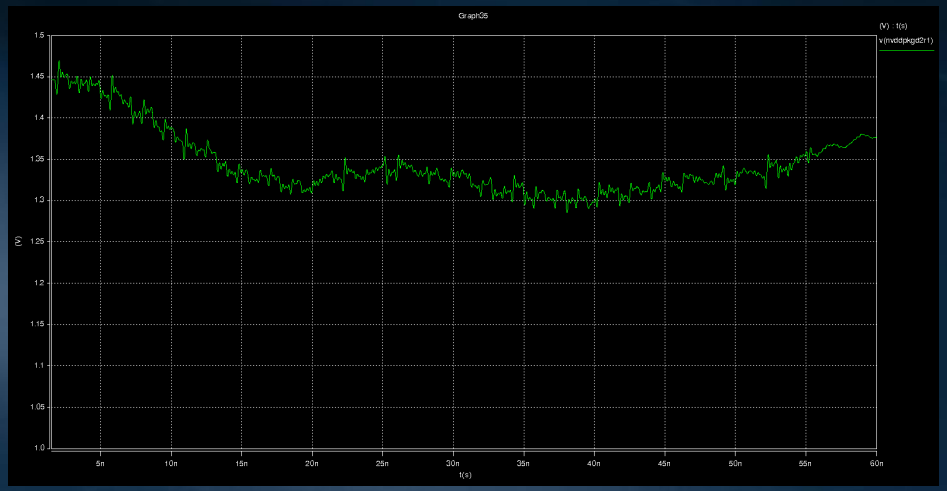


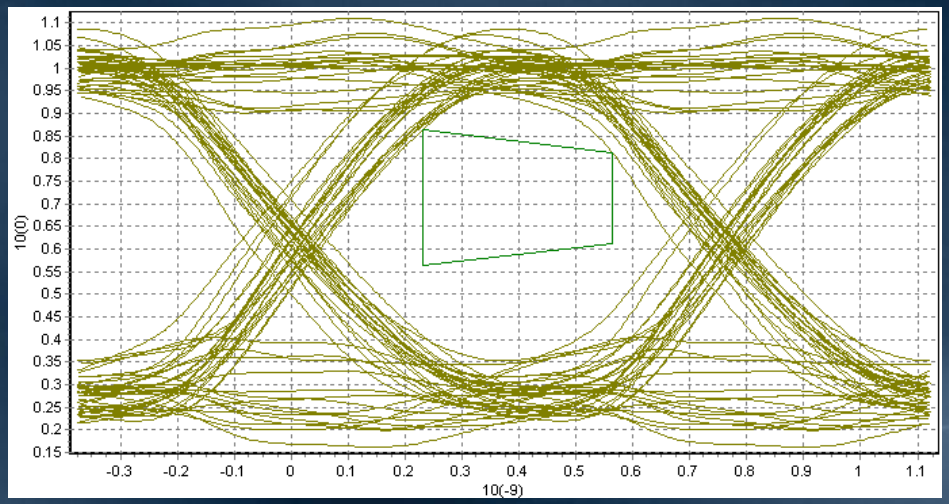


*Other names and brands may be claimed as the property of others

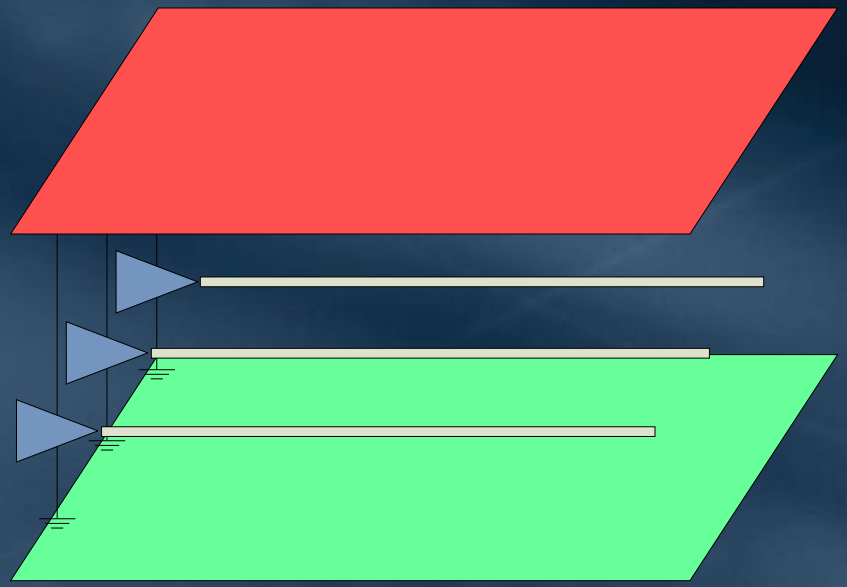
X-Layer Pkg, MB#2, YnF/Ch







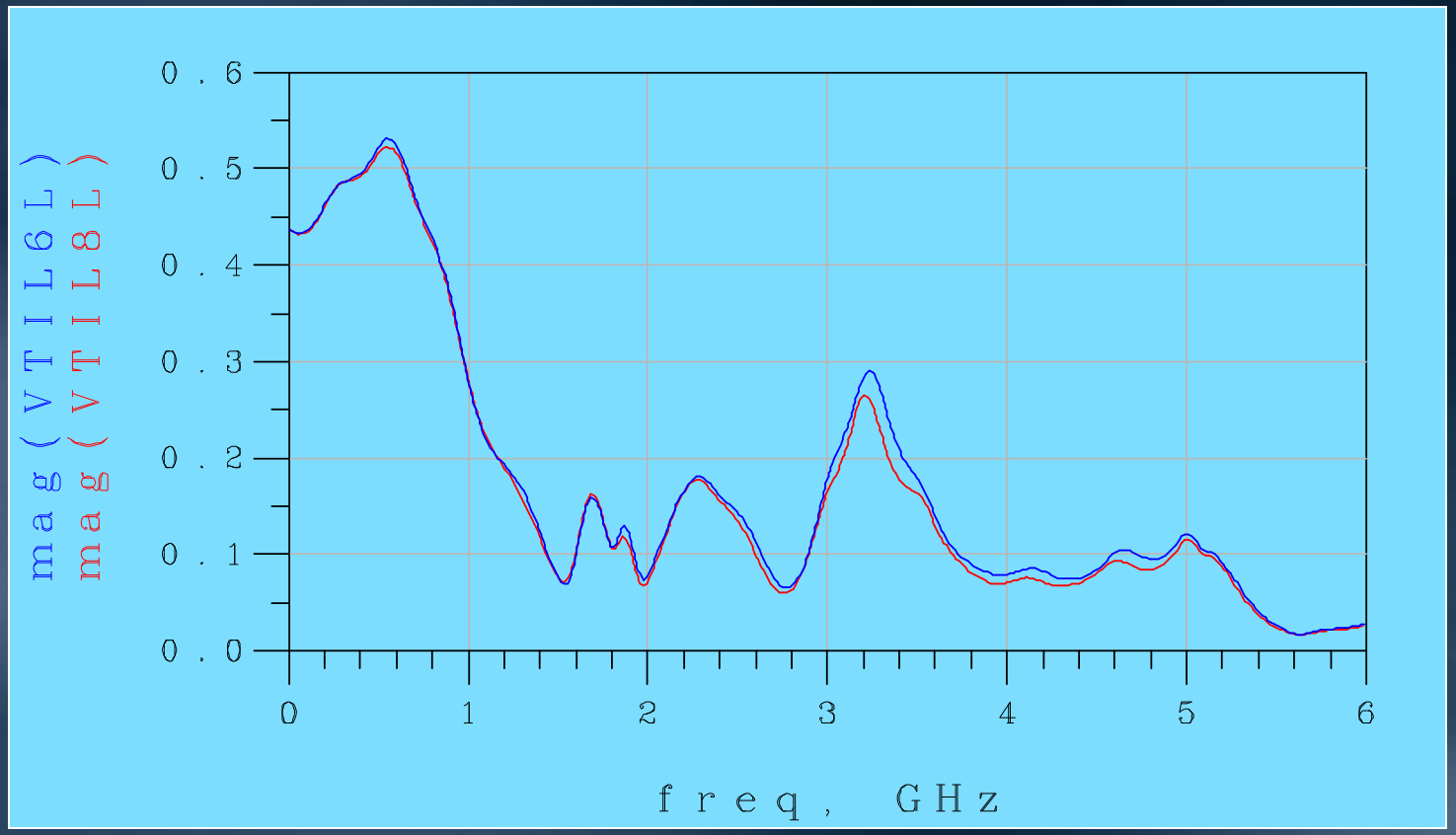
ISI, Xtalk, SSN



SI-PI Co-sim, Co-analysis: Why?

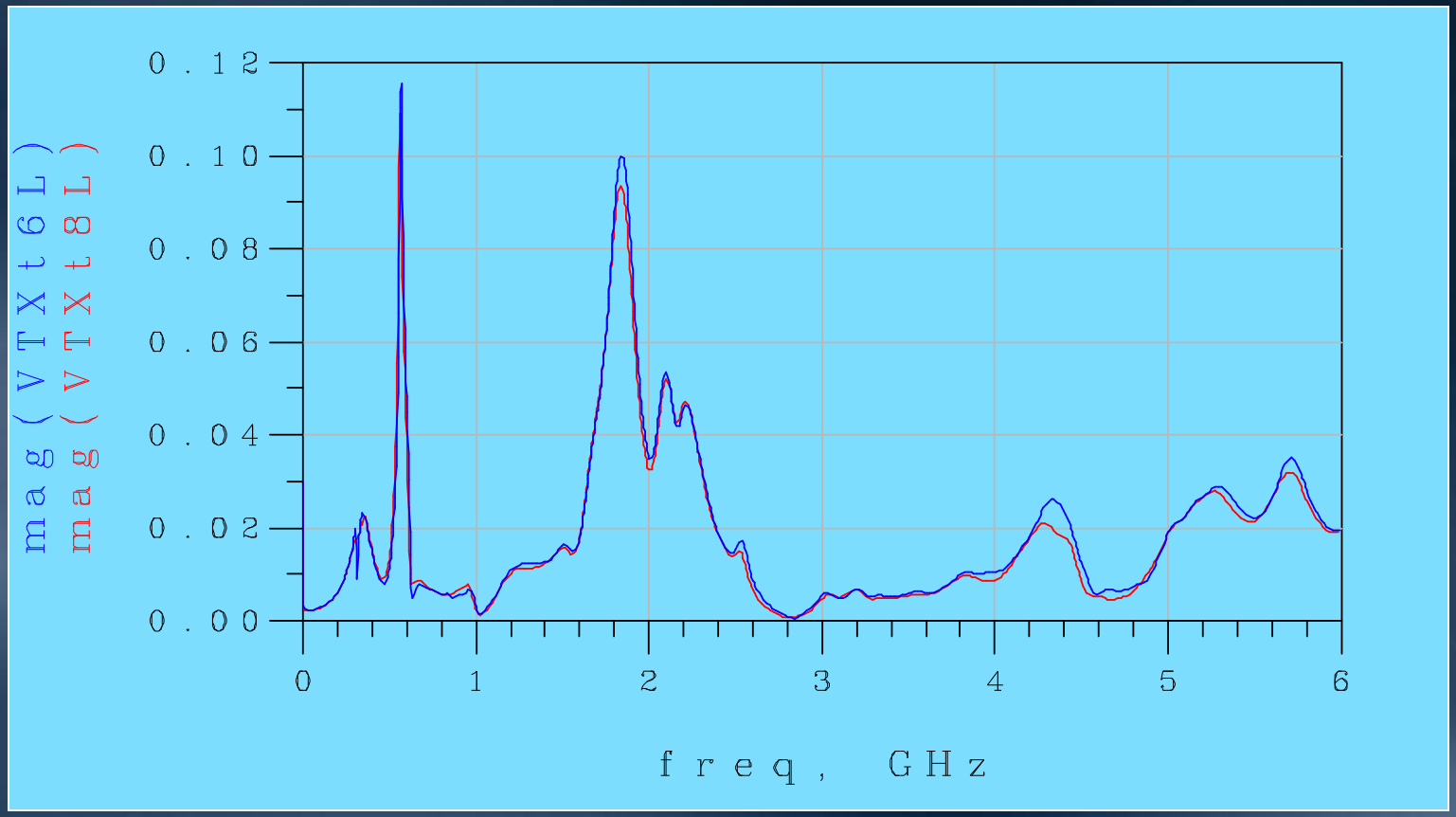
Low power, Low cost, Higher freq.

Voltage Transfer/Gain for ISI node



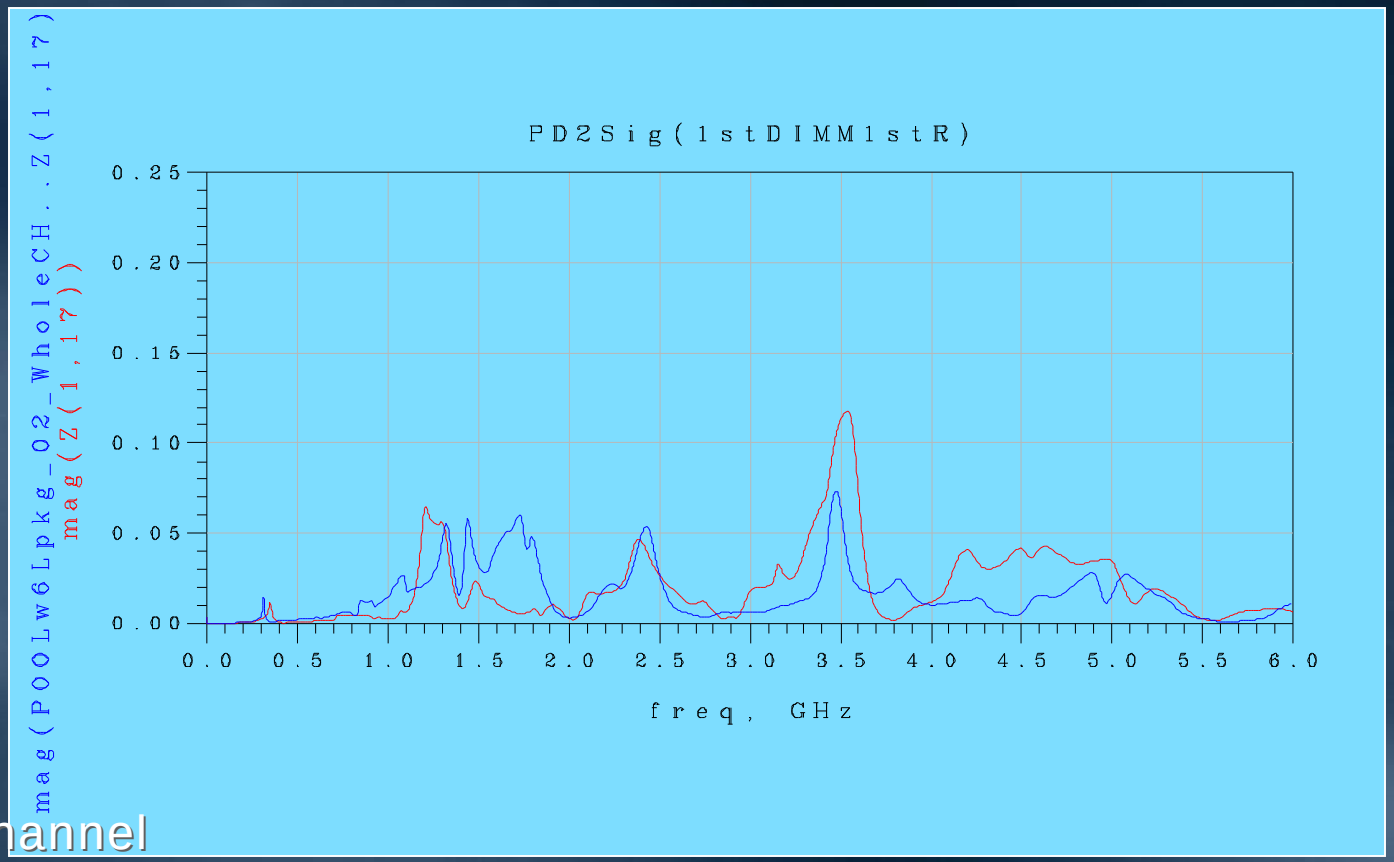
Whole Channel

Voltage Transfer/Gain for Xtalk Node



Whole Channel

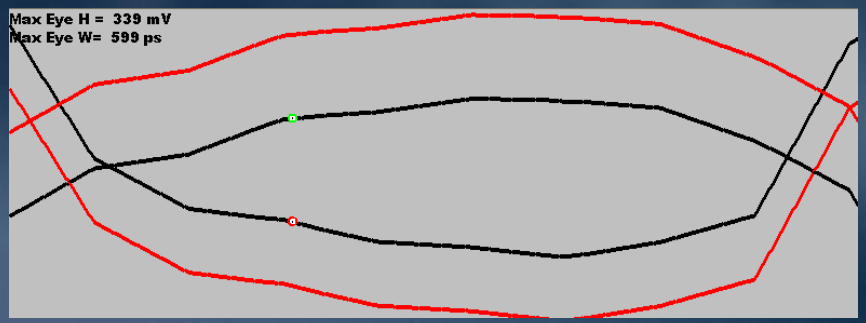
PD2Sig Coupling - Z



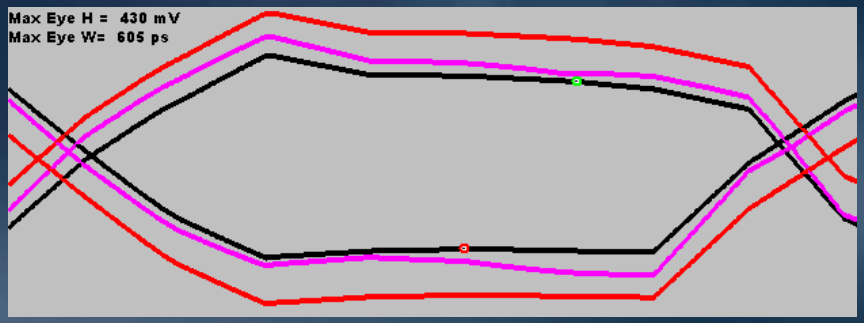
Whole Channel

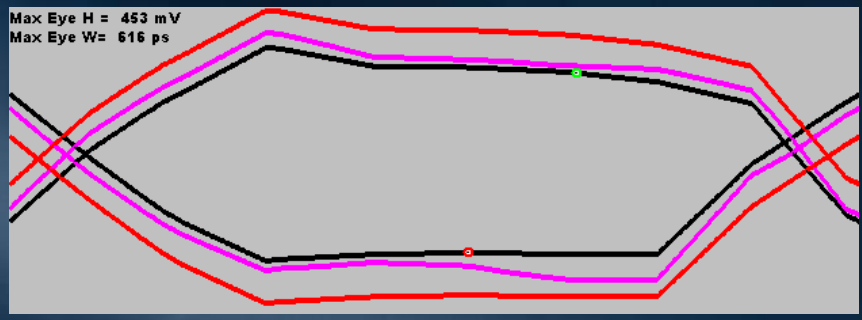
PD2Sig Coupling Mechanism: Via, transition <=Major

PDA* WC eye EX

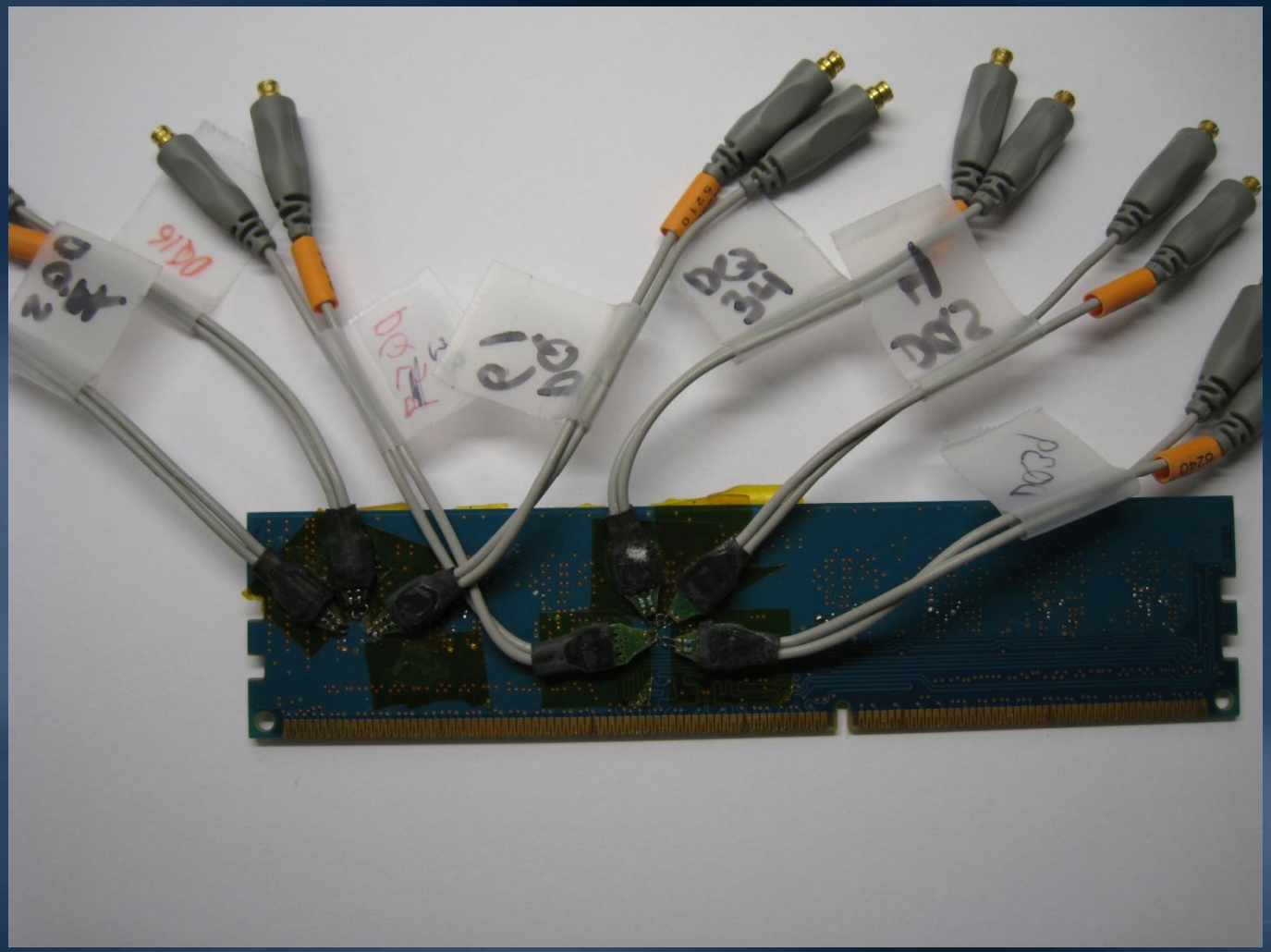


PDA* WC Eye Ex

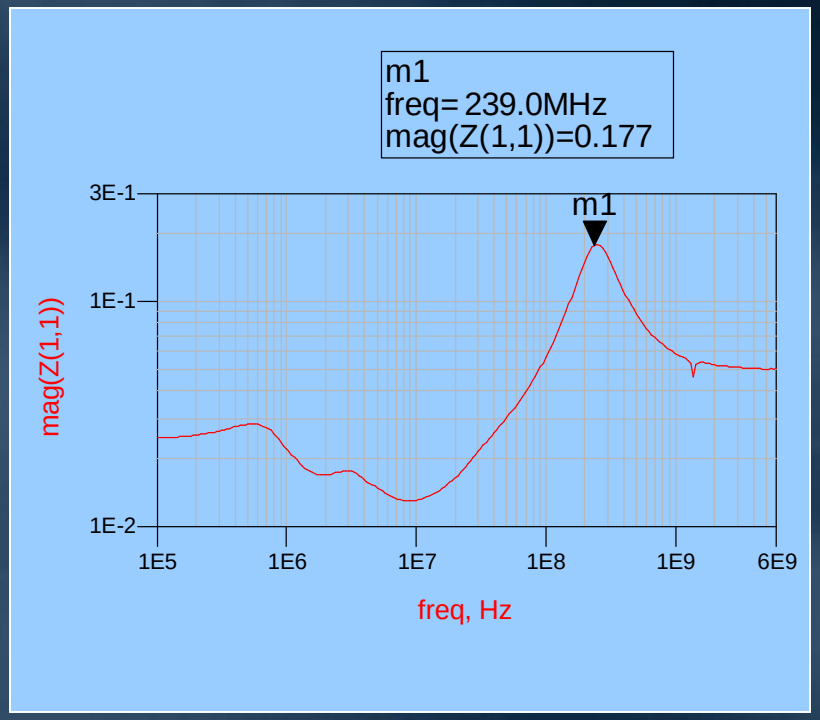




Measurement Setup

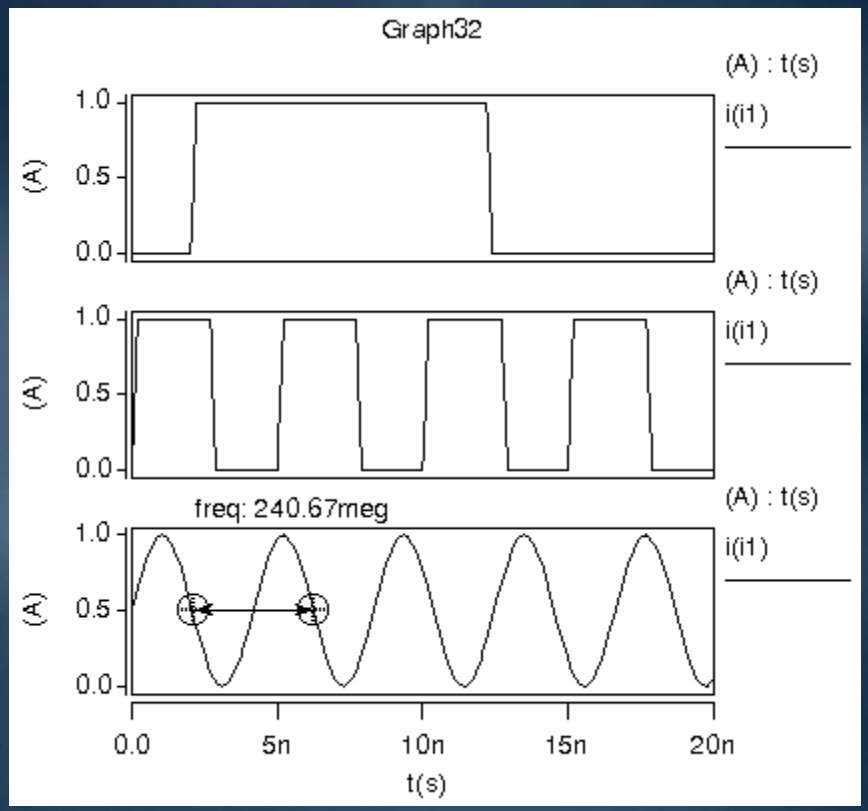


Frequency Domain Response PDN

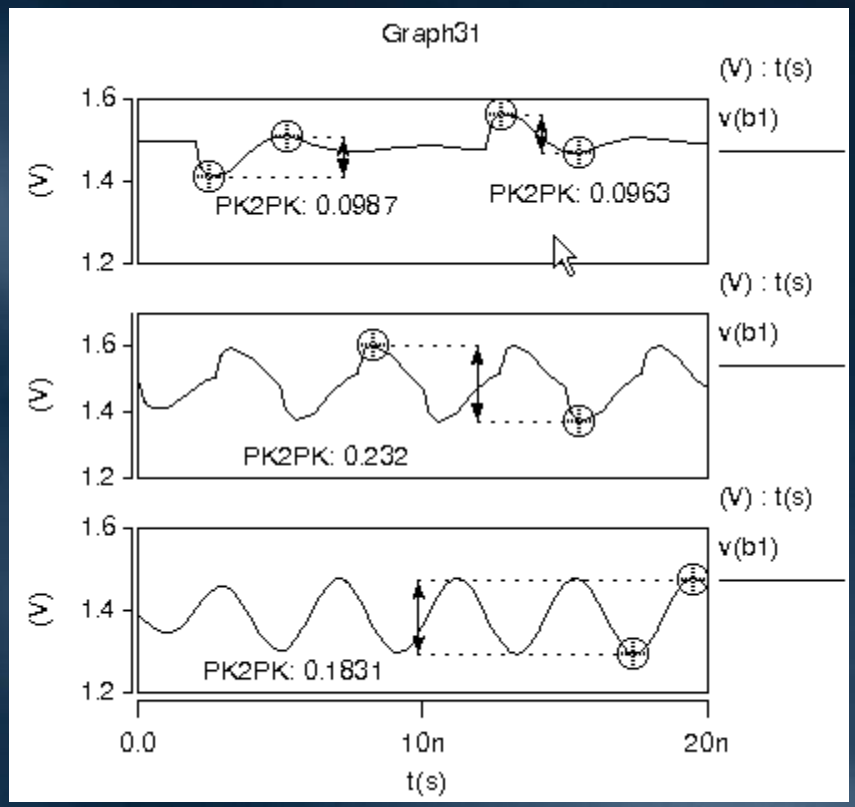


Time Domain Response

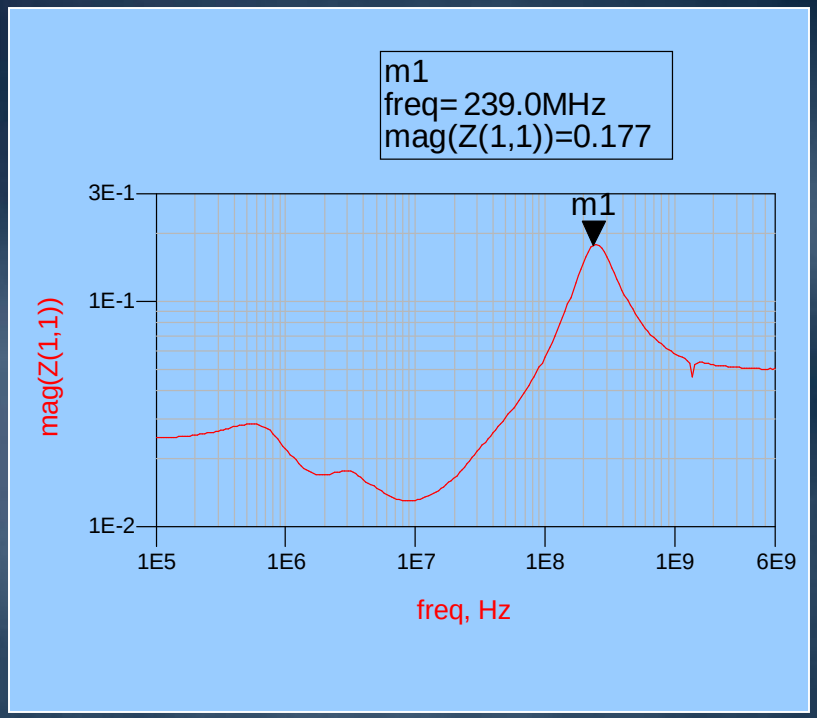
Current

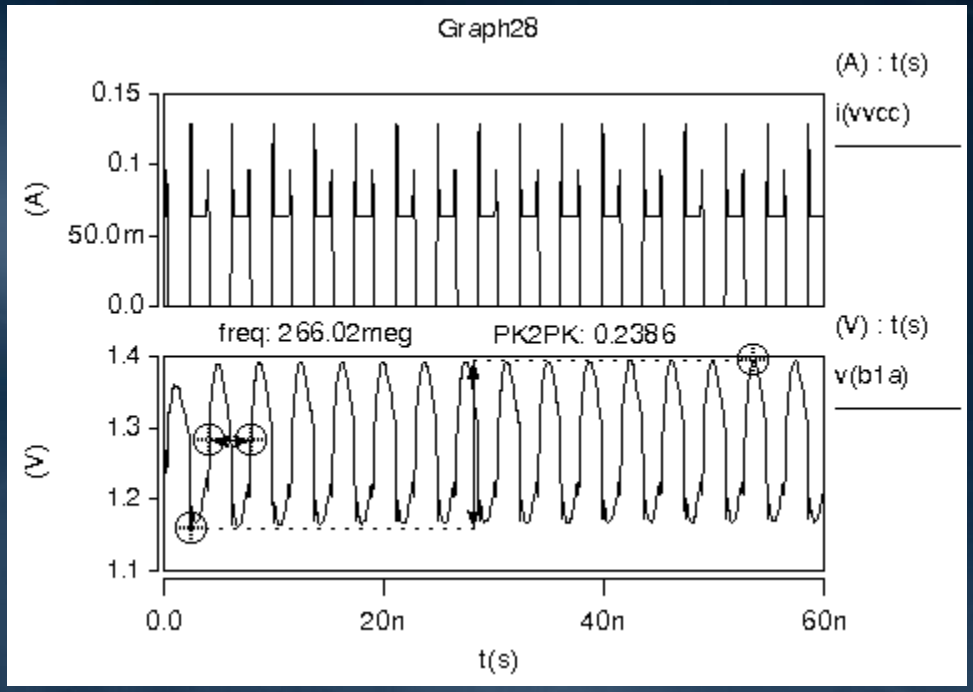


Noise



Single Ended System





Inter-domain Transfer Function Ex