

Buffers for Advanced SPICE to IBIS Testing

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IBIS Summit Meeting
Design Automation Conference 2006
San Francisco, California
July 25, 2006



Configurable CMOS & ECL Buffers

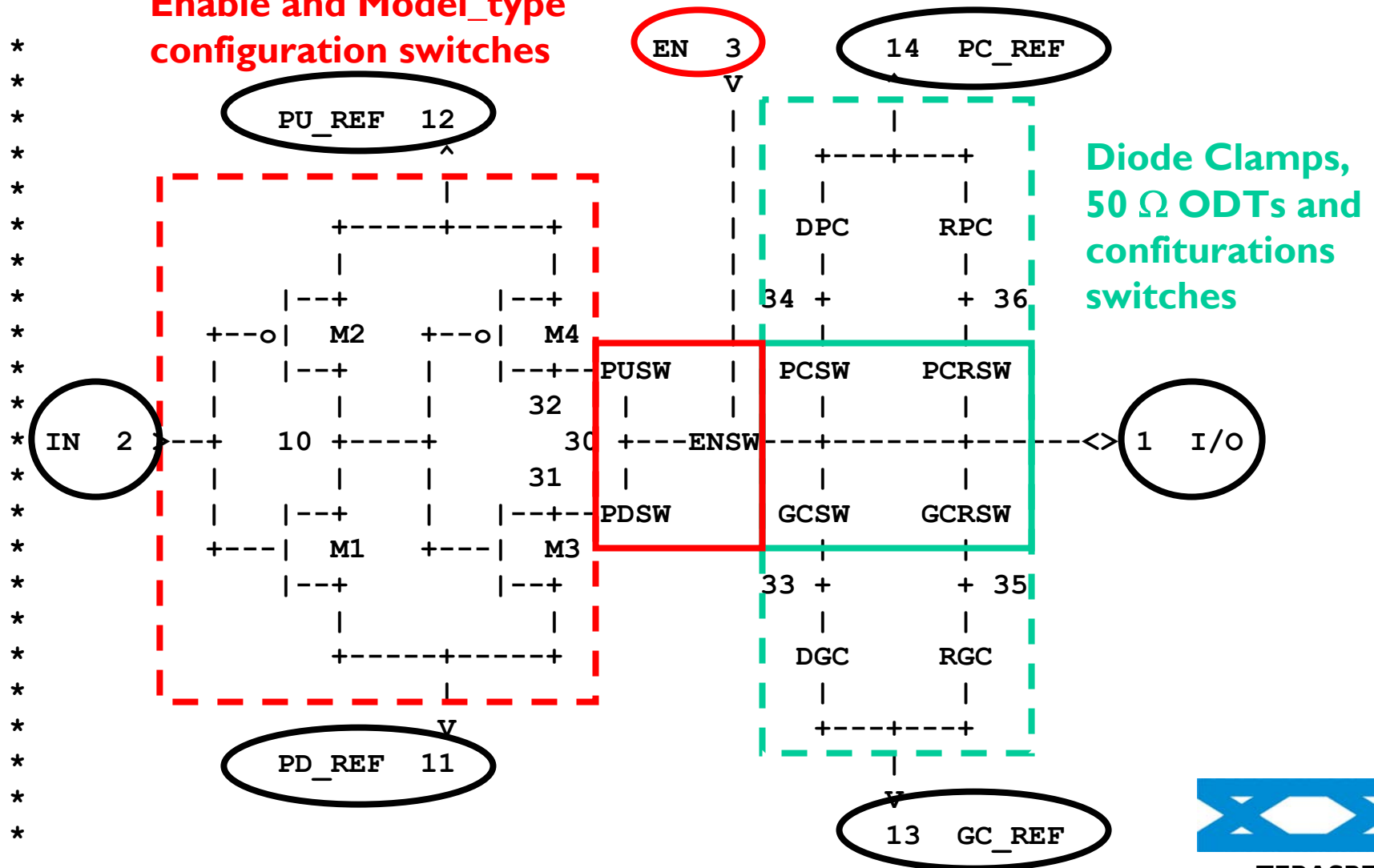
- Two buffers for all Model_types, voltages, clamps and on-die terminators ($\overline{\text{ODT}}$ s)
- Berkeley SPICE to support all SPICEs
 - Level 2 CMOS, standard bipolar ECL & simple diodes
 - Numerical nodes
 - Syntax-neutral multiplier switched conductance
 - GPDSW 30 31 POLY(2) (30,31) (21,0) 0 0 0 0 1000
 - RPDSW 30 31 IG
 - Open: $R = 1 \text{ G}\Omega$
 - Closed: $G = 1000 \text{ S}$ ($0.001 \text{ }\Omega$)
 - Externally set 0 and 1 voltage assignments
 - Could be parameterized
- Multiple cases through s2ibis and scripts



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CMOS Buffer

Enable and Model_type
configuration switches



CMOS Configuration Controls

.SUBCKT CMOSTEST

* ON-OFF CONFIGURATION SWITCHES

* (1 OR ABOVE = ON, 0 = OFF)

*

* VPD 1 PULLDOWN

* VPU 1 PULLUP

Model_type plus Enable Control

* VGC 1 GND CLAMP

* VPC 1 POWER CLAMP

* VGCR 0 INTERNAL GND CLAMP RESISTOR (50 ohm)

* VPCR 0 INTERNAL POWER CLAMP RESISTOR (50 ohm)

**Diode Clamps
and 50 Ω ODTs**

VPD	VPU	VEN = 1	VEN = 1,0	VEN = 0
1	1	Output	3-state, I/O	Input, Terminator
1	0	Open_drain	I/O_open_drain	Input, Terminator
0	1	Open_source	I/O_open_source	Input, Terminator
X	X			Input, Terminator

**Enable with
Model_type**

*

* Control

* I/O Inputs

* Voltage

* References

* Configuration

* Switches (1 = ON)

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1	2	3
I/O	IN	EN

11	12	13	14
PD	PU	GC	PC

21	22	23	24	25	26
PD	PU	GC	PC	GCR	PCR

*

**I/O, Input
and Enable**

**Voltage
Refs**

**Model_type, Clamps
and ODT Config.**



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Switches (Berkeley SPICE)

```

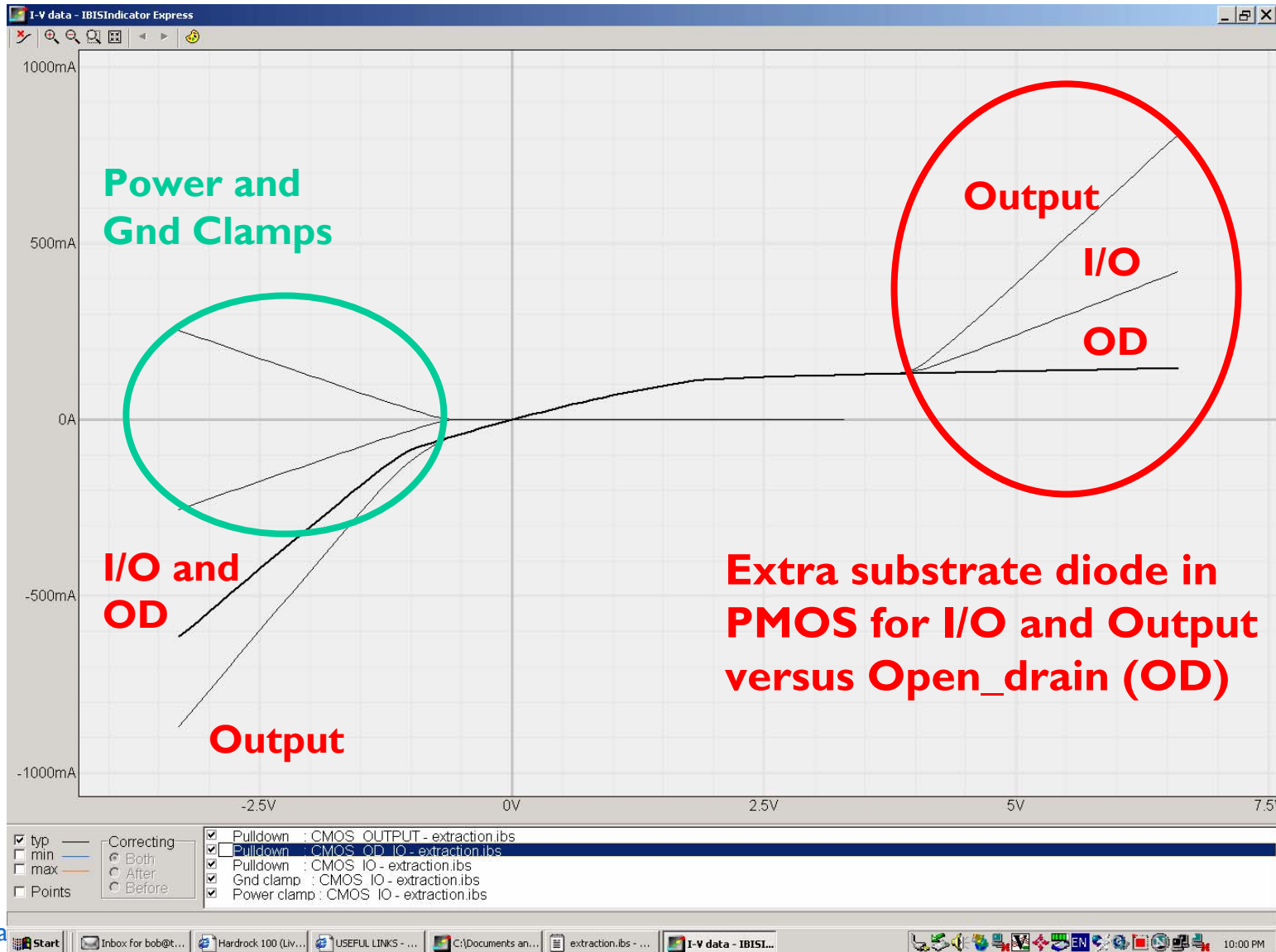
*****
*
*
*           Control      Voltage      Configuration
*           I/O         Inputs    References    Switches (1 = ON)
*           ---         -
* .SUBCKT CMOSTEST 1      2 3      11 12 13 14      21 22 23 24 25 26
*           I/O         IN EN      PD PU GC PC      PD PU GC PC GCR PCR
*
*****
* CONFIGURATION CONTROL SWITCHES---|
*
* Pulldown and Pullup
GPDSW  30  31  POLY(2) (30,31) (21,0)  0 0 0 0 1000
RPDSW  30  31  1G
GPUSW  32  30  POLY(2) (32,30) (22,0)  0 0 0 0 1000
RPUSW  32  30  1G
* Gnd Clamp and Power Clamp
GGCSW  1  33  POLY(2) (1,33) (23,0)  0 0 0 0 1000
RGCSW  1  33  1G
GPCSW  34  1  POLY(2) (34,1) (24,0)  0 0 0 0 1000
RPCSW  34  1  1G
* Gnd Clamp Resistor and Power Clamp Resistor
GGCRSW  1  35  POLY(2) (1,35) (25,0)  0 0 0 0 1000
RGCRSW  1  35  1G
GPCRSW  36  1  POLY(2) (36,1) (26,0)  0 0 0 0 1000
RPCRSW  36  1  1G
* Enable
GENSW  30  1  POLY(2) (30,1) (3,0)  0 0 0 0 1000
RENSW  30  1  1G

```

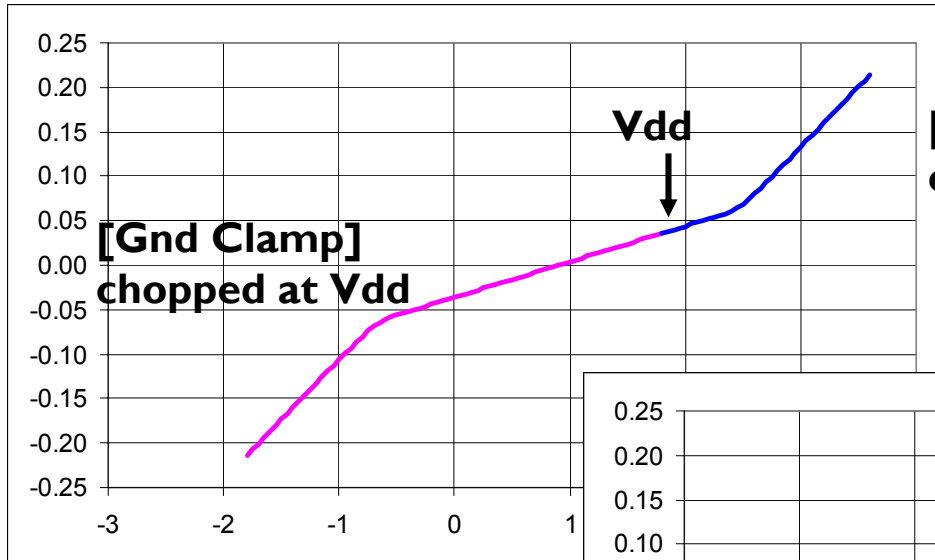


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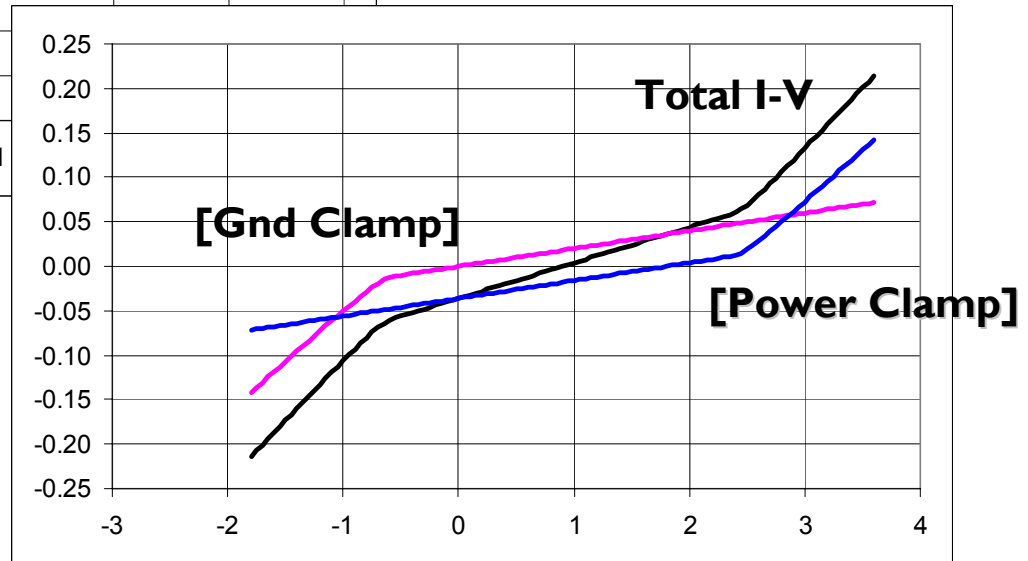
[Pulldown]s for Several Model_types



Diode and ODT – Test I-V Processing and SPICE to IBIS Methods

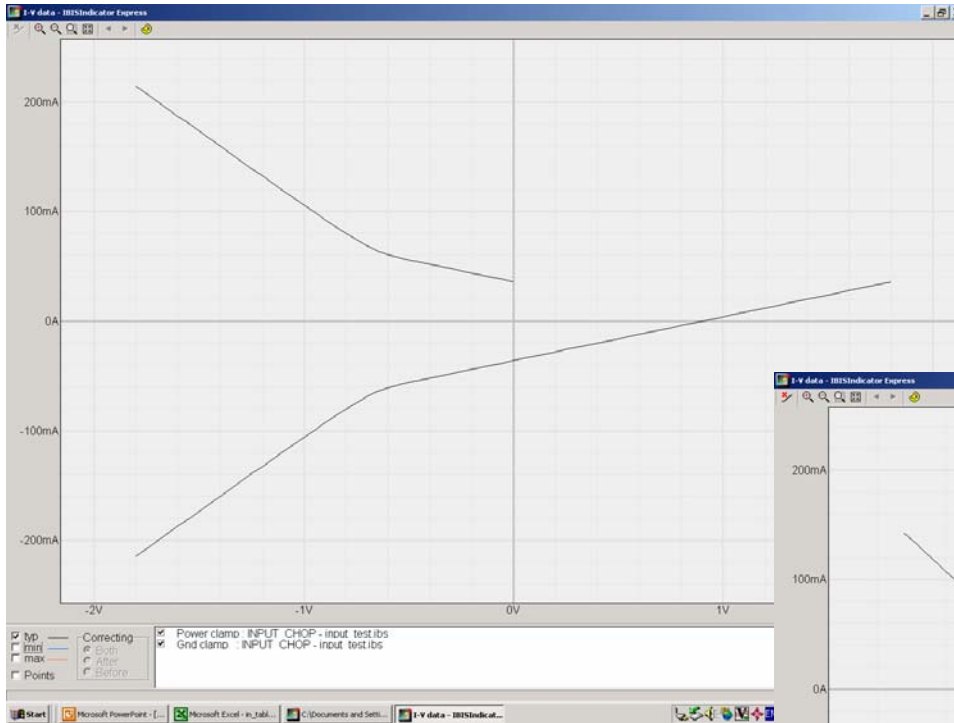


One method based on chopping the I-V tables

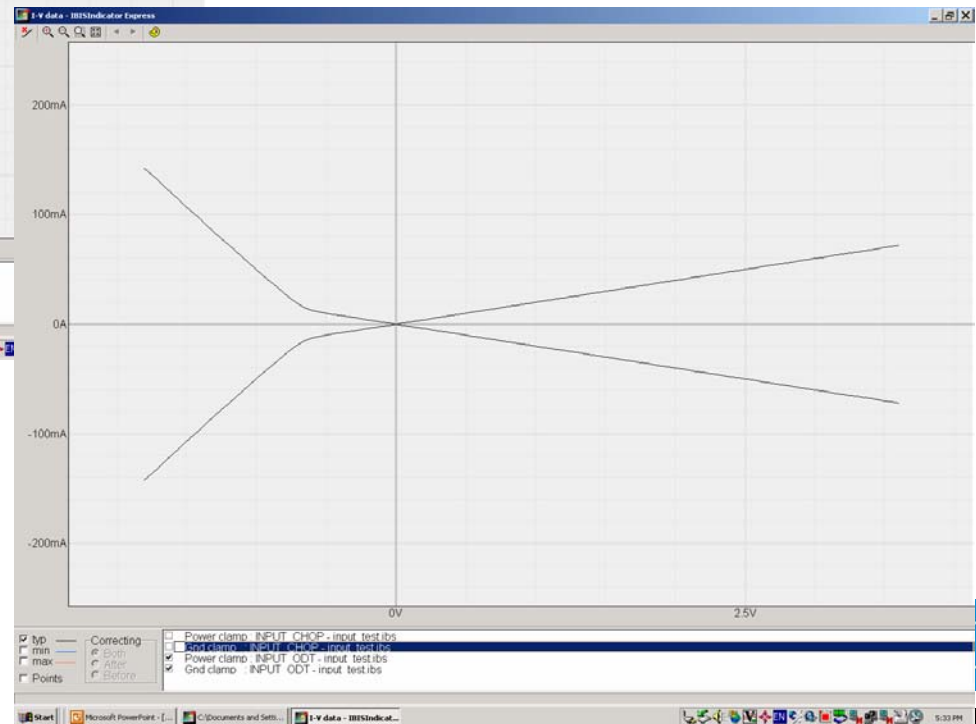


**Better tables based on “DEC”
(Deviate, Extrapolate, Calculate)**

Diode and ODT – Corresponding IBIS Model Plots

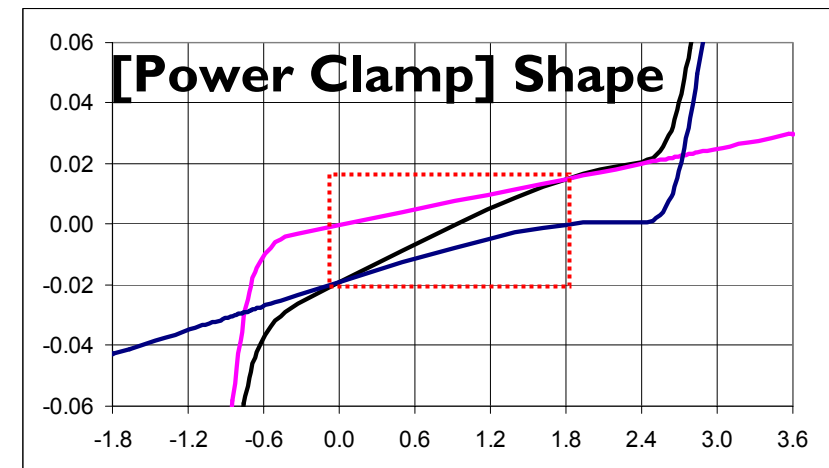
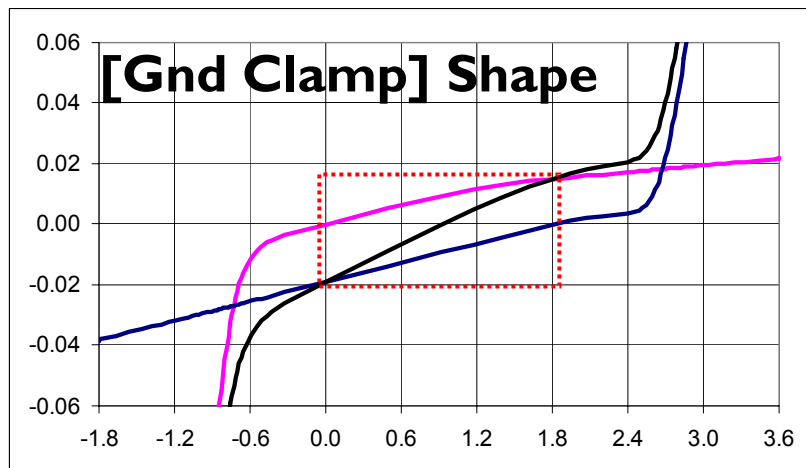
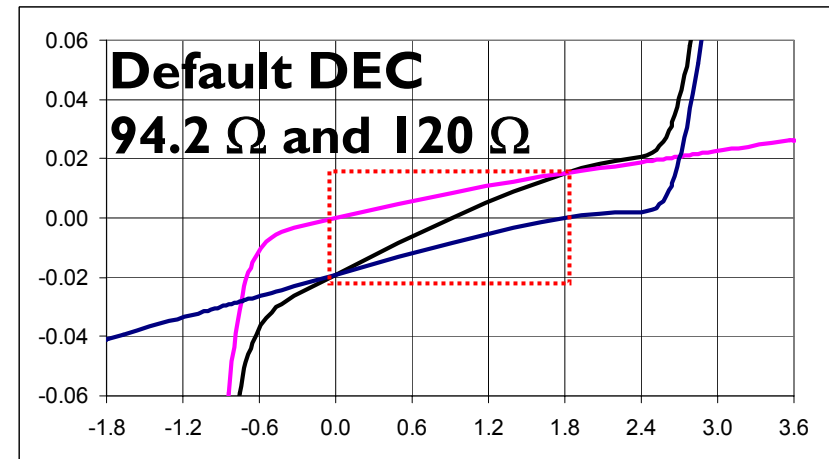
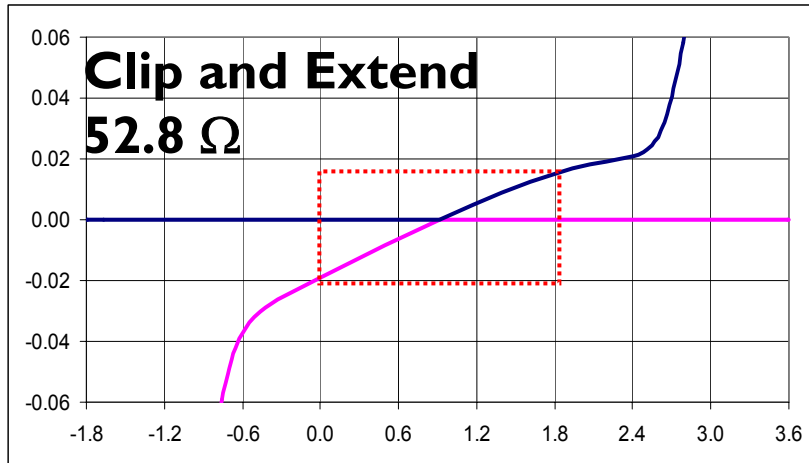


“DEC” IBIS plots show extended range

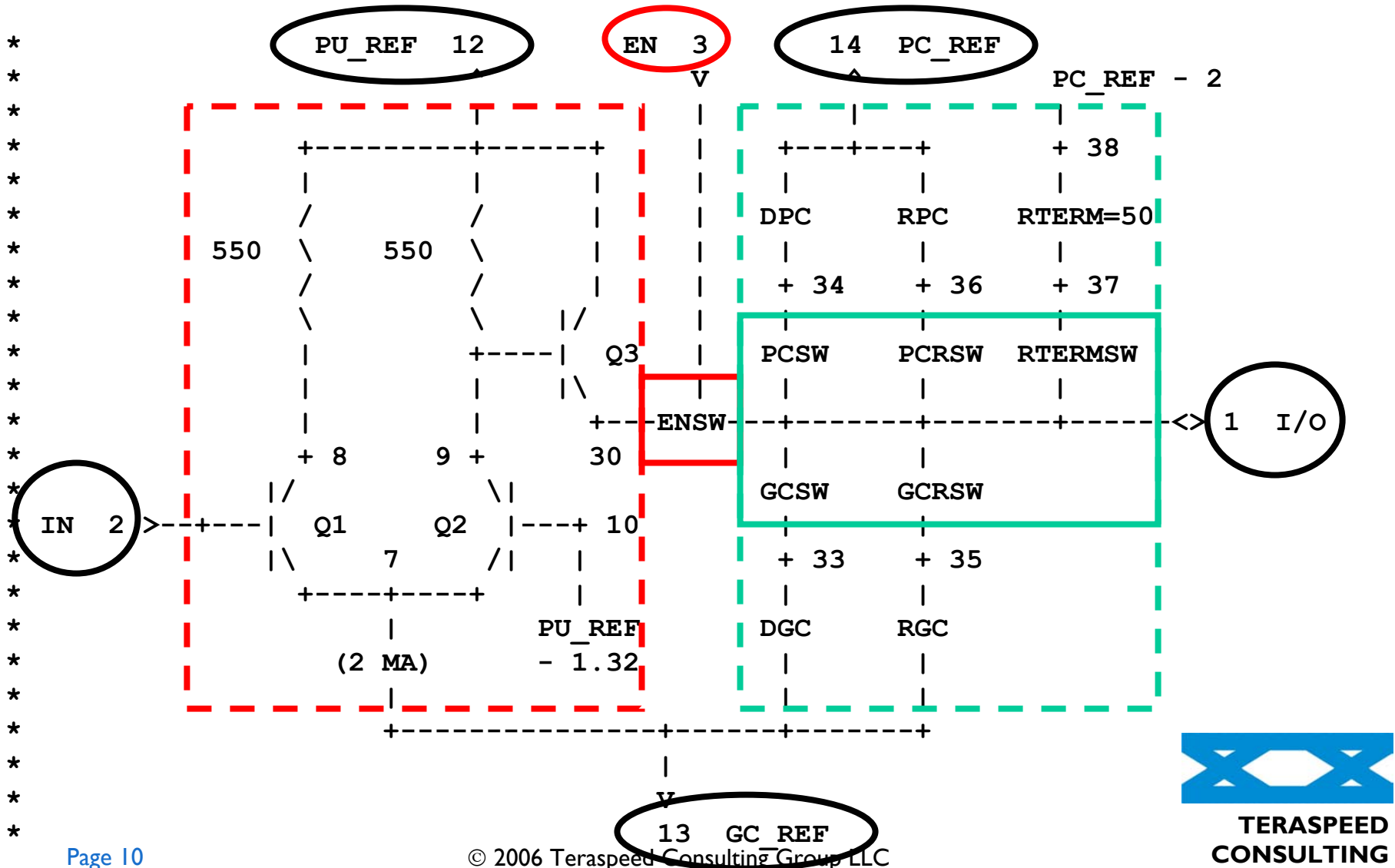


Chopped – can cause double counting of ODT currents in some EDA tools

DEC and Some Other Choices from Ross, 9/2005 ODT Presentation



ECL (PECL) Buffer



ECL (PECL) Configuration Control

.SUBCKT ECLTEST

* ON-OFF CONFIGURATION SWITCHES

* (1 OR ABOVE = ON, 0 = OFF)

*

VGC	1	GND CLAMP
VPC	1	POWER CLAMP
VGCR	0	INTERNAL GND CLAMP RESISTOR (3K ohm)
VPCR	0	INTERNAL POWER CLAMP RESISTOR (2K ohm)
VTERM	0	INTERNAL 50 OHM TERMINATOR TO VCC - 2

Diode Clamps, 2 k Ω
and 3 k Ω ODTs, and
50 Ω Internal
Terminator

VEN = 1	VEN = 1,0	VEN = 0
Output_ECL	I/O_ECL,	Input_ECL
	3-state_ECL	

Enable (ECL/PECL voltage
levels require EN voltage
shifts so that "0" is off)

*

	Control I/O Inputs			Voltage References			Configuration Switches (1 = ON)					
	---	---	---	---	---	---	-----					
.SUBCKT ECLTEST	1	2	3	12	13	14	23	24	25	26	27	
	I/O	IN	EN	PU	GC	PC	GC	PC	GCR	PCR	R50	
									3K	2K	50_2V	

*

I/O, Input
and **Enable**

Voltage
Refs

Clamps and ODT
Configuration



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Extraction Tests

- CMOSTEST and ECLTEST for advanced extraction testing
 - All Model_type configurations
 - Voltage reference settings
 - Clamps and internal ODT
 - Double counting
 - Truncation of tables
 - Differential models though subcircuit calls
 - Typ-Min-Max alignment
- Does any s2ibis tool consider all these cases??
 - Otherwise need several passes and hand calculations
- Not covered
 - Submodel modes (for example: DDR2 ODT)
 - Pre-emphasis - [Driver Schedule] partitioning