

# Gate modulation and BIRD97/98

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# Background

#### • It all started with BIRD95 "Power Integrity Analysis using IBIS"

- BIRD95 introduces additional I-t tables to be used with the well known V-t tables in order to account for the power and ground supply currents more accurately during the high to low or low to high transitions
- It was noted that in order to describe the supply currents more accurately during these transients, we would also need to include the gate modulation effect in the model
  - The gate modulation effect refers to changes in the output current due to the supply voltage variations
  - This motivated the authors to start writing BIRD97 "Gate modulation effect"
  - BIRD98 is essentially the same content using a tabulated format to help IP protection
- Simulation experiments with a transistor level buffer model revealed a dynamic relationship between  $I_{out}$  and the on-die supply voltage
  - BIRD97/98 describe a static (or direct) relationship between I<sub>out</sub> and the supply voltage variations
  - In reality there are also some delay factors involved (i.e. reaction time)





# **Summary of prior work**

- Informal presentations in the IBIS Open Forum Teleconference and the IBIS Futures teleconference documented numerous simulation waveforms to show how the buffer reacts to voltage variations in the power supply
  - V<sub>out</sub> as a function of V<sub>supply</sub> of a transistor level model was shown as the voltage was stepped down from 5 to 4 V at various slopes
  - The response of a statically scaled behavioral model was compared against a transistor level model
  - The sensitivity to C\_comp splitting was demonstrated
  - An idea for a possible solution using additional RC circuit(s) to account for the internal delays was introduced

http://www.vhdl.org/pub/ibis/futures/Quiet\_line\_experiment\_2.pdf

• The next few pages will show some of the highlights





# **Simulation circuit**



In the initial experiments the buffer model was an HSPICE transistor level model from the IBIS class labs.

A Verilog-A model was also used in later experiments in which the 2EQ/2UK basic IBIS algorithm was modified so that the output current would be scaled proportionally with the supply variations.





#### The transistor model's output response (high state)



The input was held steady (high). The supply voltage was stepped from 5 to 4 V at various rates. The reaction at the pad voltage was observed.





#### Zooming in to see the details...







### Gate voltage of the output transistors (high state)



In high state the gates of the output transistors are "tied" to the local "DieGND" by the pre-driver transistor's channel. In this case "DieGND" was not moving, yet the gate voltages were.





#### Zooming in to see the details...



The waveforms of the gate voltages look very similar to the exponential response of RC circuits.







#### **Percent deviation of I**<sub>out</sub> (high state)







#### **C\_comp splitting changes the deviation (high state)**







# **Additional RC explained**



#### The circuit shown here also agrees with the results of other presentations

http://www.vhdl.org/pub/ibis/birds/bird79.txt http://www.eda.org/pub/ibis/summits/mar02/giacotto.pdf http://www.eda.org/pub/ibis/summits/jun02/giacotto.pdf http://www.eda-stds.org/ibis/summits/apr04/mirmak2.pdf http://www.eda-stds.org/ibis/summits/oct04/mirmak2.pdf





## Series RC || with I-V and C\_comp - modulating V<sub>out</sub>







#### Zooming in to see the details...





# **Counting the possible sources of RC effects**

- Pullup transistor ON state
- Pullup transistor OFF state
- Pullup transistor's channel and C<sub>ds</sub> to top supply rail
- Pullup transistor's  $C_{gs}$  to top supply rail
- Pulldown transistor ON state
- Pulldown transistor OFF state
- Pulldown transistor's channel and C<sub>ds</sub> to GND supply rail
- Pulldown transistor's  $C_{gs}$  to GND supply rail
- and the list probably goes on...
- It is most likely impossible to obtain values for this many parameters using a black-box like characterization technique without additional test hooks in the buffer





# **Series RC || with I-V and C\_comp - modulating V**<sub>supply</sub>





### Same as previous with "tweaked" RC values



Waveforms are better, but RC values seem to be unreasonable.





#### Use the waveform of the RC node to scale the I-V curves



### Using RC waveform to scale I-V curves (low state)



RC parameters more reasonable, but still unable to match all waveforms equally well.







#### Using RC waveform to scale I-V curves (high state)

Unable to match all waveforms in the high state either.





# **Problems**

- None of these techniques resulted in an improvement that made the correlation better than 3%
- Additionally, in all of these experiments the buffer was in a steady high or low state (i.e. it was not in a transient condition)
- The main purpose of BIRD97/98 was to improve on the transient waveforms by accounting for the changes in the drive strength due to the supply voltage fluctuations during transients
- What will happen if we tried matching the buffer behavior while it is switching?





#### The 2EQ / 2UK algorithm revisited



$$0 = k_{pu}(t) \cdot IV_{pu}(V_{wfm1}(t)) + IV_{pc}(V_{wfm1}(t)) - k_{pd}(t) \cdot IV_{pd}(V_{wfm1}(t)) - IV_{gc}(V_{wfm1}(t)) - I_{out}(V_{wfm1}(t)))$$
  
$$0 = k_{pu}(t) \cdot IV_{pu}(V_{wfm2}(t)) + IV_{pc}(V_{wfm2}(t)) - k_{pd}(t) \cdot IV_{pd}(V_{wfm2}(t)) - IV_{gc}(V_{wfm2}(t)) - I_{out}(V_{wfm2}(t)))$$

where

$$I_{out} = \frac{V_{out} - V_{fixture}}{R_{fixture}}$$

and wfm1 and wfm2 are waveforms of the same switching direction (rising edges or falling edges) obtained with two different  $V_{fixture}$  values (usually Vcc and GND)





### The bottom line...

- The two equations find  $k_{pu}(t)$  and  $k_{pd}(t)$  such that  $I_{out}$  of the behavioral model matches  $I_{out}$  obtained from the V-t curves
- These equations do not include  $I_{vcc}$  or  $I_{gnd}$ , therefore  $k_{pu}(t)$ ,  $k_{pd}(t)$ , and consequently  $I_{pu}$  and  $I_{pd}$  could be practically anything as long as  $I_{out}$  is good
- BIRD95 tries to remedy this situation with the I-t tables measured at Vcc in order to be able to get more accurate waveforms at Vcc and GND during simulations, but it does not give any detail on how much of the current in the I-t table comes from the pre-driver or the output stage
- If we don't know the exact  $k_{pu}(t)$  and  $k_{pd}(t)$ , or  $I_{pu}$  and  $I_{pd}$  while the buffer is changing states, how can we refine them by scaling them further using the supply voltage variations?





# Conclusions

• Since the scaling coefficients of the I-V curves are more or less bogus during transients, no refinements can be added to them to account for the gate modulation effect

- two wrongs don't make a right...

- In order to achieve this level of detail we would first need to replace the 2EQ/2UK algorithm with a different one to account for the power and ground currents correctly during the state transitions of the buffer
- Based on this, the best we can do at this point is a static scaling as described in BIRD98 (or nothing) since there is no way to improve the accuracy of the switching currents without rethinking the fundamental algorithms



